



Programmable Binary Counter

**ELECTRICALLY TESTED PER:
MPG54LS718**

These monolithic devices are programmable, cascadable, modulo-N-counters. The 54LS716 can be programmed to divide by any number (N) from 0 through 9, the 54LS718 from 0 through 15.

The parallel enable (\overline{PE}) input enables the parallel data inputs D_0 through D_3 . All zeros are entered into the counter by applying a logic "0" level to the master reset (\overline{MR}) and \overline{PE} inputs. This causes the counter to stop counting (count = 0). All data inputs are independent of the logic level of the Clock.

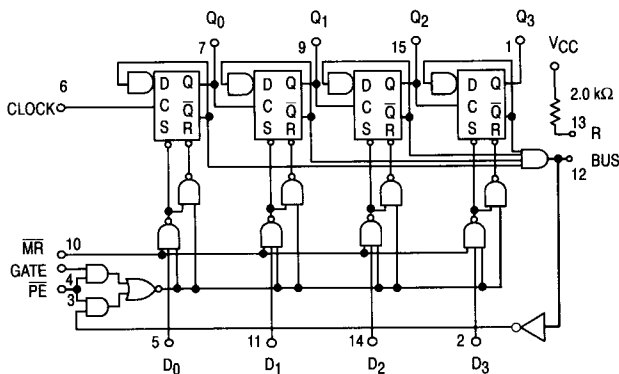
Modulo-N counters are useful in frequency synthesizers, in phase-locked loops, and in other applications where a simple method for frequency division is needed.

All Types:

Input Loading Factor:
Clock, \overline{PE} = 2
 D_0, D_1, D_2, D_3 Gate = 1
 \overline{MR} = 4
Output Loading Factor = 8

Total Power Dissipation =
85 mW typ/pkg
Propagation Delay Time:
Clock to Q_3 = 50 ns typ
Clock to Bus = 35 ns typ

LOGIC DIAGRAM



Military 54LS718



AVAILABLE AS:

- 1) JAN: N/A
- 2) SMD: N/A
- 3) 883: 54LS718/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

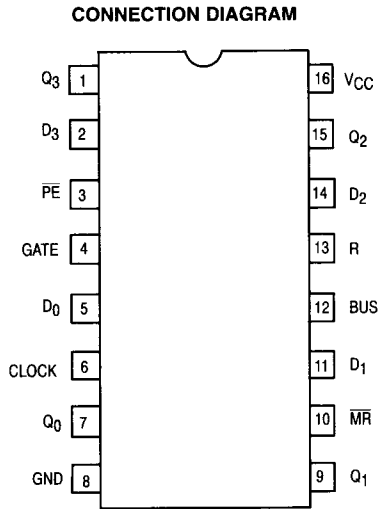
PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
Q_3	1	1	2	VCC
D_3	2	2	3	VCC
\overline{PE}	3	3	4	GND
GATE	4	4	5	VCC
D_0	5	5	7	VCC
CLK	6	6	8	VCC
Q_0	7	7	9	VCC
GND	8	8	10	GND
Q_1	9	9	12	VCC
\overline{MR}	10	10	13	GND
D_1	11	11	14	VCC
BUS	12	12	15	PN17
R	13	13	17	PN15
D_2	14	14	18	VCC
Q_2	15	15	19	VCC
VCC	16	16	20	VCC

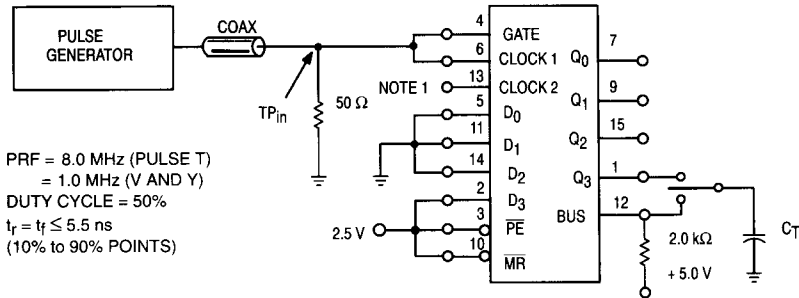
**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

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TRUTH TABLE				
Count	Outputs			
	Q ₃	Q ₂	Q ₁	Q ₀
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



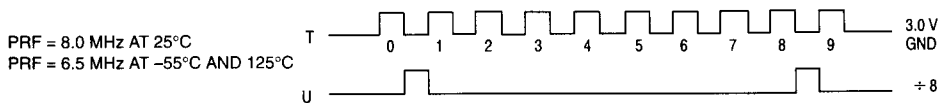
FUNCTIONAL SWITCHING TIME CIRCUIT



$C_T = 50$ pF = TOTAL PARASITIC CAPACITANCE WHICH INCLUDES PROBE, WIRING, AND LOAD CAPACITANCE.

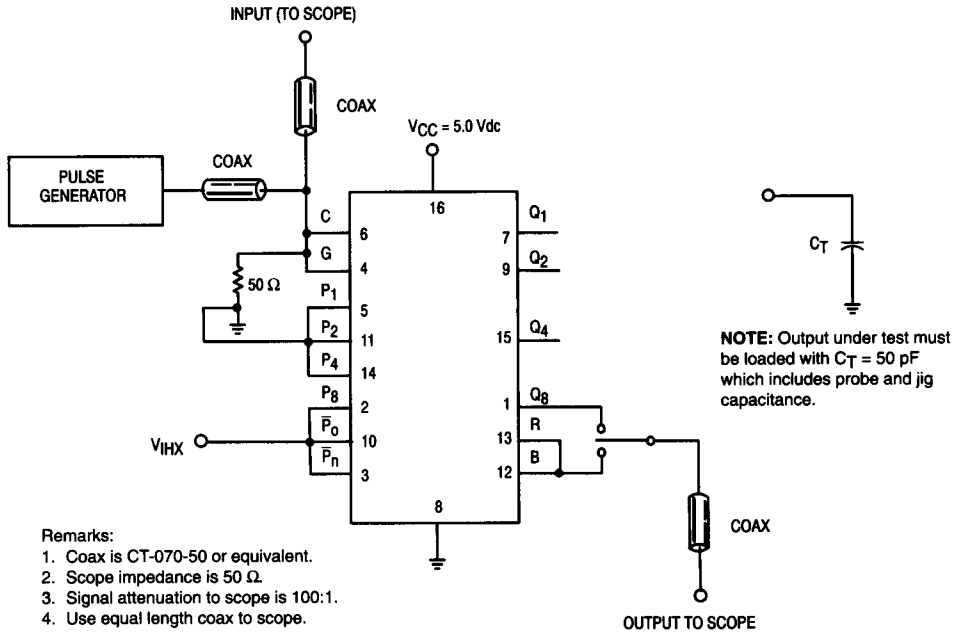
NOTE:

- Counter programmed for ÷ 8 operation, Pin 13 is the resistor pin, and left open.

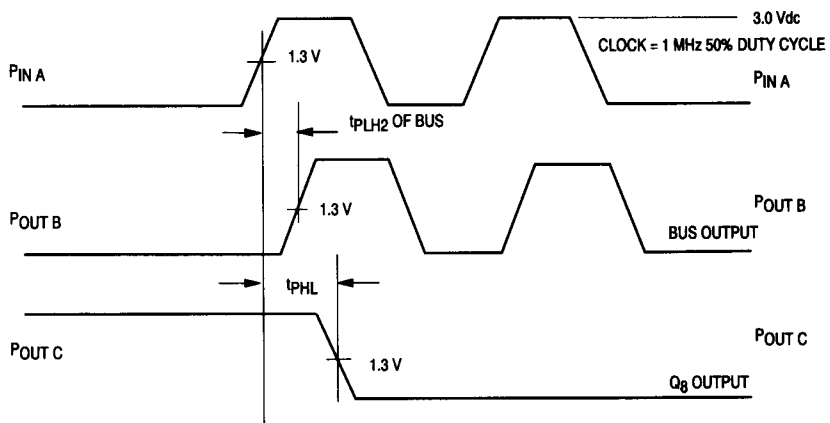


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SWITCHING CIRCUIT AND WAVEFORMS

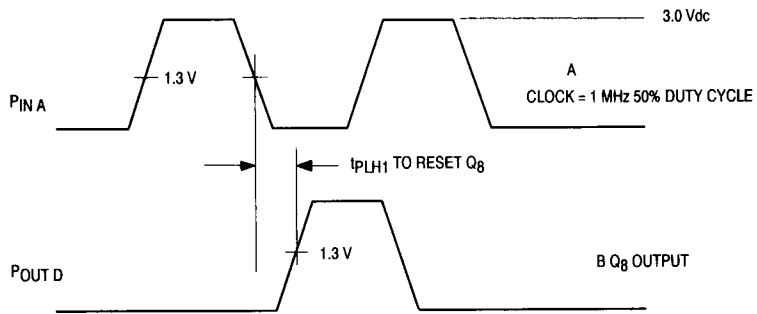


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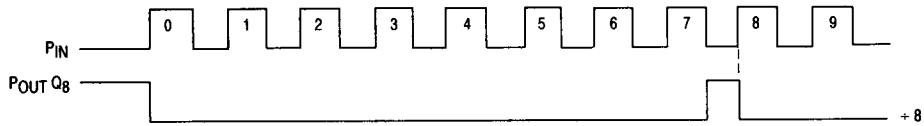
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SWITCHING CIRCUIT WAVEFORM



NOTE:

Check output waveform as shown below prior to measuring propagation delay.



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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{IH} = 2.0 V, V _{IL} = 0.7 V, other inputs are open.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 12 mA, V _{IL} = 0.7 V, V _{IH} = 2.0 V, other inputs are open.
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IH}	Logical "1" Input Current		40		40		40	μA	V _{CC} = 5.5 V, V _{IH} (PE) = 2.7 V, other inputs are open, Gate = GND.
I _{IHH}	Logical "1" Input Current		200		200		200	μA	V _{CC} = 5.5 V, V _{IHH} (PE) = 5.5 V, other inputs are open, Gate = GND.
I _{IH}	Logical "1" Input Current		80		80		80	μA	V _{CC} = 5.5 V, V _{IH} (MR) = 2.7 V, other inputs are open, D ₀ -D ₃ = GND.
I _{IHH}	Logical "1" Input Current		400		400		400	μA	V _{CC} = 5.5 V, V _{IHH} (MR) = 5.5 V, other inputs are open, D ₀ -D ₃ = GND.
I _{IL}	Logical "0" Input Current		- 0.4		- 0.4		- 0.4	mA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs are open.
I _{IL}	Logical "0" Input Current		- 0.8		- 0.8		- 0.8	μA	V _{CC} = 5.5 V, V _{IL} (PE) = 0.4 V, other inputs are open, MR = 2.7 V.
I _{IL}	Logical "0" Input Current		- 1.6		- 1.6		- 1.6	μA	V _{CC} = 5.5 V, V _{IL} (MR) = 0.4 V, other inputs are open, D ₀ -D ₃ = 2.7 V.
I _{OS}	Output Short Circuit Current	- 30	- 130	- 30	- 130	- 30	- 130	mA	V _{CC} = 5.5 V, V _{IN} = 2.7 V, other inputs are open, PE = 0.7 V, V _{OUT} = GND.
I _{CC}	Power Supply Current Off		32		32		32	mA	V _{CC} = 5.5 V, V _{IN} = GND, other inputs are open.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, (Repeat at) V _{CC} = 5.5 V, V _{INL} = 0.4 V, and V _{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay Clock to Q _n		93 78		125 120		125 120	ns	V _{CC} = 5.0 V, C _T = 50 pF, R _L = 50 Ω. V _{CC} = 5.0 V, C _T = 15 pF.
t _{PLH1} t _{PHL1}	Propagation Delay Gate to Q _n		35 35		50 44		50 44	ns	V _{CC} = 5.0 V, C _T = 50 pF, R _L = 50 Ω. V _{CC} = 5.0 V, C _T = 15 pF.
t _{PHL2} t _{PHL2}	Propagation Delay Clock to Bus		80 65		95 90		95 90	ns	V _{CC} = 5.0 V, C _T = 50 pF, R _L = 50 Ω. V _{CC} = 5.0 V, C _T = 15 pF.
f _{tog} f _{tog}	Toggle Frequency	8.0 8.0		6.5 —		6.5 —		MHz	V _{CC} = 5.0 V, C _T = 50 pF, R _L = 50 Ω. V _{CC} = 5.0 V, C _T = 15 pF.

NOTE:

- The limits specified for C_T = 15 pF is guaranteed but not tested.