

SED1722/24

CMOS LCD DRIVER

● CMOS 80-Bit Segment Driver

■ DESCRIPTION

The SED1722/24 is an 80 dot matrix LCD segment (column) driver for driving high-capacity LCD panels at duty cycles higher than 1/100 (up to 1/500). The LSI features a wide range of LCD drive voltages.

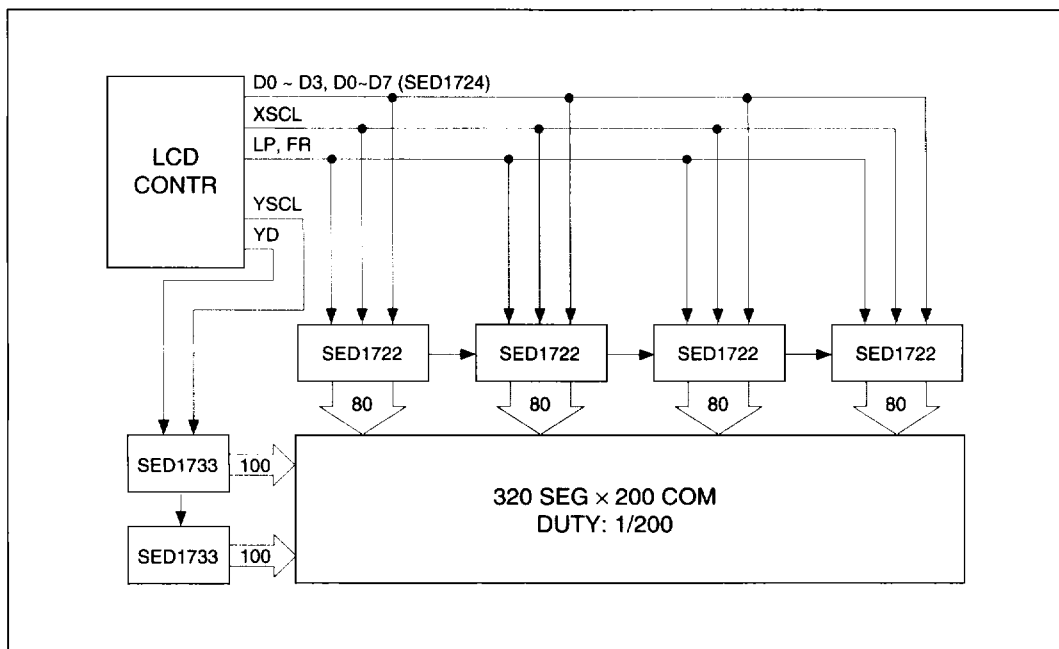
The device uses a high-speed daisy-chain enable system which decreases power consumption and eliminates the need for separate enable signals for each driver.

The SED1722/24 is used in conjunction with the SED1733F (100-bit output common driver) to drive a large-capacity dot matrix LCD panel.

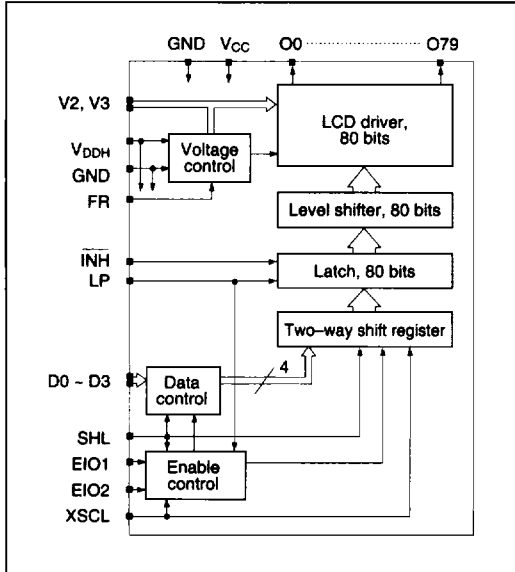
■ FEATURES

- Low-power high-speed CMOS technology
- 80-bit segment (column) driver
- High-speed data bus 4-bit (SED1722)
8-bit (SED1724)
- Duty cycle 1/100 to 1/500
- Shift clock frequency 12 MHz
- Adjustable LCD drive voltages
- Selectable output shift direction
- Supports display blanking
- Low output resistance
- Ability to adjust offset bias of the LCD source from V_{DD}
- Low output impedance 1K Ω
- Wide range of LCD voltage 14 to 40V
- Supply voltage 4.5 to 5.5V
- Package QFP-5 100 pins (FoA)
AI pad (DoA)

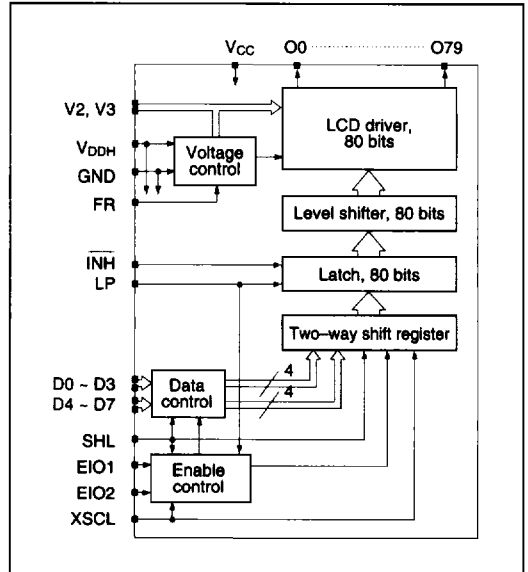
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM
● SED1722



● SED1724



■ PIN DESCRIPTION

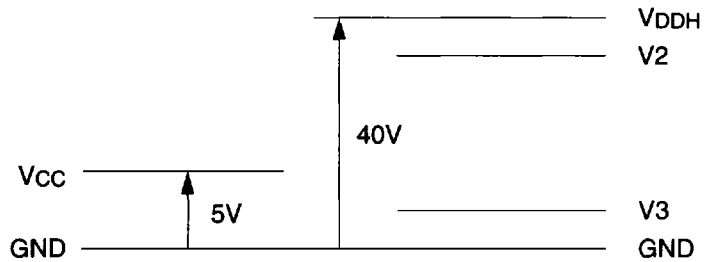
Pin Name	I/O	Function	Q'ty																																															
O0 to 79	O	To output the driving segment (column). The output changes at the LP fall edge.	80																																															
D0 to D3 (SED1722)	I	To input display data. H: Selection data, L: Non-selection data	4																																															
D0 to D7 (SED1724)	I	To input display data. H: Selection data, L: Non-selection data	8																																															
XSCL	I	To input shift clock for display data (fall edge trigger)	1																																															
LP	I	To input latch pulse for display data (fall edge trigger)	1																																															
EI01 EI02	I/O	Enable input and output: Input or output is set on the SHL input level. Output is reset by an input to LP and falls to "L" automatically when 80-bit data is completely fetched in.	2																																															
SHL	I	To select shift direction and to input input-output control data for the EIO terminal. <In the case of SED1724> When the data are input to (D0, D1,.. D7) terminals in the order of (a, b, .. g, h), (i,.. o, p) ... (s, t,.. y, z), relations between data and segment outputs come to be as per the following table: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th rowspan="2">SHL</th> <th colspan="9">O (SEG Output)</th> <th colspan="2">EIO</th> </tr> <tr> <th>0</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>.....</th> <th>77</th> <th>78</th> <th>79</th> <th>1</th> <th>2</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>a</td> <td>b</td> <td>c</td> <td>d</td> <td>e</td> <td>.....</td> <td>x</td> <td>y</td> <td>z</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>L</td> <td>z</td> <td>y</td> <td>x</td> <td>w</td> <td>v</td> <td>.....</td> <td>c</td> <td>b</td> <td>a</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table> <p>Note: The relations between data and segment outputs are set irrespectively to number of shift locks.</p>	SHL	O (SEG Output)									EIO		0	1	2	3	4	77	78	79	1	2	H	a	b	c	d	e	x	y	z	Input	Output	L	z	y	x	w	v	c	b	a	Output	Input	1
SHL	O (SEG Output)									EIO																																								
	0	1	2	3	4	77	78	79	1	2																																							
H	a	b	c	d	e	x	y	z	Input	Output																																							
L	z	y	x	w	v	c	b	a	Output	Input																																							
FR	I	To input AC signal for LCD driving output.	1																																															
Vcc, GND	Power Supply	Logic power supply, GND: 0 V, Vcc: +5 V	2																																															
VDDH	Power Supply	Power supply for LCD driving circuit VDDH: +14 V to 40 V, (Liquid crystal driving selection level)	1																																															
V2, V3	Power Supply	Power supply for driving liquid crystal VDDH ≥ V2 ≥ 7/9 VDDH, 2/9 VDDH ≥ V3 ≥ GND	2																																															
$\overline{\text{INH}}$	I	Forced blank input Output on the "L" level are forced to non-selection level.	1																																															

■ ELECTRICAL CHARACTERISTICS
 ● Absolute Maximum Ratings

(GND = 0 V)

Parameter	Symbol	Ratings	Unit
Supply voltage (1)	V _{cc}	-0.3 to +7.0	V
Supply voltage (2)	V _{DDH}	-0.3 to +45.0	V
Supply voltage (3)	V ₂ , V ₃	-0.3 to V _{DDH} +0.3	V
Input voltage	V _i	-0.3 to V _{cc} +0.3	V
Output voltage	V _o	-0.3 to V _{cc} +0.3	V
EIO output current	I _{o1}	20	mA
LCD circuit output current	I _{o2}	20	mA
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-65 to +150	°C

Note 1. Let the V₂ and V₃ voltages maintain the condition, V_{DDH} ≥ V₂ ≥ V₃ ≥ GND, all the time.



Note 2. If the logic circuit power supply comes to float power-supply voltage supply voltage is applied to the liquid crystal driving circuit, the LSI may be broken permanently. So, prevent the logic circuit power supply from floating. Pay special attention to the power supply sequence when the system is switched on or off.

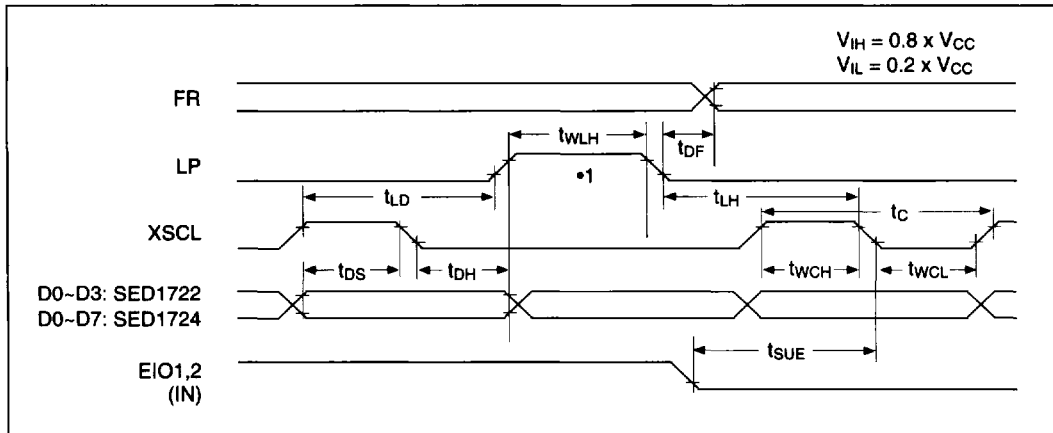
● DC Electrical Characteristics

(Unless otherwise specified, GND=0V, VCC= +5.0V±10%, Ta= -20 to 75°C)

Parameter	Symbol	Condition	Terminal	Min	Typ	Max	Unit	
Supply voltage (1)	VCC		VCC	4.5	5.0	5.5	V	
Recommended supply voltage	VDDH		VDDH	14.0	—	40.0	V	
Operable voltage	VDDH	Function	VDDH	8.0	—	—	V	
Supply voltage (2)	V2	Recommendation value	V2	7/9VDDH	—	VDDH	V	
Supply voltage (3)	V3	Recommendation value	V3	GND	—	2/9VDDH	V	
High level input voltage	VIH		EIO1, EIO2, D0 to D3: (SED1722) D0 to D7 (SED1724), XSCL, SHL, FR, LP, INH	0.8VCC	—	VCC	V	
Low level input voltage	VIL			GND	—	0.2VCC	V	
High level output voltage	VOH	IOH = -0.6 mA	EIO1, EIO2	VCC-0.4	—	VCC	V	
Low level output voltage	VOL	IOL = 0.6 mA		GND	—	0.4	V	
Input leak current	ILI	GND ≥ VIN ≥ VCC	D0 to D3: (SED1722) D0 to D7 (SED1724), SHL, XSCL, LP, FR, INH	—	—	2.0	μA	
Input-output leak current	II/O	GND ≥ VIN ≥ VCC	EIO1, EIO2	—	—	5.0	μA	
Static current	IGND	VDDH = 14.0 to 40.0 V VIH = VCC, VIL = GND	GND	—	—	25	μA	
Output resistance.	RSEG	ΔVON = 0.5V	*1 O0 to O79	VDDH=+30.0V	—	0.7	1.8	kΩ
				VDDH=+20.0V	—	0.8	2.2	
				VDDH=+14.0V	—	1.0	2.6	
Current consumed (1)	ICC	VCC = +5.0 V, VIH = VCC, VIL = GND, fXSCL = 5.38 MHz, fLP = 33.6 kHz, fFR = 70 Hz; Input data: To be inverted 1 bit/1H. No load	VCC	—	0.5	1.5	mA	
Current consumed (2)	IDDH	VCC = +5.0 V, V3 = +4.0 V, V2 = +26.0 V, VDDH = +30.0V Other conditions are same as those of ICC	VDDH	—	0.2	1.5	mA	
Input terminal capacity	CI	Freq.=1 MHz, Ta = 25°C	D0 to D3: (SED1722) D0 to D7 (SED1724), SHL, XSCL, LP, FR, INH	—	—	8	pF	
I/O terminal capacity	CI/O		EIO1, EIO2	—	—	15	pF	

*1. The output resistance is specified within the ranges of the supply voltages (2) and (3).

● AC Electrical Characteristics
 ○ Input Timing Characteristics

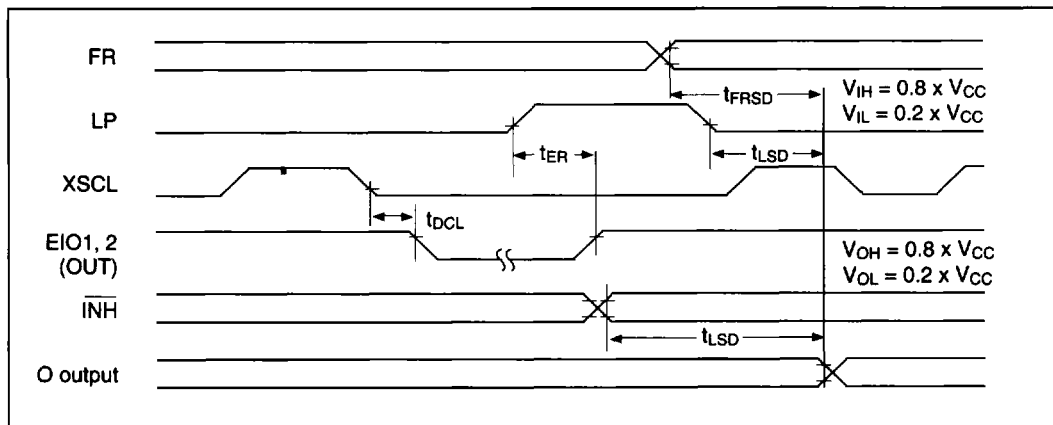


($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_a = -20 \text{ to } 75^\circ\text{C}$)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
XSCL cycle	t_C		83	—	—	ns
XSCL high level pulse width	t_{WCH}		30	—	—	ns
XSCL low level pulse width	t_{WCL}		30	—	—	ns
Data setup time	t_{DS}		30	—	—	ns
Data hold time	t_{DH}		20	—	—	ns
XSCL to LP rise time	t_{DL}		0	—	—	ns
LP to XSCL fall time	t_{LH}		200	—	—	ns
LP high level pulse width	t_{WLH}	see note	70	—	—	ns
FR delay allowable time	t_{DF}		-300	—	300	ns
EIO setup time	t_{SUE}		36	—	—	ns

Note: t_{WLH} is the time when LP is "H" and XSCL is "L"

○ Output Timing Characteristics

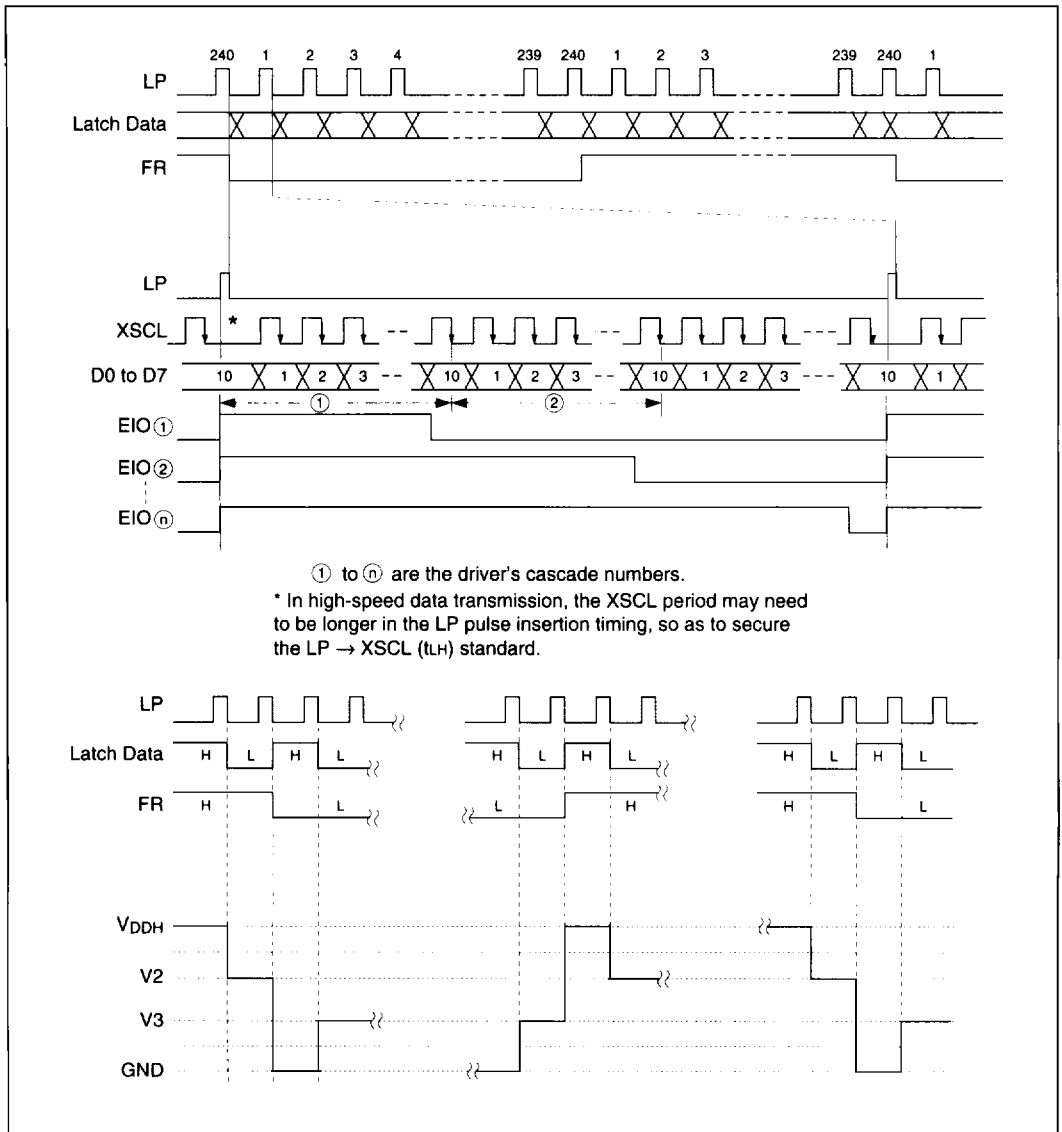


($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{DDH} = 14.0\text{ to }40.0\text{ V}$, $T_a = -20\text{ to }75^\circ\text{C}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EIO reset time	t_{ER}	$C_L = 15\text{ pF}$	—	—	120	ns
EIO output delay time	t_{DCL}		—	—	45	ns
LP to output delay time	t_{LSD}	$C_L = 100\text{ pF}$	—	—	0.5	μs
FR to output delay time	t_{FRSD}		—	—	0.7	μs
INH to output delay time	t_{pdINH}		—	—	0.5	μs

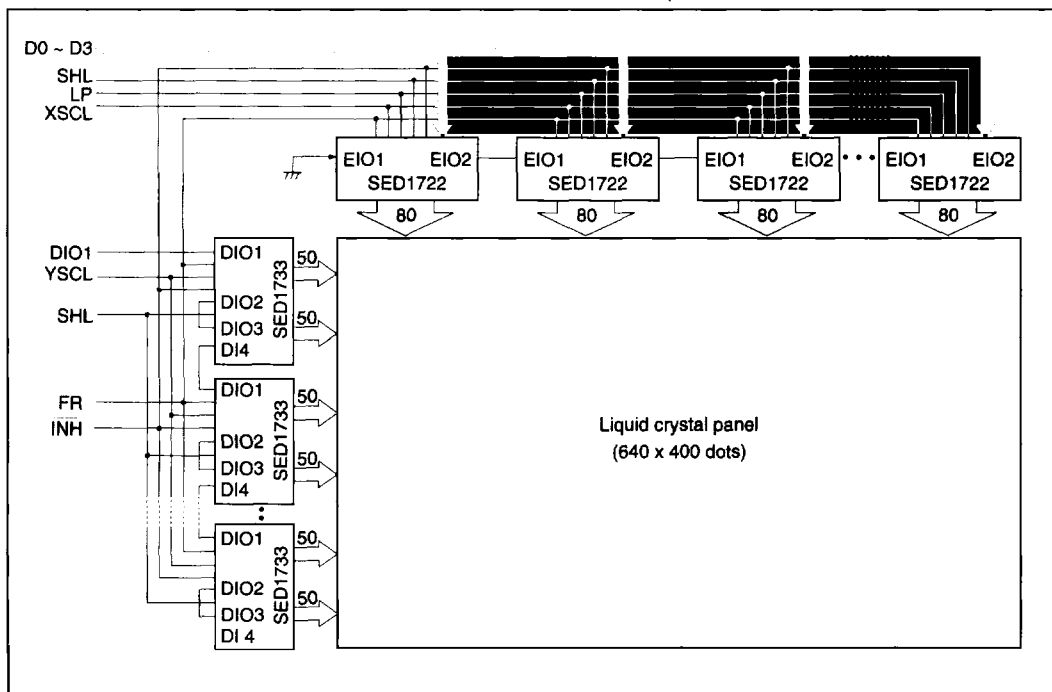
■ Timing Diagram

When it is 1/240 duty (example for reference)

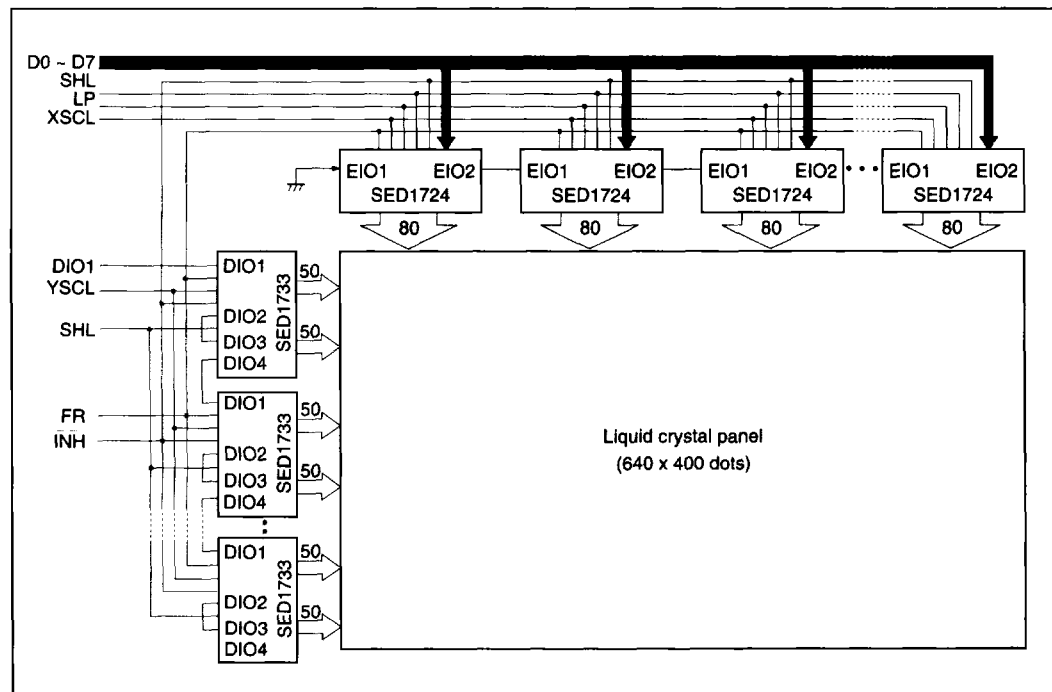


■ EXAMPLE OF REFERENCE CIRCUIT

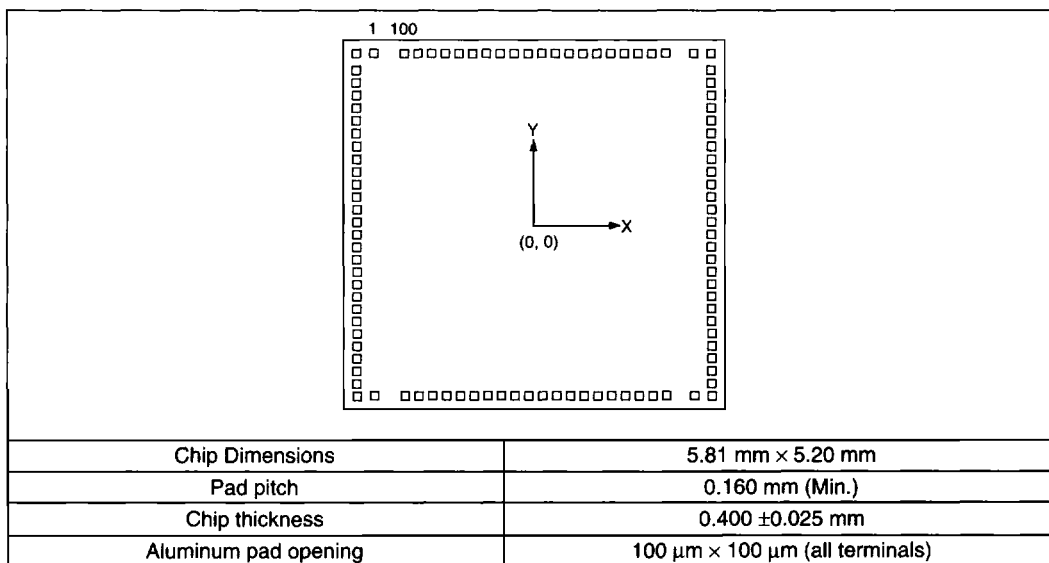
(Combination of SED1722 with SED1733)



(Combination of SED1724 with SED1733)



■ PAD LAYOUT (SED1722D0A, SED1724D0A)



■ PAD COORDINATES

Pad		X (μm)	Y (μm)
Number	Name		
1	O 50	-2488	2432
2	O 51	-2488	2432
3	O 52	-2738	2222
4	O 53	-2738	2022
5	O 54	-2738	1835
6	O 55	-2738	1660
7	O 56	-2738	1485
8	O 57	-2738	1310
9	O 58	-2738	1135
10	O 59	-2738	960
11	O 60	-2738	785
12	O 61	-2738	610
13	O 62	-2738	435
14	O 63	-2738	260
15	O 64	-2738	85
16	O 65	-2738	-85
17	O 66	-2738	-260
18	O 67	-2738	-435
19	O 68	-2738	-610
20	O 69	-2738	-785
21	O 70	-2738	-960
22	O 71	-2738	-1135
23	O 72	-2738	-1310
24	O 73	-2738	-1485
25	O 74	-2738	-1660
26	O 75	-2738	-1835
27	O 76	-2738	-2022
28	O 77	-2738	-2222
29	O 78	-2738	-2432
30	O 79	-2488	-2432
31	EIO2	-2000	-2432
32	EIO1	-1750	-2432
33	D0	-1500	-2432
34	D1	-1300	-2432

Pad		X (μm)	Y (μm)
Number	Name		
35	D2	-1100	-2432
36	D3	-900	-2432
37	NC/D4	-700	-2432
38	NC/D5	-500	-2432
39	NC/D6	-300	-2432
40	NC/D7	-100	-2432
41	SHL	100	-2432
42	XSCL	300	-2432
43	INH	500	-2432
44	LP	700	-2432
45	FR	900	-2432
46	Vcc	1100	-2432
47	V2	1300	-2432
48	V3	1500	-2432
49	GND	1750	-2432
50	VDDH	2000	-2432
51	O 0	2488	-2432
52	O 1	2738	-2432
53	O 2	2738	-2222
54	O 3	2738	-2022
55	O 4	2738	-1835
56	O 5	2738	-1660
57	O 6	2738	-1485
58	O 7	2738	-1310
59	O 8	2738	-1135
60	O 9	2738	-960
61	O 10	2738	-785
62	O 11	2738	-610
63	O 12	2738	-435
64	O 13	2738	-260
65	O 14	2738	-85
66	O 15	2738	85
67	O 16	2738	260
68	O 17	2738	435

Pad		X (μm)	Y (μm)
Number	Name		
69	O 18	2738	610
70	O 19	2738	785
71	O 20	2738	960
72	O 21	2738	1135
73	O 22	2738	1310
74	O 23	2738	1485
75	O 24	2738	1660
76	O 25	2738	1835
77	O 26	2738	2022
78	O 27	2738	2222
79	O 28	2738	2432
80	O 29	2488	2432
81	O 30	2000	2432
82	O 31	1750	2432
83	O 32	1500	2432
84	O 33	1300	2432
85	O 34	1100	2432
86	O 35	900	2432
87	O 36	700	2432
88	O 37	500	2432
89	O 38	300	2432
90	O 39	100	2432
91	O 40	-100	2432
92	O 41	-300	2432
93	O 42	-500	2432
94	O 43	-700	2432
95	O 44	-900	2432
96	O 45	-1100	2432
97	O 46	-1300	2432
98	O 47	-1500	2432
99	O 48	-1750	2432
100	O 49	-2000	2432