



PM-7574/883

CMOS MICROPROCESSOR-COMPATIBLE 8-BIT A/D CONVERTER

Precision Monolithics Inc.

1.0 SCOPE

This specification covers the detail requirements for an 8-bit microprocessor compatible monolithic CMOS analog-to-digital converter which uses the successive-approximation technique to provide a conversion time of 15 μ s.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

1.2 Part Number. The complete part numbers per Table I of this specification follow:

<u>Device</u>	<u>Part Number</u>	<u>Package</u>
A	PM-7574AX/883	X
B	PM-7574BX/883	X
B	PM-7574BRC/883	RC*

*Future product, contact PMI Sales for present availability.

1.2.3 Case Outline.

<u>Letter</u>	<u>Case Outline (Lead finish per MIL-M-38510)</u>
X	18-lead ceramic dual-in-line package (CERDIP)
RC	20-contact hermetic leadless chip carrier (LCC)

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$, unless otherwise noted)

V_{DD} to AGND	0V, +7V
V_{DD} to DGND.....	0V, +7V
AGND to DGND.....	$\pm 0.3\text{V}$
Digital Input Voltage (Pin 15-16) to DGND.....	-0.3V, V_{DD}
Digital Output Voltage (Pin 6-14) to DGND.....	-0.3V, V_{DD}
Clock Input Voltage (Pin 17) to DGND.....	-0.3V to V_{DD}
V_{REF} (Pin 2)	-0V, -20V
V_{BOFS} (Pin 3)	$\pm 20\text{V}$
V_{AIN} (Pin 4)	$\pm 20\text{V}$
Power Dissipation	
To +75 $^\circ\text{C}$ (any package)	450mW
Derate above +75 $^\circ\text{C}$ by.....	6.0mW/ $^\circ\text{C}$
Operating Temperature Range	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
Storage Temperature Range.....	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Lead Temperature (Soldering, 10 sec).....	+300 $^\circ\text{C}$

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1.5 Thermal Characteristics:

Thermal Resistance, CERDIP (X) package:

Junction-to-Case (θ_{JC}) = 35 °C/W MAX

Junction-to-Ambient (θ_{JA}) = 120 °C/W MAX

Thermal Resistance, LCC (RC) package:

Junction-to-Case (θ_{JC}) = 35 °C/W MAX

Junction-to-Ambient (θ_{JA}) = 110 °C/W MAX

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TABLE 1

$V_{DD} = +5V$; $V_{REF} = -10V$; $AGND = DGND = 0V$; Unipolar Configuration; $R_{CLK} = 150k\Omega$; $C_{CLK} = 100pF$;
 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	PM-7574/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Resolution	RES		8	--	8	--	Bits
Integral Nonlinearity (Note 1)	INL		--	$\pm 1/2$	--	$\pm 3/4$	LSB
Differential Nonlinearity (Note 1)	DNL		--	$\pm 3/4$	--	$\pm 7/8$	LSB
Gain Error (Note 2)	AE		--	± 4.5	--	± 6.5	LSB
		$T_A = +25^{\circ}C$	--	± 3	--	± 5	LSB
Offset Error	V_{OS}		--	± 50	--	± 80	mV
		$T_A = +25^{\circ}C$	--	± 30	--	± 60	mV
Resistance Mismatch B_{OFS} (Pin 3) to A_{IN} (Pin 4)	ΔR_{AB}		--	± 1.5	--	± 1.5	%
Input Resistance	R_{IN}	@ V_{REF} (Pin 2)	5	15	5	15	k Ω
		@ B_{OFS} (Pin 3)	10	30	10	30	k Ω
		@ A_{IN} (Pin 4)	10	30	10	30	k Ω
Digital Input High Level	V_{IH}	\overline{RD} (Pin 15), \overline{CS} (Pin 16)	2.4	--	2.4	--	V
Digital Input Low Level	V_{IL}	\overline{RD} (Pin 15), \overline{CS} (Pin 16)	--	0.8	--	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	--	± 10	--	± 10	μA
		$V_{IN} = 0V$ or V_{DD} ; $T_A = +25^{\circ}C$	--	± 1	--	± 1	μA



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 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	PM-7574/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Digital Input Capacitance (Note 4)	C_{IN}		--	5	--	5	pF
Clock Input High Level	V_{IH}		3.0	--	3.0	--	V
Clock Input Low Level	V_{IL}		--	0.4	--	0.4	V
Clock Input High Current	I_{IH}		--	± 2	--	± 2	mA
Clock Input Low Current	I_{IL}	$T_A = +25^{\circ}C$	--	± 10	--	± 10	μA
			--	± 1	--	± 1	μA
Digital Output High Level (DB7-DB0; \overline{BUSY})	V_{OH}	$I_{SOURCE} = 40\mu A$	4	--	4	--	V
Digital Output Low Level (DB7-DB0; \overline{BUSY})	V_{OL}	$I_{SINK} = 1.6mA$	--	0.4	--	0.4	V
Supply Current from V_{DD}	I_{DD}	$A_{IN} = 0V$, \overline{BUSY} and \overline{RD} High	--	5	--	5	mA
Floating State Leakage Current (DB7-DB0)	I_{LKG}	$V_O = 0V$ or V_{DD} $V_O = 0V$ or V_{DD} ; $T_A = +25^{\circ}C$	--	± 10	--	± 10	μA
			--	± 1	--	± 1	μA
Floating State Output Capacitance (DB7-DB0) (Note 4)	C_{OUT}		--	7	--	7	pF



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 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	PM-7574/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
\overline{CS} Pulse Width (Note 4)	t_{CS}		150	--	150	--	ns
\overline{RD} to \overline{CS} Set-up Time (Note 4)	t_{WCS}		0	--	0	--	ns
\overline{CS} to \overline{BUSY} Propagational Delay (Note 4)	t_{CBPD}	BUSY load = 20pF	--	180	--	180	ns
		BUSY load = 100pF	--	200	--	200	ns
\overline{BUSY} to \overline{RD} Set-up Time (Note 4)	t_{BSR}		0	--	0	--	ns
\overline{BUSY} to \overline{CS} Set-up Time (Note 4)	t_{BSCS}		0	--	0	--	ns
Data Valid Access Time (DB0-DB7) (Note 4)	t_{RAD}	Load = 20pF	--	220	--	220	ns
		Load = 100pF	--	400	--	400	ns
Data Valid Hold Time (Note 4)	t_{RHD}		80	180	80	180	ns
\overline{CS} to \overline{RD} Hold Time (Note 4)	t_{RHCS}		--	500	--	500	ns
Reset Time Requirement (Note 4)	t_{RESET}		3	--	3	--	μS
\overline{RD} to \overline{BUSY} Propagation Delay (Note 4)	t_{WBPD}	BUSY load = 20pF	--	2	--	2	μS



TABLE 1

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 $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise specified.

Characteristics	Symbol	Special Conditions	PM-7574/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Conversion Time (Notes 1, 3 and 4)	$t_{CONVERT}$		--	15	--	15	μS

NOTES:

1. Measured using external clock frequency of 550kHz.
2. Gain Error is measured after calibrating out offset error.
3. Static RAM interface mode.
4. Design limit.



TABLE 2

PM-7574/883

**Electrical Test Requirements
For Class B Devices**

MIL-STD-883 Test Requirements	Subgroups (see Table 3)
Interim Electrical Parameters (pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3

* PDA applies to Subgroup 1 only.
No other Subgroups are included in PDA.



TABLE 3

Group A Inspection

$V_{DD} = +5V$; $V_{REF} = -10V$; $AGND = DGND = 0V$; Unipolar Configuration; $R_{CLK} = 150k\Omega$; $C_{CLK} = 100pF$; unless otherwise specified.

Subgroup	Symbol	Special Conditions	PM-7574/883				Units	
			LIMITS A		LIMITS B			
			Min	Max	Min	Max		
Subgroup 1	INL	(Note 1)	--	$\pm 1/2$	--	$\pm 3/4$	LSB	
$T_A = +25^\circ C$	DNL	(Note 1)	--	$\pm 3/4$	--	$\pm 7/8$	LSB	
	AE	(Note 2)	--	± 3	--	± 5	LSB	
	V_{OS}		--	± 30	--	± 60	mV	
	ΔR_{AB}		--	± 1.5	--	± 1.5	%	
	R_{IN}	@ V_{REF} (Pin 2)		5	15	5	15	$k\Omega$
		@ B_{OFS} (Pin 3)		10	30	10	30	$k\Omega$
		@ A_{IN} (Pin 4)		10	30	10	30	$k\Omega$
	V_{IH}	\overline{RD} (Pin 15), \overline{CS} (Pin 16)(Note 3)		2.4	--	2.4	--	V
	V_{IL}	\overline{RD} (Pin 15), \overline{CS} (Pin 16)(Note 3)		--	0.8	--	0.8	V
	I_{IN}	$V_{IN} = 0V$ or V_{DD} , \overline{RD} (Pin 15) \overline{CS} (Pin 16)		--	± 1	--	± 1	μA
	V_{IH}	Clock (Pin 17)(Note 3)		3.0	--	3.0	--	V
	V_{IL}	Clock (Pin 17)(Note 3)		--	0.4	--	0.4	V
	I_{IH}	Clock (Pin 17), $V_{IN} = V_{DD}$		--	± 2	--	± 2	mA
	I_{IL}	Clock (Pin 17), $V_{IN} = 0V$		--	± 1	--	± 1	μA
	V_{OH}	$I_{SOURCE} = 40\mu A$		4	--	4	--	V
	V_{OL}	$I_{SINK} = 1.6mA$		--	0.4	--	0.4	V
I_{LKG}	$V_O = 0V$ or V_{DD}		--	± 1	--	± 1	μA	
I_{DD}	$A_{IN} = 0V$, \overline{BUSY} and \overline{RD} High		--	5	--	5	mA	



TABLE 3

Group A Inspection

$V_{DD} = +5V$; $V_{REF} = -10V$; $AGND = DGND = 0V$; Unipolar Configuration; $R_{CLK} = 150k\Omega$; $C_{CLK} = 100pF$;
unless otherwise specified.

Subgroup	Symbol	Special Conditions	PM-7574/883				Units	
			LIMITS A		LIMITS B			
			Min	Max	Min	Max		
Subgroup 2	INL	(Note 1)	–	±1/2	–	±3/4	LSB	
	DNL	(Note 1)	–	±3/4	–	±7/8	LSB	
$T_A = +125^\circ C$	AE	(Note 2)	–	±4.5	–	±6.5	LSB	
	V_{OS}		–	±50	–	±80	mV	
	ΔR_{AB}		–	±1.5	–	±1.5	%	
	R_{IN}	@ V_{REF} (Pin 2)		5	15	5	15	k Ω
		@ B_{OFS} (Pin 3)		10	30	10	30	k Ω
		@ A_{IN} (Pin 4)		10	30	10	30	k Ω
	V_{IH}	\overline{RD} (Pin 15), \overline{CS} (Pin 16)(Note 3)		2.4	–	2.4	–	V
	V_{IL}	\overline{RD} (Pin 15), \overline{CS} (Pin 16)(Note 3)		–	0.8	–	0.8	V
	I_{IN}	$V_{IN} = 0V$ or V_{DD} , \overline{RD} (Pin 15) \overline{CS} (Pin 16)		–	±10	–	±10	μA
	V_{IH}	Clock (Pin 17)(Note 3)		3.0	–	3.0	–	V
	V_{IL}	Clock (Pin 17)(Note 3)		–	0.4	–	0.4	V
	I_{IH}	Clock (Pin 17), $V_{IN} = V_{DD}$		–	±2	–	±2	mA
	I_{IL}	Clock (Pin 17), $V_{IN} = 0V$		–	±10	–	±10	μA
	V_{OH}	$I_{SOURCE} = 40\mu A$		4	–	4	–	V
	V_{OL}	$I_{SINK} = 1.6mA$		–	0.4	–	0.4	V
I_{LKG}	$V_O = 0V$ or V_{DD}		–	±10	–	±10	μA	
I_{DD}	$A_{IN} = 0V$, \overline{BUSY} and \overline{RD} High		–	5	–	5	mA	

ANALOG-TO-DIGITAL CONVERTERS



TABLE 3

Group A Inspection

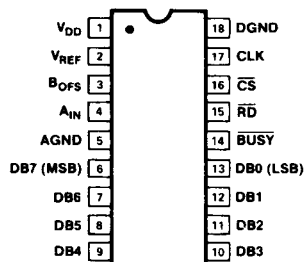
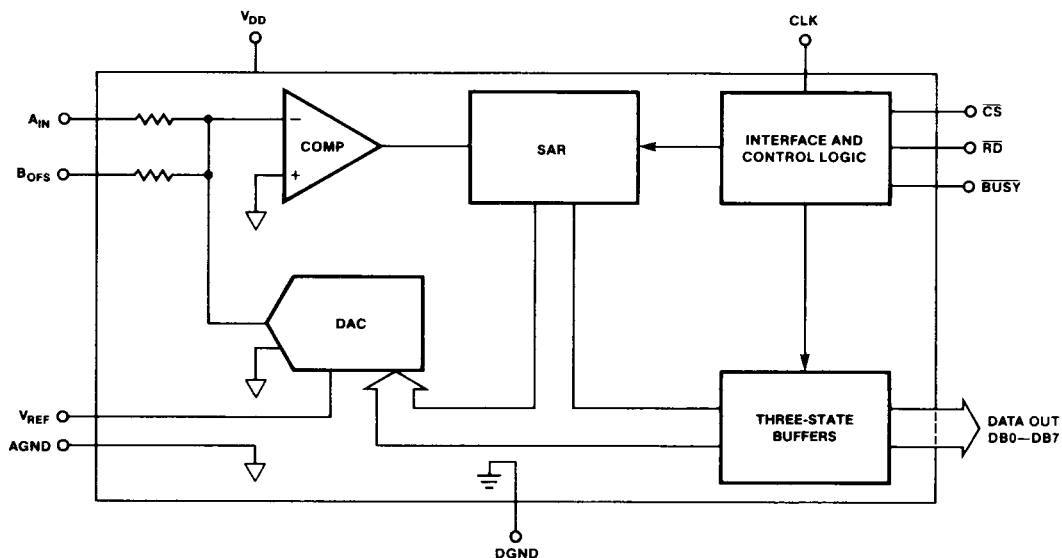
$V_{DD} = +5V$; $V_{REF} = -10V$; $AGND = DGND = 0V$; Unipolar Configuration; $R_{CLK} = 150k\Omega$; $C_{CLK} = 100pF$;
unless otherwise specified.

Subgroup	Symbol	Special Conditions	PM-7574/883				Units
			LIMITS A		LIMITS B		
			Min	Max	Min	Max	
Subgroup 3		All Tests, Limits and Conditions are the same as for Subgroup 2.					
	$T_A = -55^\circ C$						

NOTES:

1. Measured using external clock frequency of 550kHz.
2. Gain Error is measured after calibrating out offset error.
3. Guaranteed by functional pattern testing in external clock RAM, ROM and SLOW modes.

3.2.1 Functional Diagram and Pin Connections.



18-PIN CERDIP
(X-Suffix)



3.2.4 Microcircuit Group Assignment. This microcircuit is covered by microcircuit group 81.

4.2 Life Test/Burn-In Circuit.

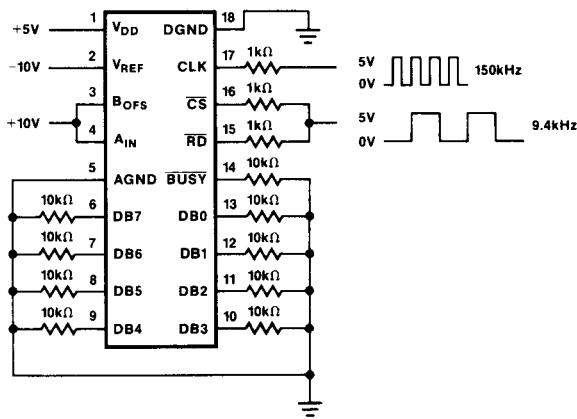


Figure 1: ROM Mode Timing Diagram (\overline{CS} Held LOW)

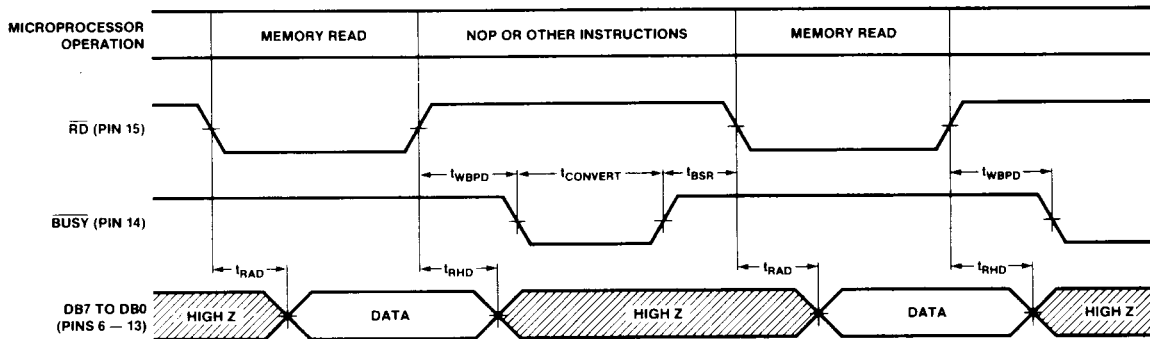


Table 1: Truth Table, ROM Mode

INPUTS		OUTPUTS		PM-7574 OPERATION
\overline{CS}	\overline{RD}	\overline{BUSY}	DB7-DB0	
L		H	HIGH-Z to DATA	Read Data
L			DATA to HIGH-Z	Reset and Start New Conversion
L		L	HIGH-Z	No Effect (Converter Busy)
L		L	HIGH-Z	Conversion Error Not Allowed

NOTE 1: If \overline{RD} goes LOW to HIGH, the ADC is internally reset, regardless of the states of \overline{CS} or \overline{BUSY} .



Figure 2: Static RAM Mode Timing Diagram

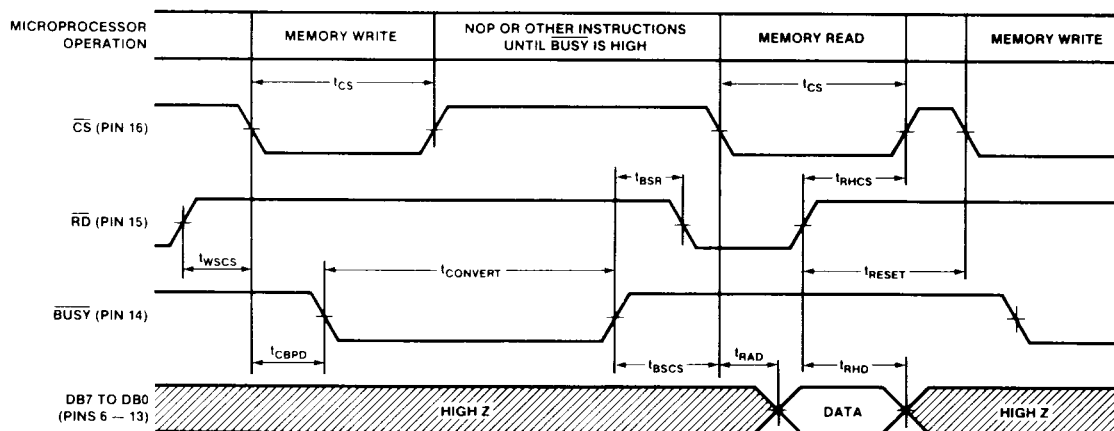


Table 2: Truth Table, Static RAM Mode

INPUTS		OUTPUTS		PM-7574 OPERATION
CS	RD	BUSY	DB7-DB0	
\downarrow	H	\downarrow	HIGH-Z	Start Convert (Write Cycle)
L	\downarrow	H	HIGH-Z to DATA	Read Data (Read Cycle)
L	\uparrow	H	DATA to HIGH-Z	Reset Converter
H	X (Note 1)	X	HIGH-Z	No Effect (Not Selected)
L	H	L	HIGH-Z	No Effect (Converter Busy)
L	\downarrow	L	HIGH-Z	No Effect (Converter Busy)
L	\uparrow (Note 1)	L	HIGH-Z	Conversion Error Not Allowed

NOTE 1: if RD goes LOW to HIGH, the ADC is internally reset, regardless of the states of CS or BUSY



Figure 3: Slow Memory Mode Timing Diagram (\overline{CS} and \overline{RD} Tied Together)

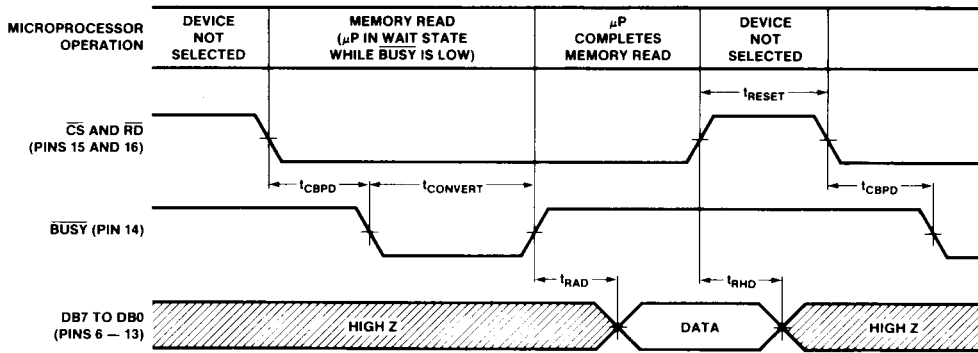


Table 3: Truth Table, Slow Memory Mode

INPUTS \overline{CS} & \overline{RD}	OUTPUTS		PM-7574 OPERATION
	BUSY	DB7-DB0	
H	H	HIGH-Z	No Effect (Not Selected)
\downarrow	\downarrow	HIGH-Z	Start Conversion
L	L	HIGH-Z	Conversion in Progress. μP in WAIT State
L	\uparrow	HIGH-Z to DATA	Conversion Complete. Read Data
\uparrow (Note 1)	H	DATA to HIGH-Z	Reset and Deselect Converter

NOTE 1: If \overline{RD} goes LOW to HIGH, the ADC is internally reset, regardless of the states of \overline{CS} or \overline{BUSY} .