NEC

MOS INTEGRATED CIRCUIT

μPD42S4210A, 424210A

4 M-BIT DYNAMIC RAM
256 K-WORD BY 16-BIT, HYPER PAGE MODE, BYTE READ/WRITE MODE

Description

The μPD42S4210A, 424210A are 262 144 words by 16 bits dynamic CMOS RAMs with optional hyper page mode.

Hyper page mode is a kind of the page mode and is useful for the read operation.

The μPD42S4210A, 424210A are packed in 44-pin plastic TSOP(II) and 40-pin plastic SOJ.

Features

- Hyper page mode
- 262 144 words by 16 bits organization
- Single +5.0 V ± 10 % power supply

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD42S4210A-50, 424210A-50	50 ns	84 ns	20 ns
μPD42S4210A-60, 424210A-60	60 ns	104 ns	25 ns
μPD42S4210A-70, 424210A-70	70 ns	124 ns	30 ns

- The μPD42S4210A can execute $\overline{CAS}$ before $\overline{RAS}$ self refresh

Part number	Refresh cycle	Refresh
μPD42S4210A	512 cycles / 128 ms	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424210A	512 cycles / 8 ms	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh

Ordering Information

Part number	Access time (MAX.)	Package	Refresh
μPD42S4210AG5-50	50 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ self refresh $\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD42S4210AG5-60	60 ns		
μPD42S4210AG5-70	70 ns		
μPD42S4210AG5-50-7KF	50 ns	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD42S4210AG5-60-7KF	60 ns		
μPD42S4210AG5-70-7KF	70 ns		
μPD42S4210ALE-50	50 ns	40-pin Plastic SOJ (400 mil)	
μPD42S4210ALE-60	60 ns		
μPD42S4210ALE-70	70 ns		
μPD424210AG5-50	50 ns	44-pin Plastic TSOP (II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD424210AG5-60	60 ns		
μPD424210AG5-70	70 ns		
μPD424210AG5-50-7KF	50 ns	44-pin Plastic TSOP (II) (400 mil) Reverse bent	
μPD424210AG5-60-7KF	60 ns		
μPD424210AG5-70-7KF	70 ns		
μPD424210ALE-50	50 ns	40-pin Plastic SOJ (400 mil)	
μPD424210ALE-60	60 ns		
μPD424210ALE-70	70 ns		

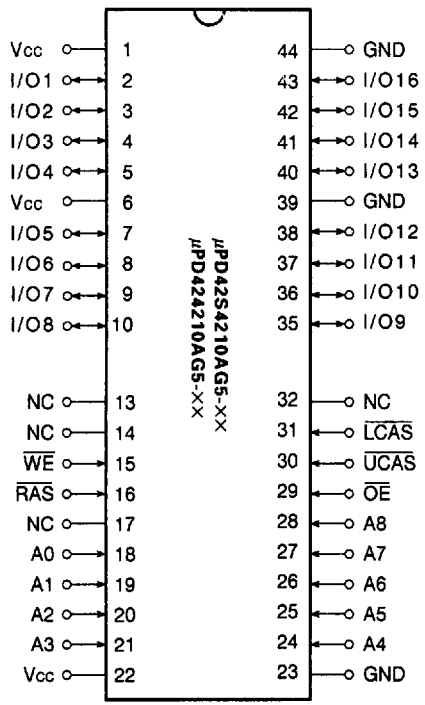
Quality Grade

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

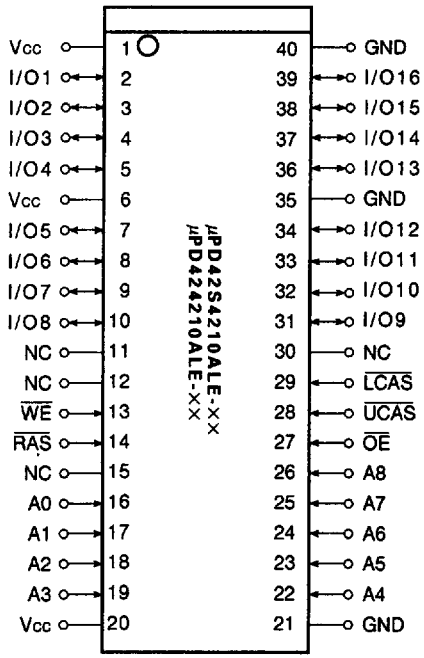
Pin Configurations (Marking Side)

44-pin Plastic TSOP (II)
(400 mil)



A0 to A8	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
$\overline{LCAS}$	: Column Address Strobe (lower)
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
Vcc	: Power Supply
GND	: Ground
NC	: No Connection

40-pin Plastic SOJ
(400 mil)



A0 to A8	: Address Inputs
I/O1 to I/O16	: Data Inputs/Outputs
$\overline{RAS}$	: Row Address Strobe
$\overline{UCAS}$	: Column Address Strobe (upper)
$\overline{LCAS}$	: Column Address Strobe (lower)
$\overline{WE}$	: Write Enable
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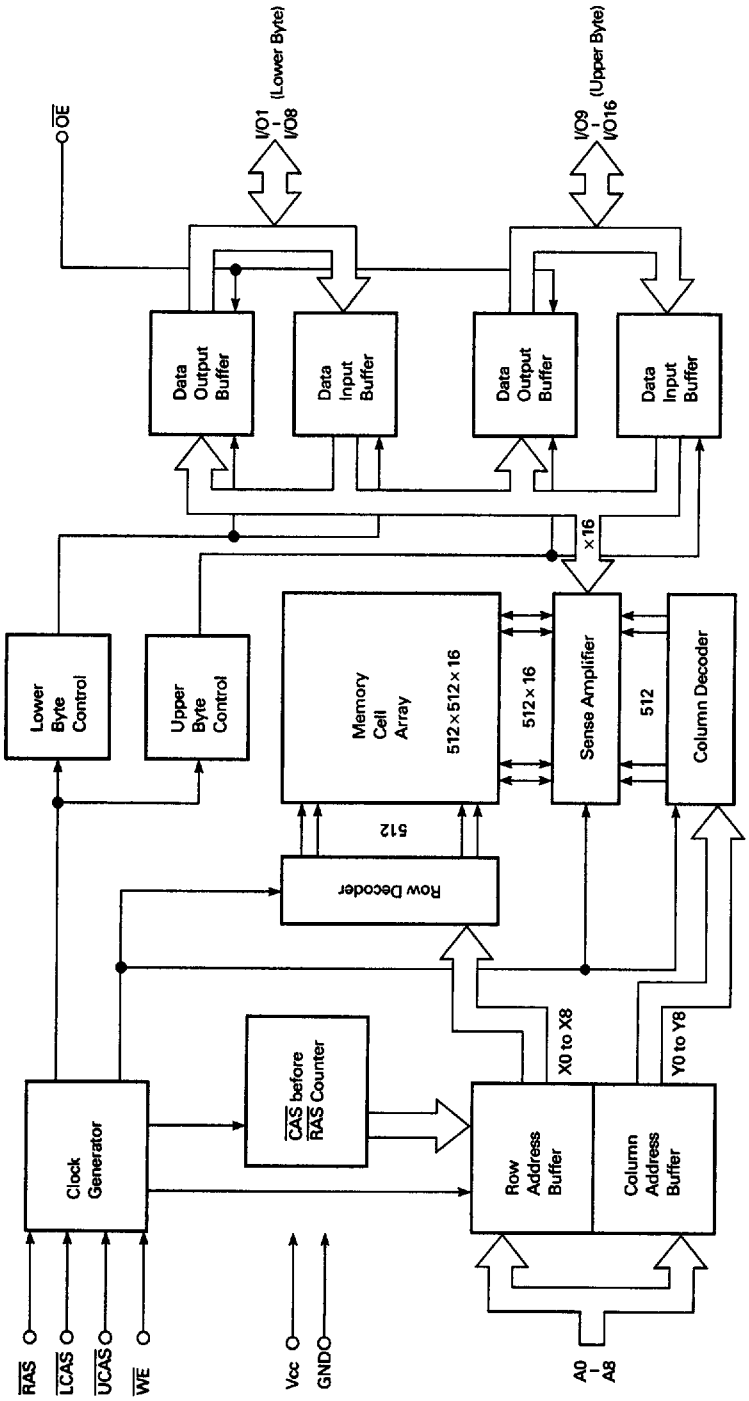
Vcc	: Power Supply
GND	: Ground
NC	: No Connection

Block Diagram



Input/Output Pin Functions

The μPD42S4210A, 424210A have input pins $\overline{RAS}$, $\overline{CAS}$ [Note], $\overline{WE}$, $\overline{OE}$, A0 to A8 and input/output pins I/O1 to I/O16.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)	Input	$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A8 (Address inputs)	Input	9-bit address bus. Input total 18-bit of address signal, upper 9-bit and lower 9-bit in sequence (address multiplex method). Therefore, one word is selected from 262 144-word by 16-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)	Input	Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)	Input	Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O16 (Data inputs/outputs)	Input/ Output	16-bit data bus. I/O1 to I/O16 are used to input/output data.

Note $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is larger than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

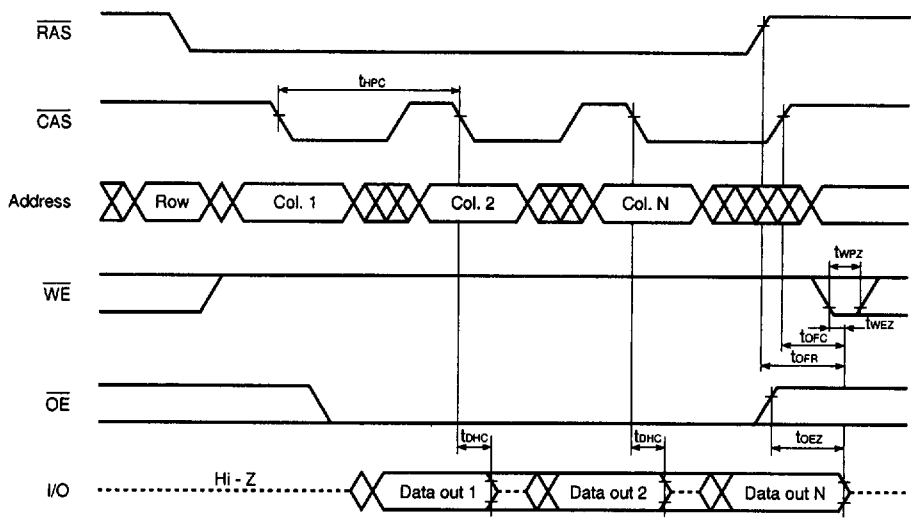
2. The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.

In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.

Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the hyper page mode is 25 ns while that in the fast page mode is 40 ns.

In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

Hyper Page Mode Read Cycle



To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)
$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
$\overline{WE}$: active, $\overline{OE}$: active··· t_{WEZ}, t_{WPZ} are effective.
$\overline{WE}$: inactive, $\overline{OE}$: inactive··· t_{OEZ} is effective.

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−1.0 to +7.0	V
Supply Voltage	V_{CC}		−1.0 to +7.0	V
Output Current	I_O		50	mA
Power Dissipation	P_D		1	W
Operating Temperature	T_{opt}		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low Level Input Voltage	V_{IL}		−1.0		+0.8	V
Ambient Temperature	T_a		0		70	°C

Capacitance (T_a = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Test Condition		MIN.	TYP.	MAX.	Unit	Notes
Operating current		I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 50 ns			90	mA	1, 2, 3
				t_{RAC} = 60 ns			80		
				t_{RAC} = 70 ns			70		
Standby current	μPD42S4210A	I_{CC2}	$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA				2	mA	
			$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA				0.15		
	μPD424210A		$\overline{RAS}$, $\overline{CAS} \geqq V_{IH(MIN.)}$, I_O = 0 mA				2		
			$\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$ – 0.2 V, I_O = 0 mA				1		
$\overline{RAS}$ only refresh current		I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geqq V_{IH(MIN.)}$ $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns			90	mA	1,2,3,4
				t_{RAC} = 60 ns			80		
				t_{RAC} = 70 ns			70		
Operating current (Hyper page mode)		I_{CC4}	$\overline{RAS} \leqq V_{IL(MAX.)}$, $\overline{CAS}$ Cycling $t_{HPC} = t_{HPC(MIN.)}$, I_O = 0 mA	t_{RAC} = 50 ns			90	mA	1, 2, 5
				t_{RAC} = 60 ns			80		
				t_{RAC} = 70 ns			70		
$\overline{CAS}$ before $\overline{RAS}$ refresh current		I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 50 ns			90	mA	1, 2
				t_{RAC} = 60 ns			80		
				t_{RAC} = 70 ns			70		
$\overline{CAS}$ before $\overline{RAS}$ long refresh current (512 Cycles / 128 ms, only for the μPD42S4210A)		I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ refresh : 512 Cycles / 128 ms $\overline{RAS}$, $\overline{CAS}$: V_{CC}–0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ 0 V $\leqq V_{IL} \leqq$ 0.2 V	$t_{RAS} \leqq$ 200 ns			200	μA	1, 2
			Standby : $\overline{RAS}$, $\overline{CAS} \geqq V_{CC}$–0.2 V Address : V_{IH} or V_{IL} $\overline{WE}$, $\overline{OE}$: V_{IH} I_O = 0 mA	$t_{RAS} \leqq$ 1 μs			300		
Self refresh current ($\overline{CAS}$ before $\overline{RAS}$ self refresh, only for the μPD42S4210A)		I_{CC7}	$\overline{RAS}$, $\overline{CAS}$: V_{CC} – 0.2 V $\leqq V_{IH} \leqq V_{IH(MAX.)}$ 0 V $\leqq V_{IL} \leqq$ 0.2 V I_O = 0 mA				150	μA	2
Input leakage current		$I_{I(L)}$	V_I = 0 to 5.5 V All other pins not under test = 0 V		–10		+10	μA	
Output leakage current		$I_{O(L)}$	V_O = 0 to 5.5 V Output is disabled (Hi-Z)		–10		+10	μA	
High level output voltage		V_{OH}	I_O = –2.5 mA		2.4			V	
Low level output voltage		V_{OL}	I_O = +2.1 mA				0.4	V	

Notes 1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{HPC}).

2. Specified values are obtained with outputs unloaded.

3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leqq V_{IL(MAX.)}$ and $\overline{CAS} \geqq V_{IH(MIN.)}$.

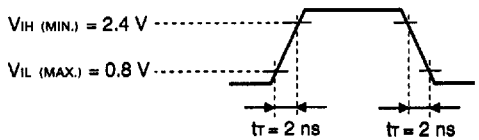
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.

5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

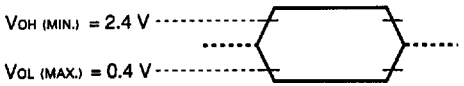
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter		Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time		tRC	84	–	104	–	124	–	ns	
$\overline{RAS}$ Precharge Time		tRP	30	–	40	–	50	–	ns	
$\overline{CAS}$ Precharge Time		tCPN	7	–	10	–	10	–	ns	
$\overline{RAS}$ Pulse Width		tRAS	50	10 000	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width		tCAS	7	10 000	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time		tRSH	7	–	10	–	12	–	ns	
$\overline{CAS}$ Hold Time		tCSH	35	–	40	–	50	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time		tRCD	11	37	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time		tRAD	9	25	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		tCRP	5	–	5	–	5	–	ns	2
Row Address Setup Time		tASR	0	–	0	–	0	–	ns	
Row Address Hold Time		tRAH	7	–	10	–	10	–	ns	
Column Address Setup Time		tASC	0	–	0	–	0	–	ns	
Column Address Hold Time		tCAH	7	–	10	–	12	–	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$		tOES	0	–	0	–	0	–	ns	
$\overline{CAS}$ to Data Setup Time		tCLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to Data Setup Time		tOLZ	0	–	0	–	0	–	ns	
$\overline{OE}$ to Data Delay Time		tOED	10	–	13	–	15	–	ns	
Masked Byte Write Hold Time Referenced to $\overline{RAS}$		tMRH	0	–	0	–	0	–	ns	
Transition Time (Rise and Fall)		tT	1	50	1	50	1	50	ns	
Refresh Time	μPD42S4210A	tREF	–	128	–	128	–	128	ms	3
	μPD424210A		–	8	–	8	–	8	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX)}$	$t_{RAC\,(MAX)}$	$t_{RAC\,(MAX)}$
$t_{RAD} > t_{RAD\,(MAX)}$ and $t_{RCD} \leqq t_{RCD\,(MAX)}$	$t_{AA\,(MAX)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX.)}$	$t_{CAC\,(MAX)}$	$t_{RCD} + t_{CAC\,(MAX.)}$

$t_{RAD(MAX)}$ and $t_{RCD(MAX)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX)}$ and $t_{RCD} \geqq t_{RCD(MAX)}$ will not cause any operation problems.

2. $t_{CRP(MIN)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.
3. This specification is applied only to the μPD42S4210A.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	18	ns	1
Access Time from Column Address	t_{AA}	–	25	–	30	–	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	–	13	–	15	–	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25	–	30	–	35	–	ns	
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\,(MAX)}$ and $t_{RCD} \leqq t_{RCD\,(MAX)}$	$t_{RAC\,(MAX)}$	$t_{RAC\,(MAX.)}$
$t_{RAD} > t_{RAD\,(MAX.)}$ and $t_{RCD} \leqq t_{RCD\,(MAX)}$	$t_{AA\,(MAX.)}$	$t_{RAD} + t_{AA\,(MAX.)}$
$t_{RCD} > t_{RCD\,(MAX)}$	$t_{CAC\,(MAX.)}$	$t_{RCD} + t_{CAC\,(MAX)}$

$t_{RAD(MAX)}$ and $t_{RCD(MAX)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX)}$ and $t_{RCD} \geqq t_{RCD(MAX)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	7	–	10	–	10	–	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	7	–	10	–	10	–	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	7	–	10	–	12	–	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	7	–	10	–	12	–	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	–	0	–	0	–	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	–	0	–	0	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	3
Data-in Hold Time	t_{DH}	7	–	10	–	10	–	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	107	–	133	–	157	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	64	–	77	–	89	–	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27	–	32	–	37	–	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	39	–	47	–	54	–	ns	1

Note 1. If $t_{WCS} \geq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Pulse Width	t_{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7	–	10	–	10	–	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	–	27	–	35	–	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	41	–	52	–	59	–	ns	1
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	27	–	35	–	40	–	ns	
Read Modify Write Cycle Time	t_{HPRWC}	52	–	66	–	75	–	ns	
Data Output Hold Time	t_{DHC}	5	–	5	–	5	–	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	2,3
$\overline{WE}$ Pulse Width	t_{WPZ}	7	–	10	–	10	–	ns	3
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	2,3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	2,3

Notes 1. If $t_{WCS} \geq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{CWD} \geq t_{CWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$, and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

2. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

3. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

(1) $\overline{RAS}$, $\overline{CAS}$: inactive (at the end of read cycle)

$\overline{WE}$: inactive, $\overline{OE}$: active
t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

(2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)

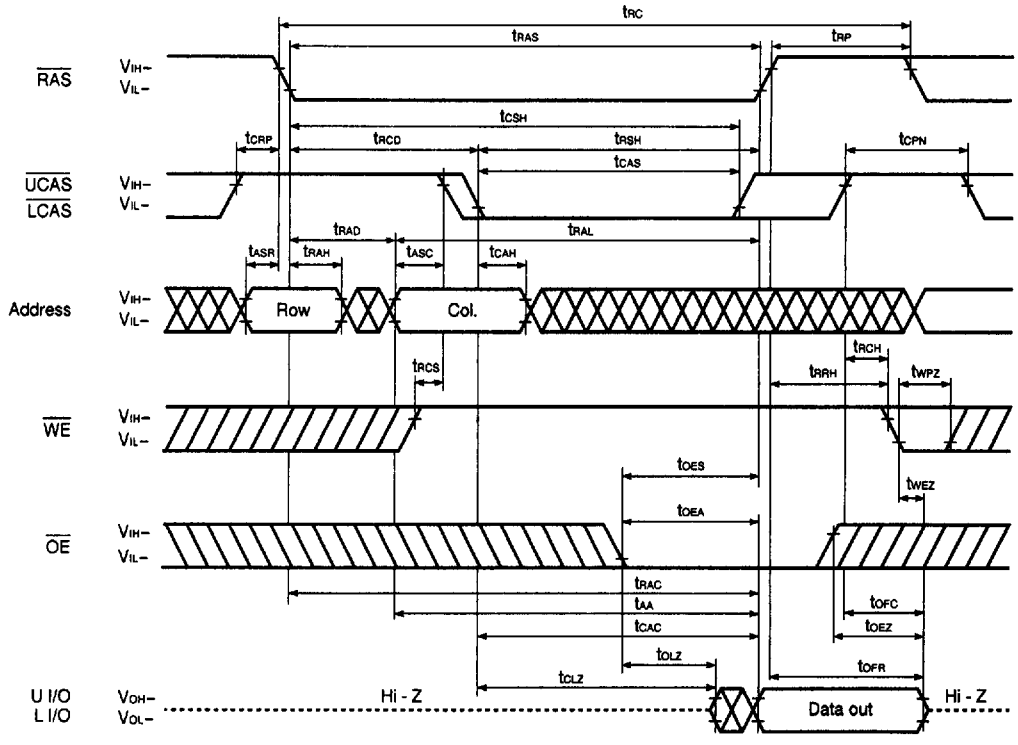
$\overline{WE}$: active, $\overline{OE}$: active ··· t_{WEZ}, t_{WPZ} are effective
$\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.

Refresh Cycle

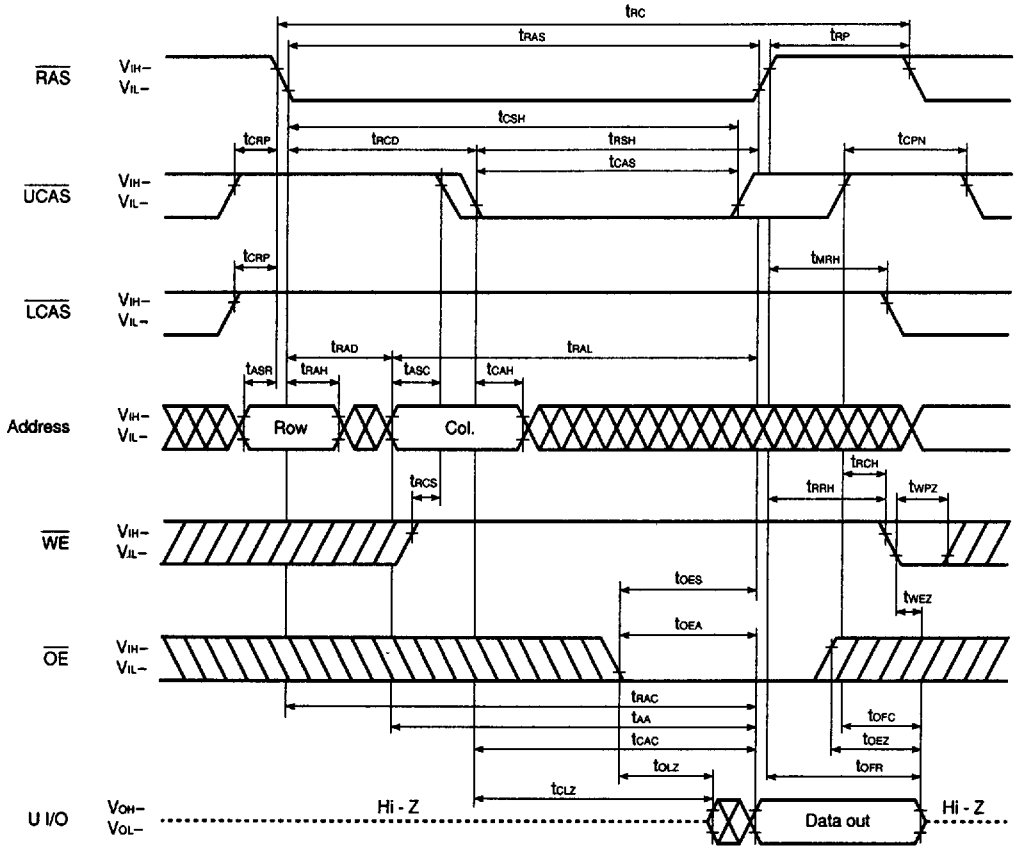
Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ Pulse Width ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	t_{RASS}	100	–	100	–	100	–	μs	1
$\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	t_{RPS}	90	–	110	–	130	–	ns	1
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Self Refresh Cycle)	t_{CHS}	−50	–	−50	–	−50	–	ns	1
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	–	15	–	15	–	ns	

Note 1. This specification is applied only to the μPD42S4210A.

Read Cycle

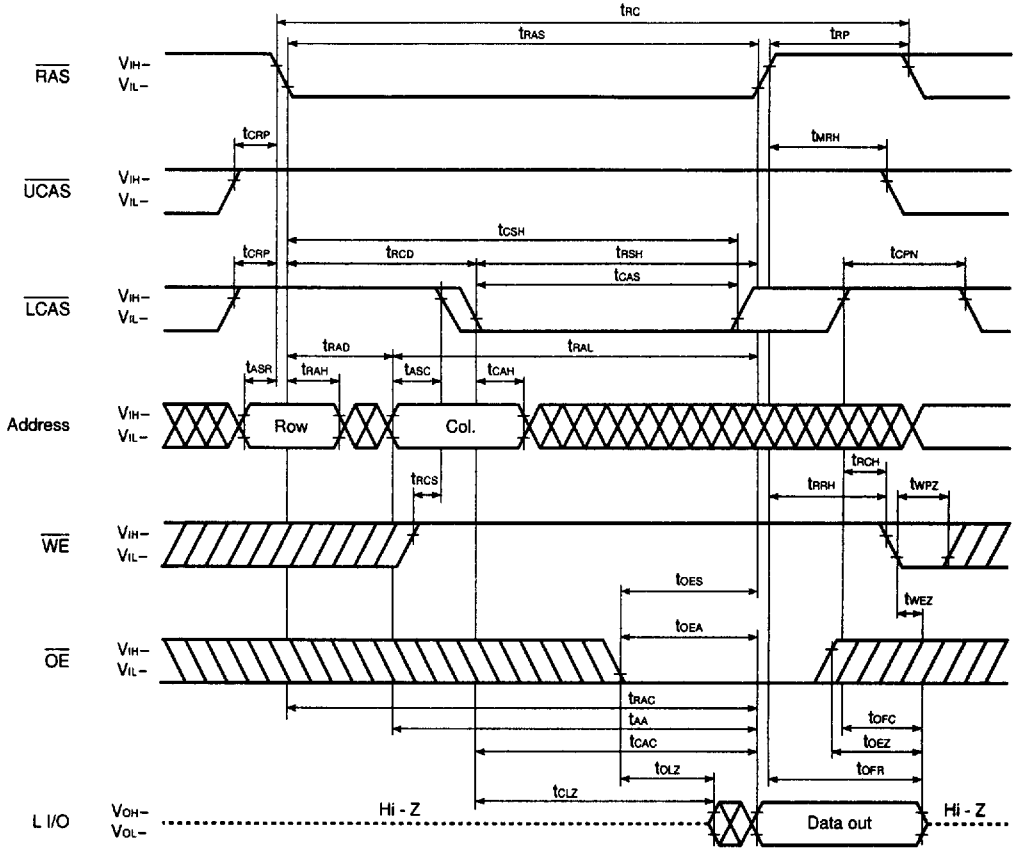


Upper Byte Read Cycle



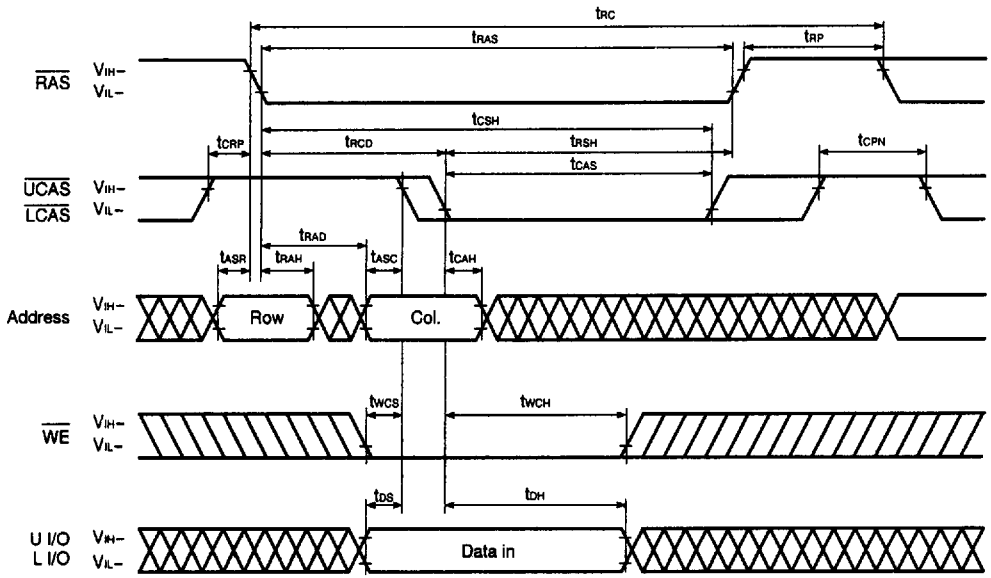
Remark L I/O : Hi-Z

Lower Byte Read Cycle



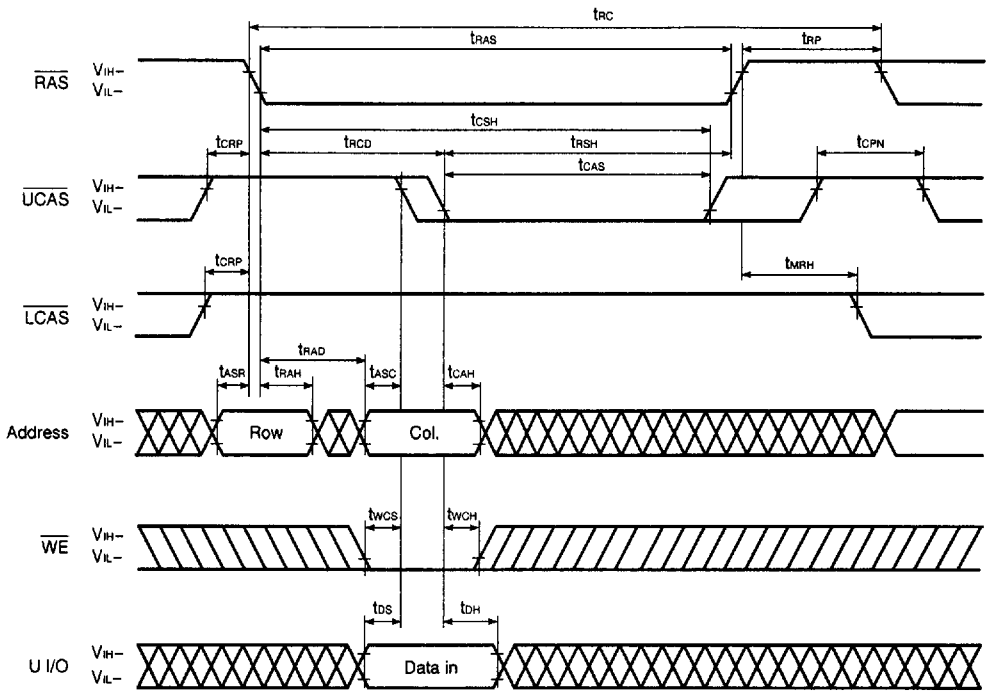
Remark U I/O : Hi-Z

Early Write Cycle



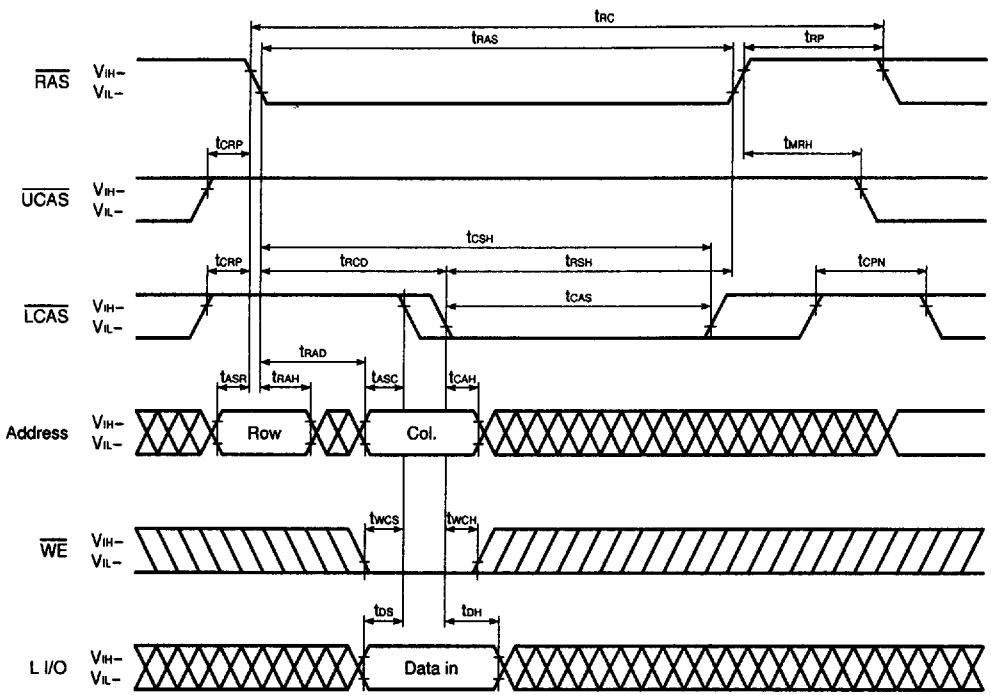
Remark $\overline{OE}$: Don't care

Upper Byte Early Write Cycle



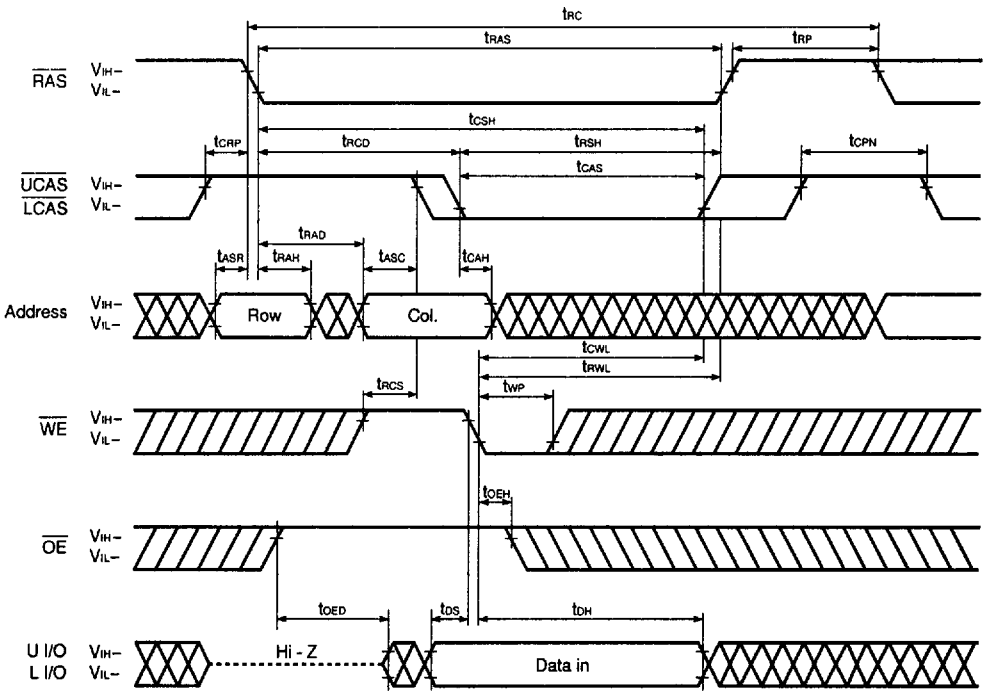
Remark $\overline{OE}$, L I/O : Don't care

Lower Byte Early Write Cycle

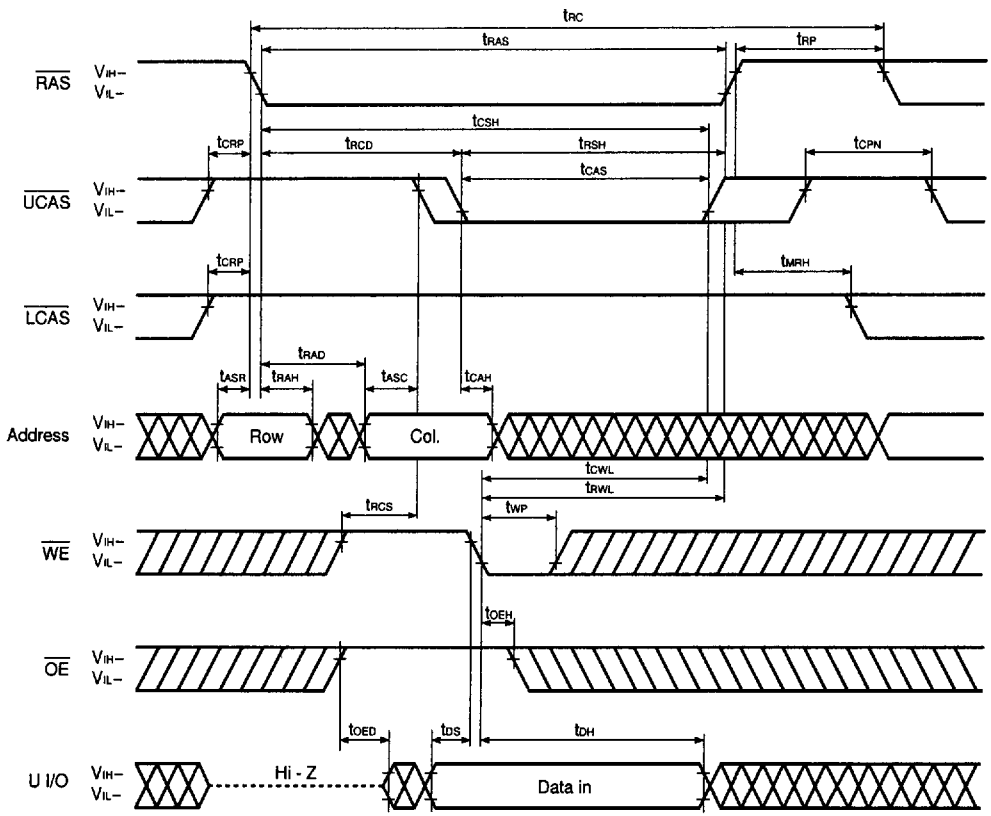


Remark $\overline{OE}$, U I/O : Don't care

Late Write Cycle

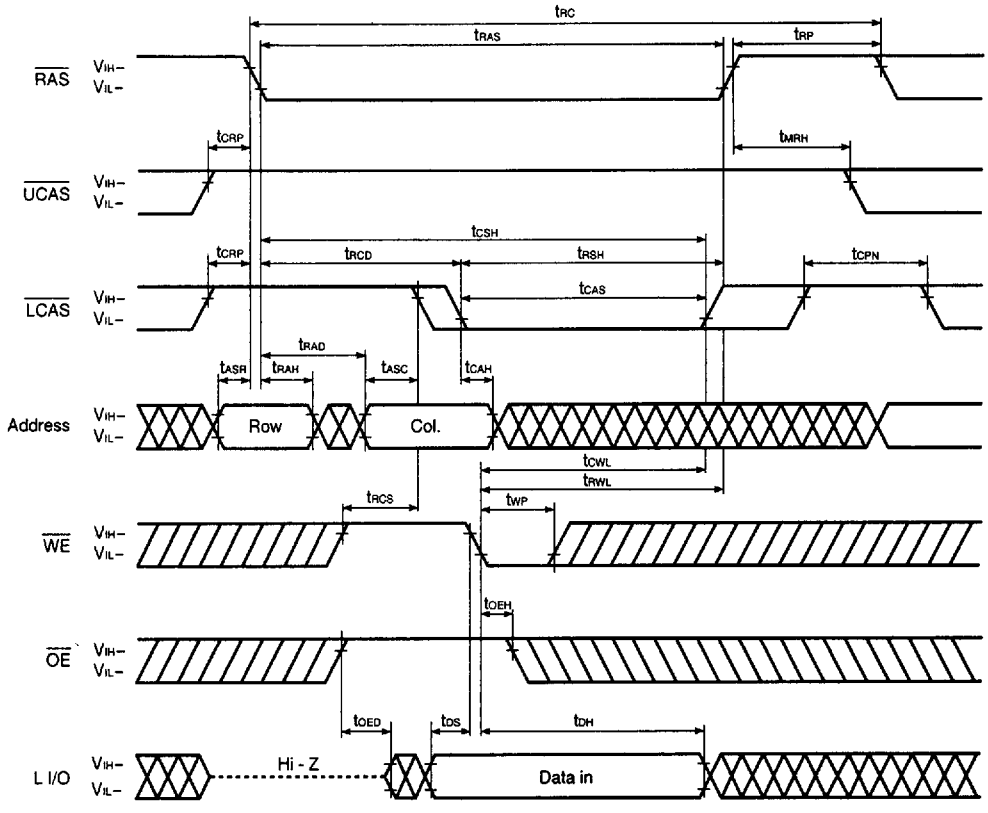


Upper Byte Late Write Cycle



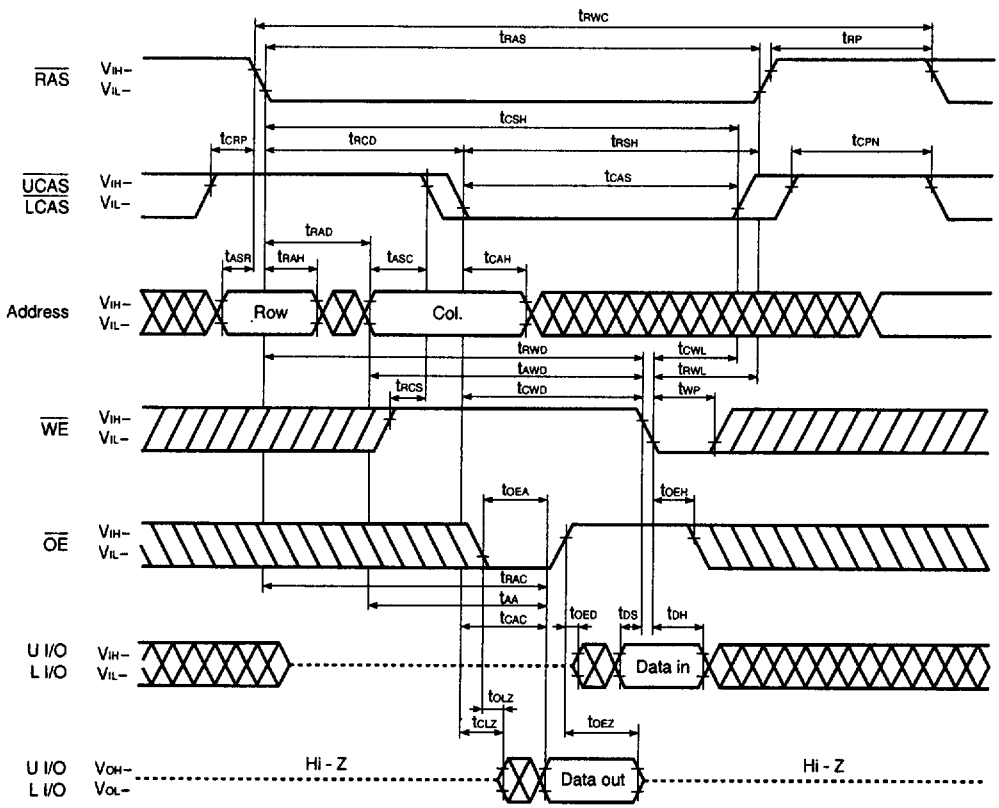
Remark L I/O : Don't care

Lower Byte Late Write Cycle

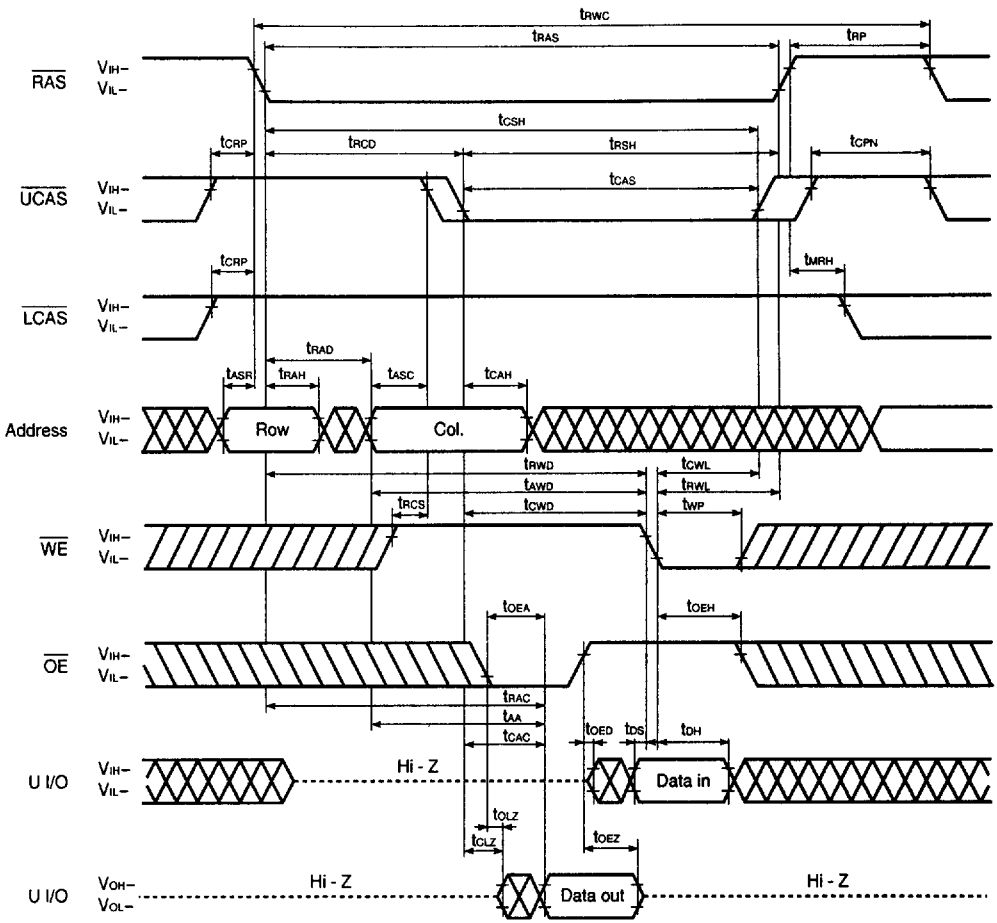


Remark U I/O : Don't care

Read Modify Write Cycle

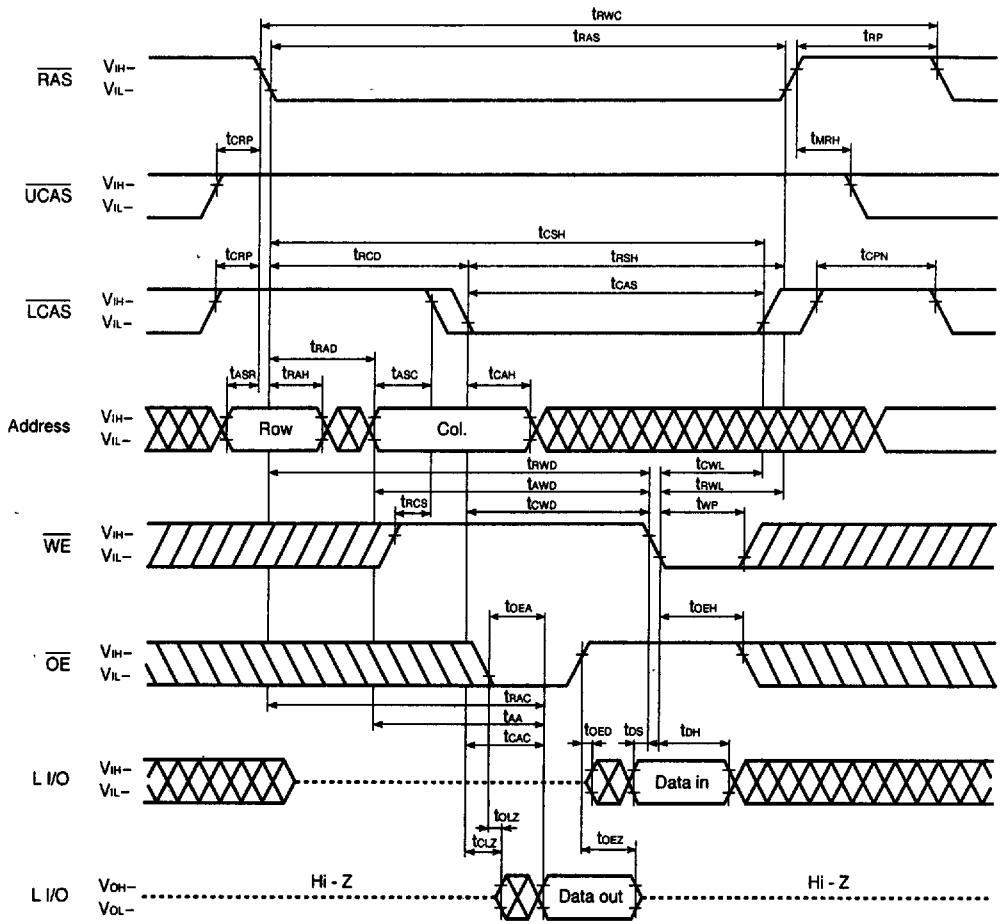


Upper Byte Read Modify Write Cycle



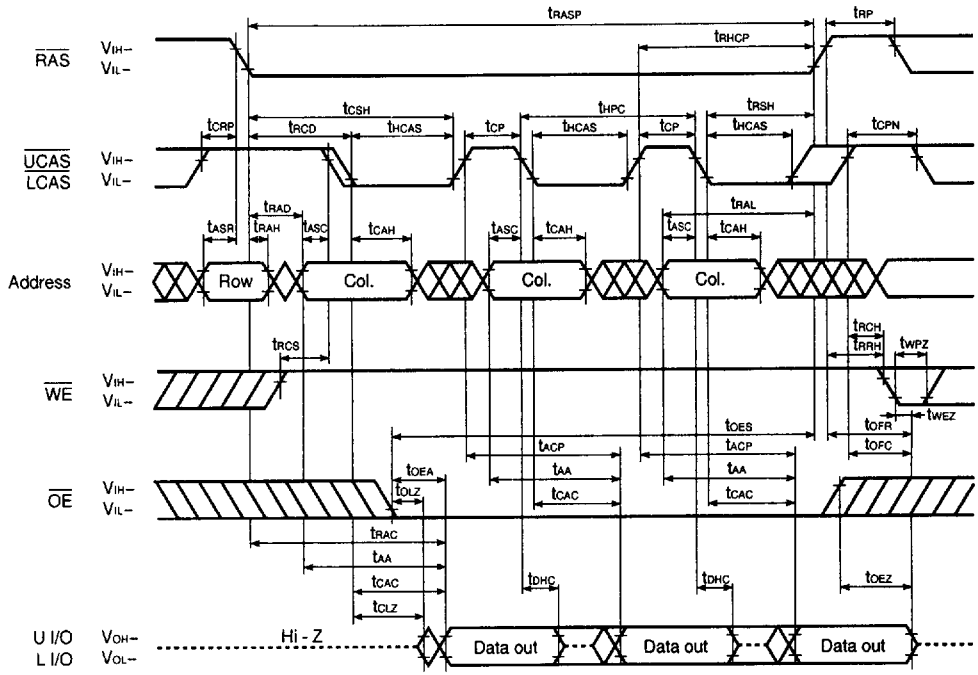
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Lower Byte Read Modify Write Cycle

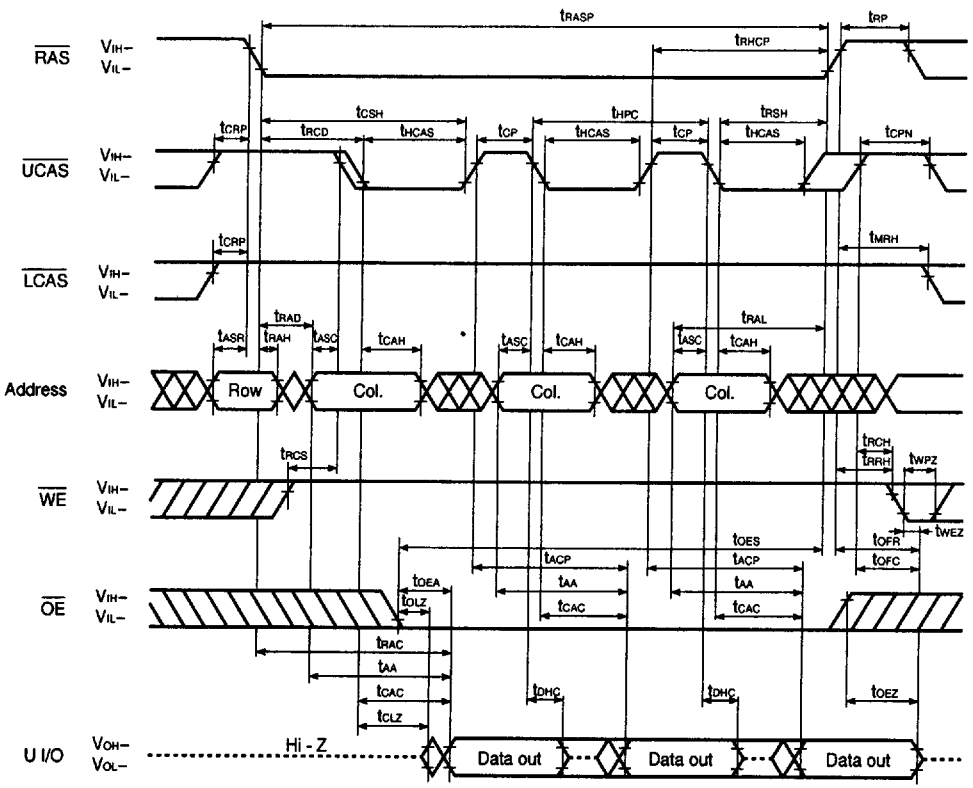


Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode Read Cycle

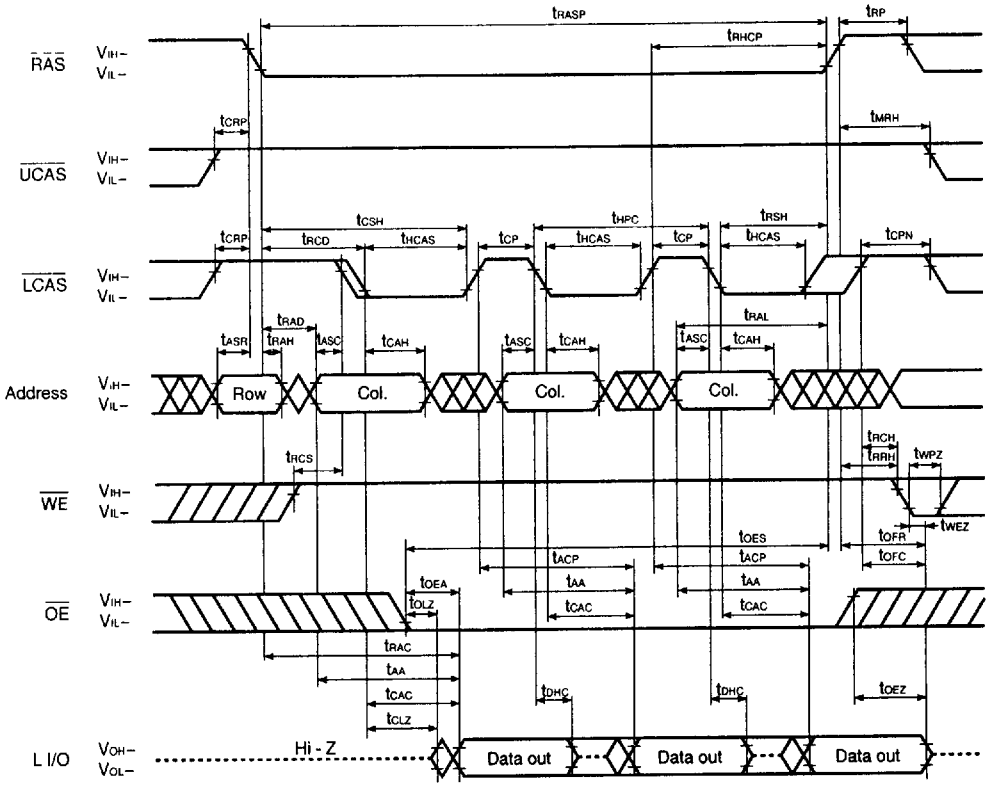


Hyper Page Mode Upper Byte Read Cycle



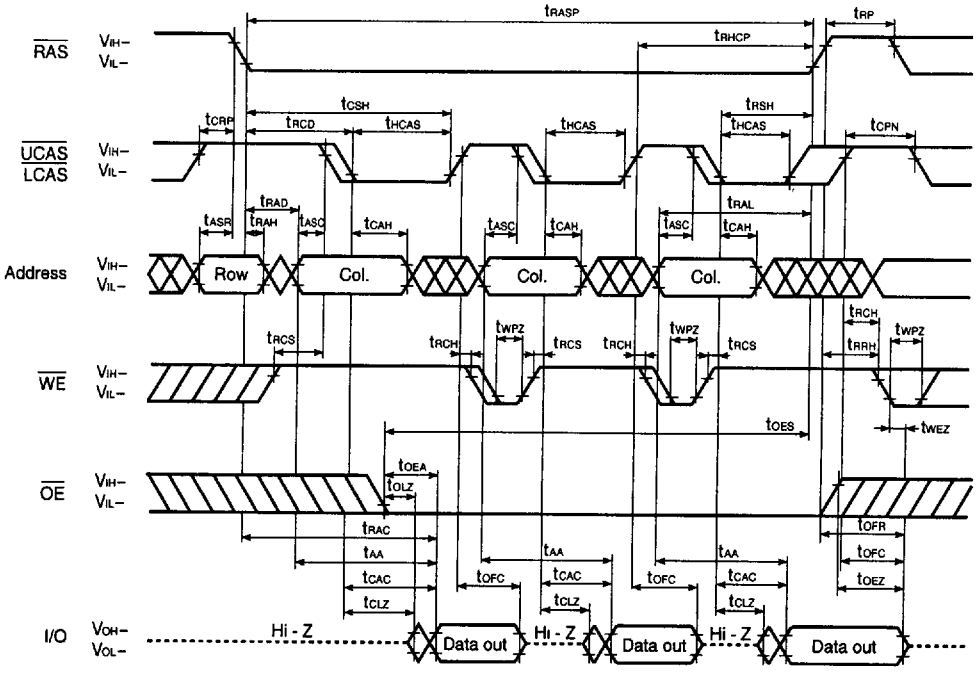
Remark L I/O : Hi-Z

Hyper Page Mode Lower Byte Read Cycle

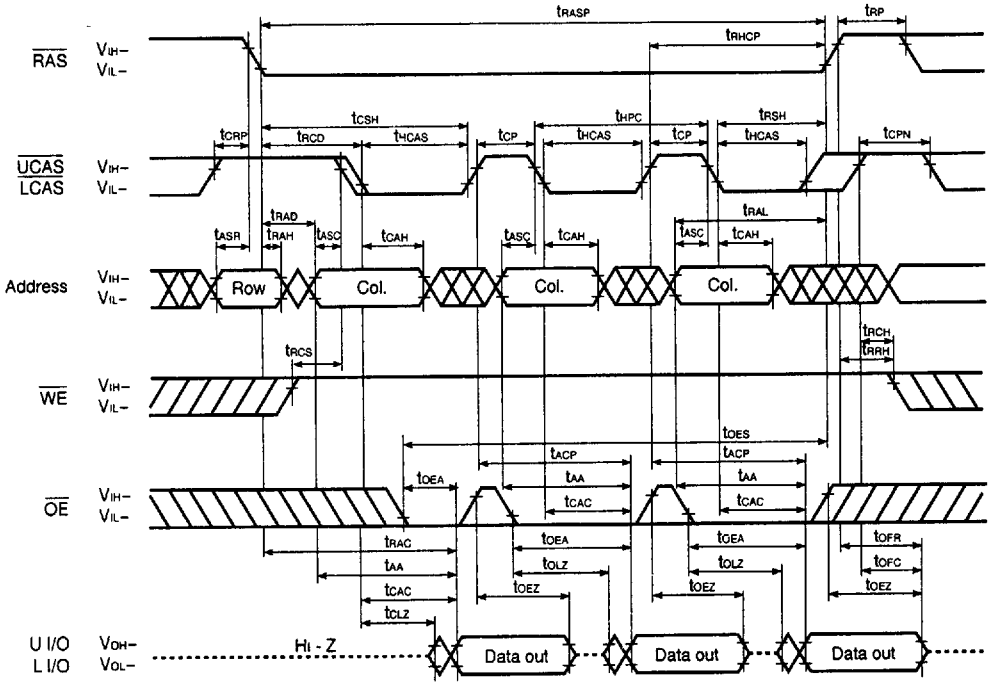


Remark U I/O : Hi-Z

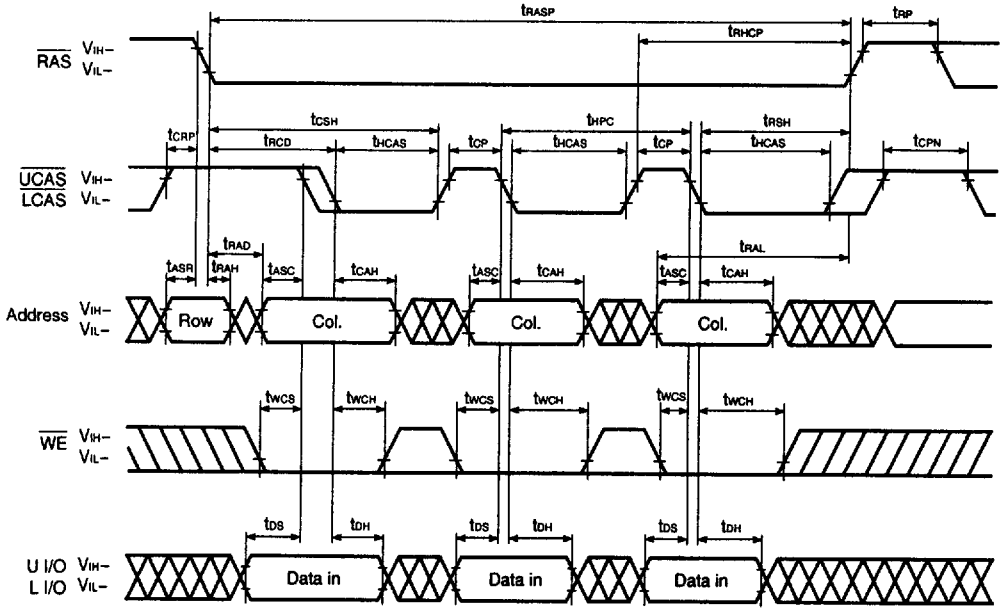
Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



Hyper Page Mode Read Cycle ($\overline{OE}$ Control)

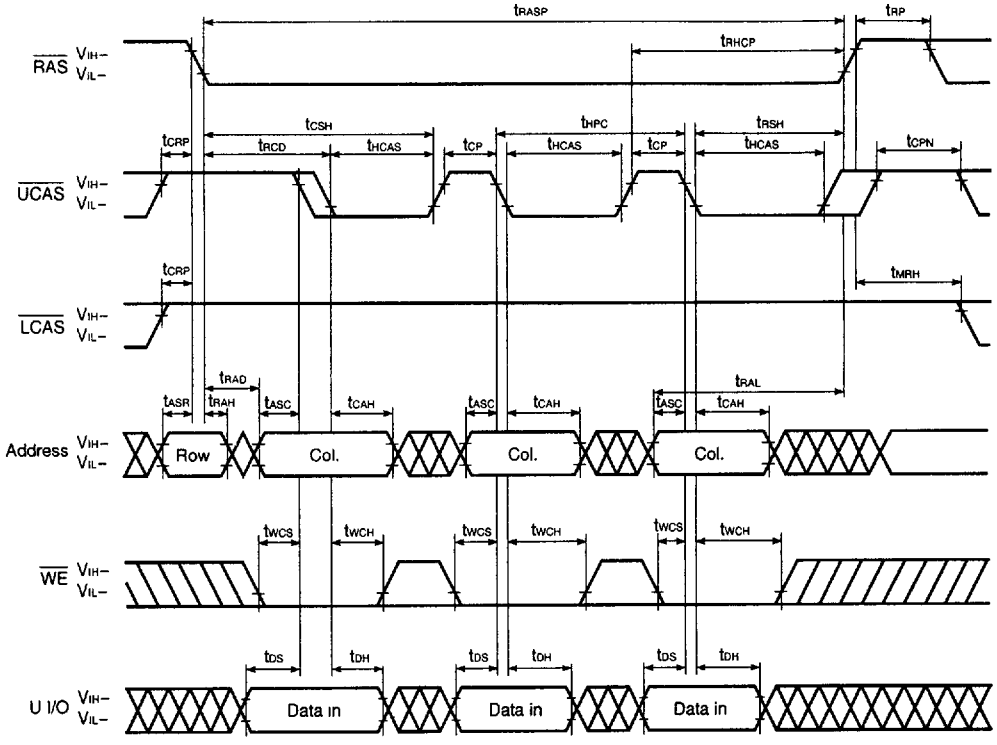


Hyper Page Mode Early Write Cycle



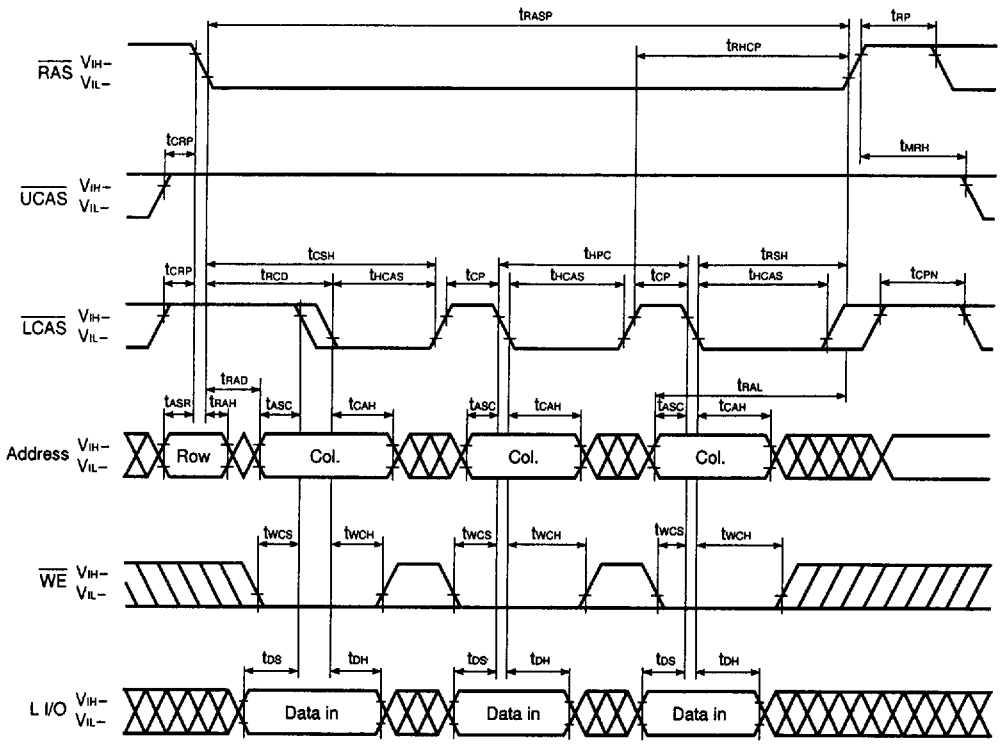
Remark $\overline{OE}$: Don't care

Hyper Page Mode Upper Byte Early Write Cycle



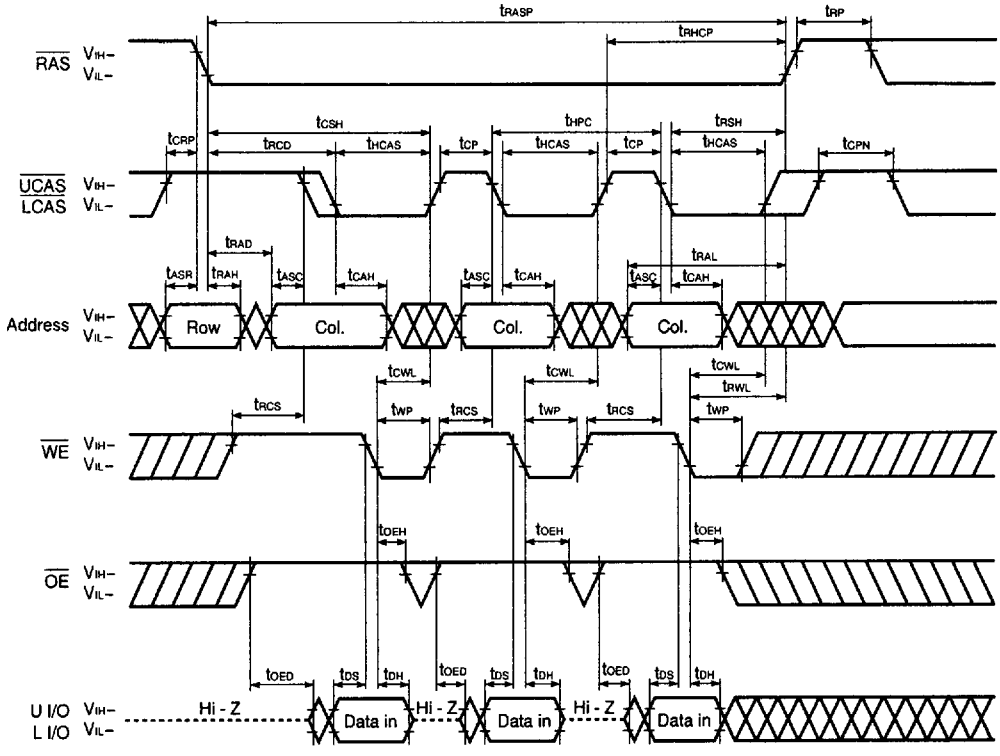
Remark $\overline{OE}$, L I/O : Don't care

Hyper Page Mode Lower Byte Early Write Cycle

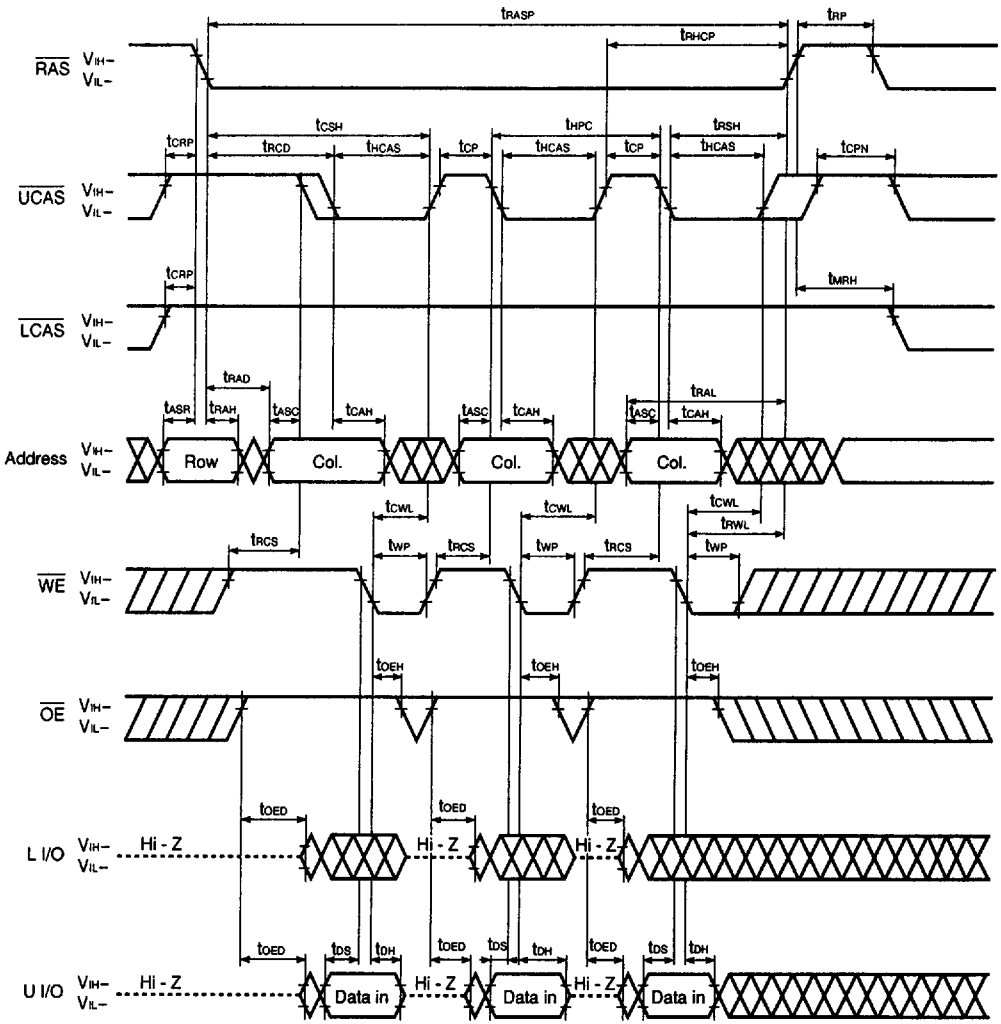


Remark $\overline{OE}$, U I/O : Don't care

Hyper Page Mode Late Write Cycle

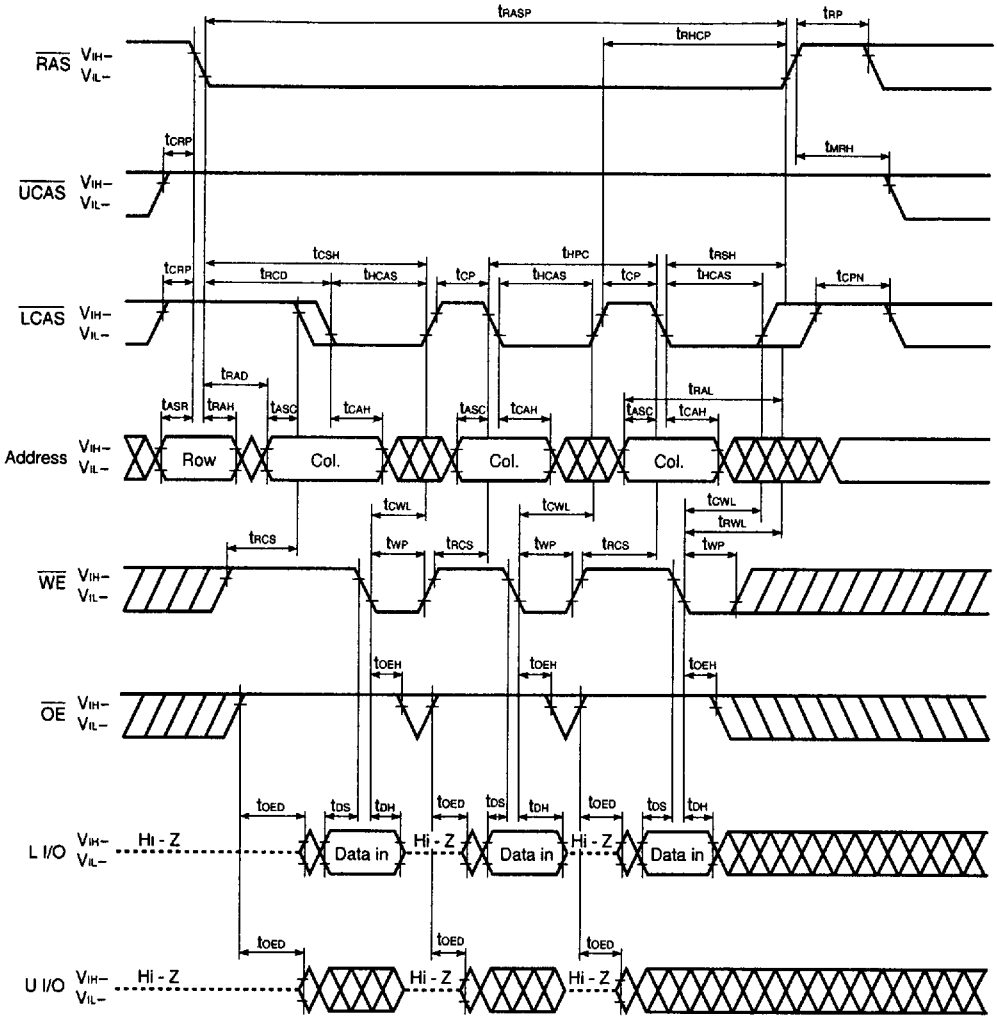


Hyper Page Mode Upper Byte Late Write Cycle



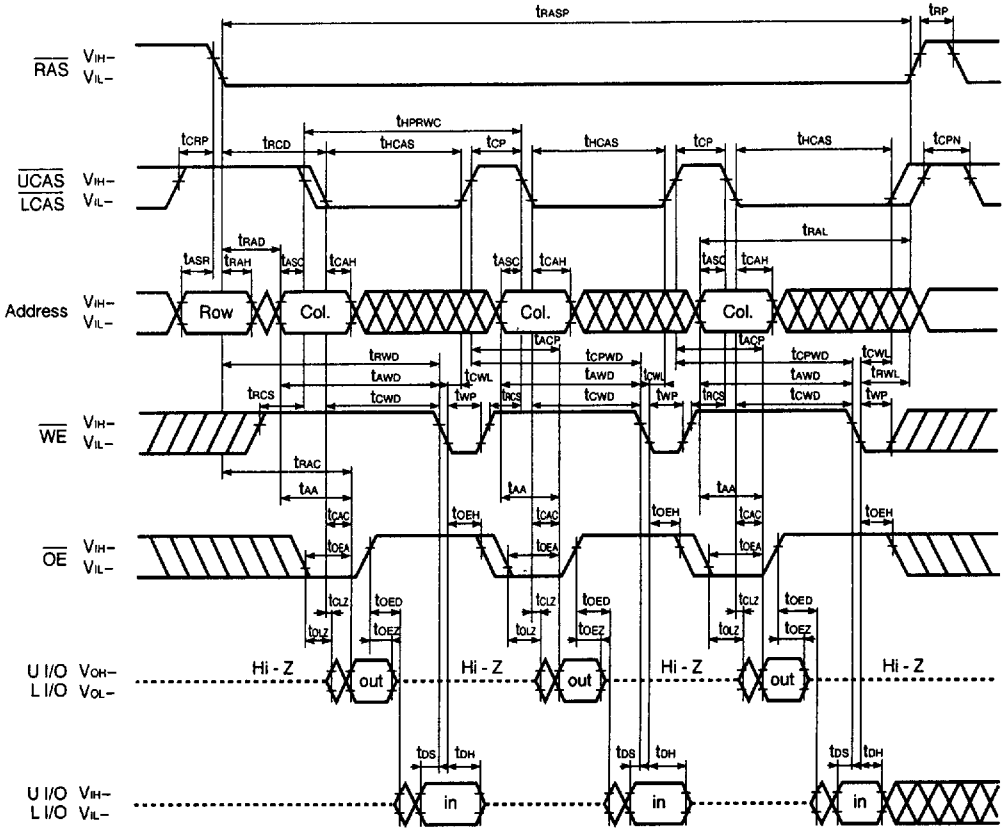
Remark In this cycle, the input data to Lower I/O is ineffective.

Hyper Page Mode Lower Byte Late Write Cycle

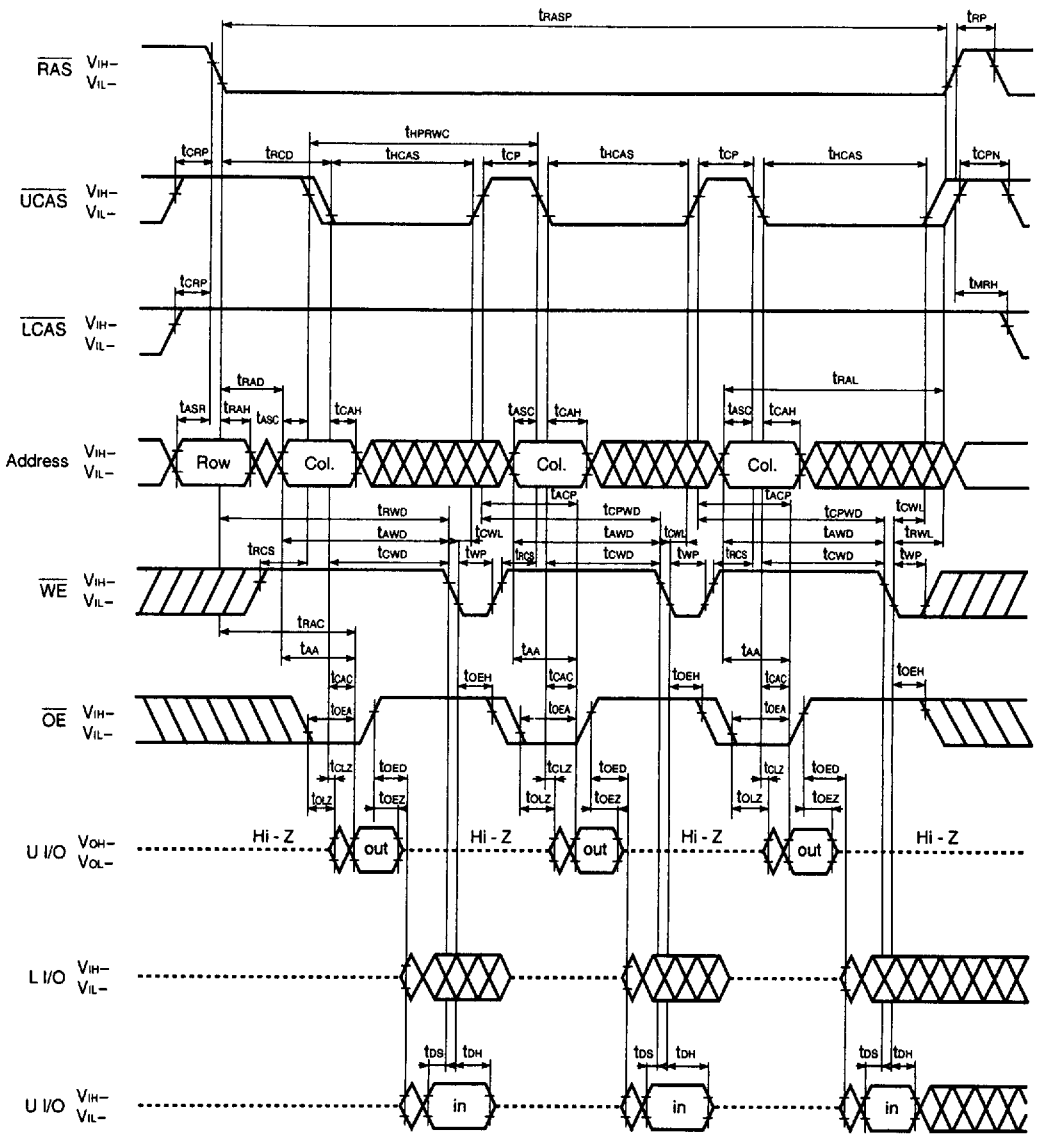


Remark In this cycle, the input data to Upper I/O is ineffective.

Hyper Page Mode Read Modify Write Cycle

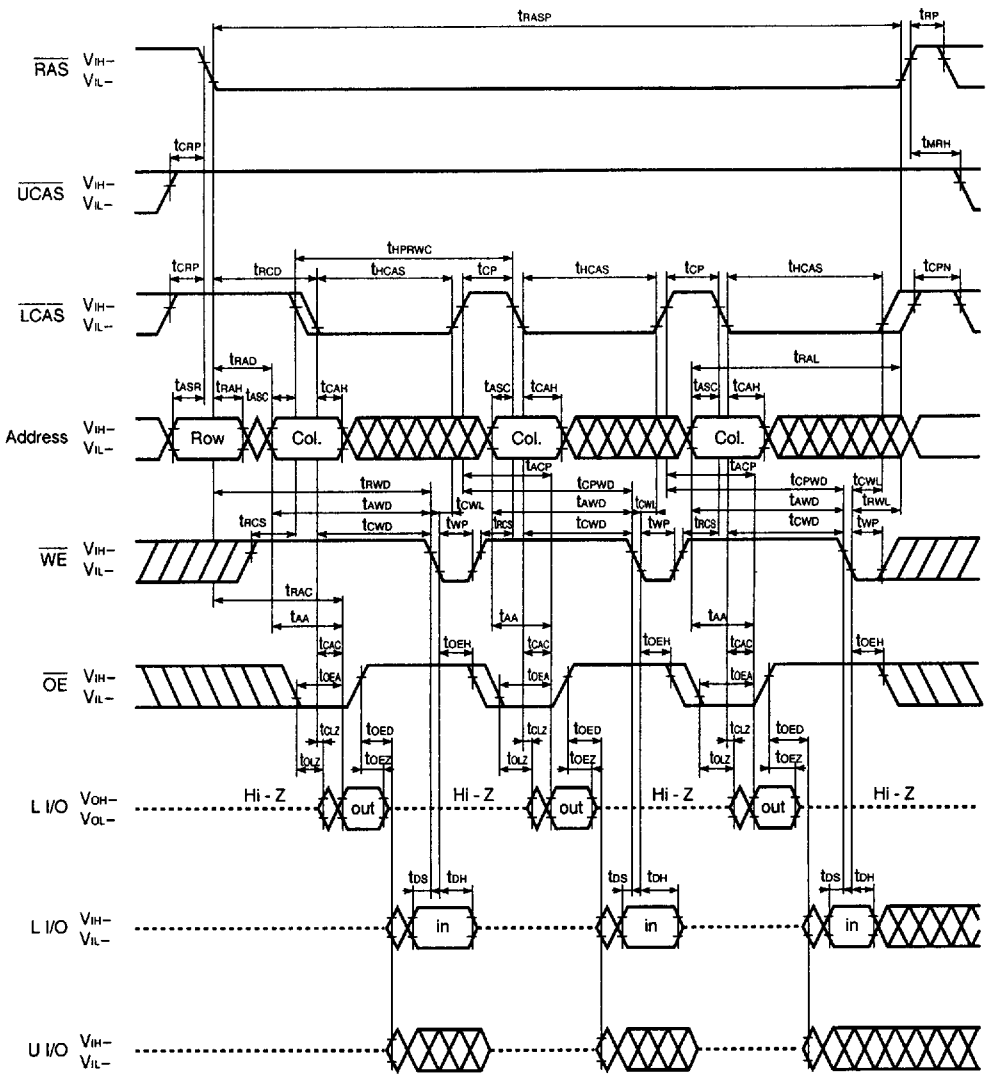


Hyper Page Mode Upper Byte Read Modify Write Cycle



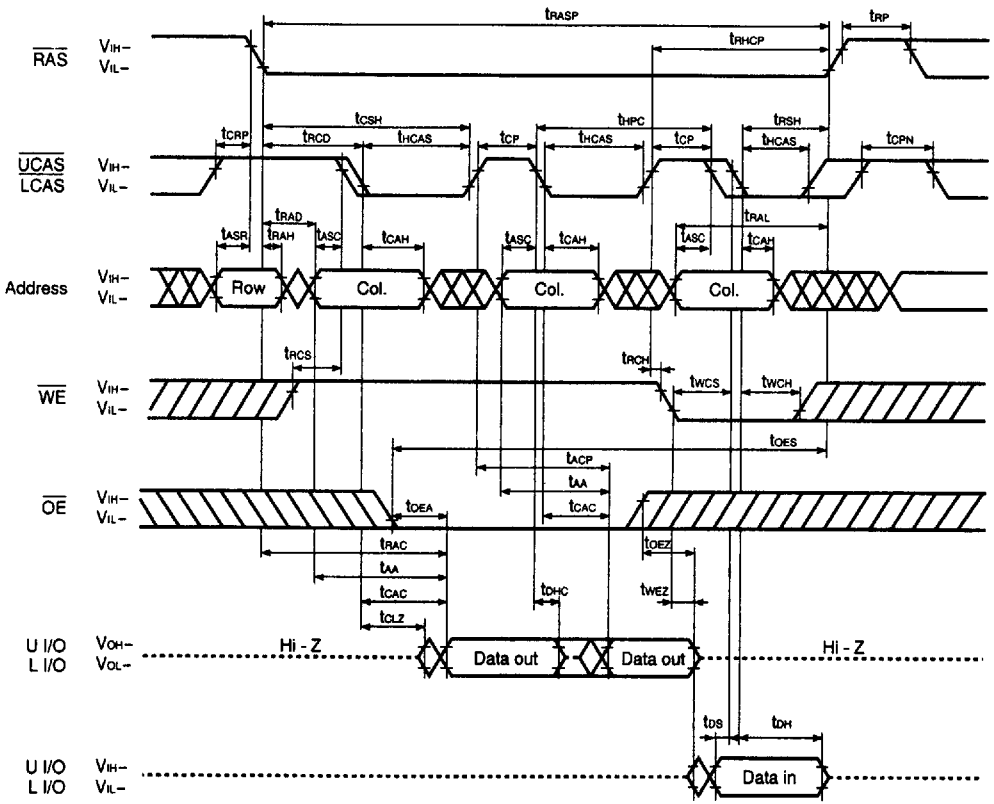
Remark In this cycle, the input data to Lower I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode Lower Byte Read Modify Write Cycle

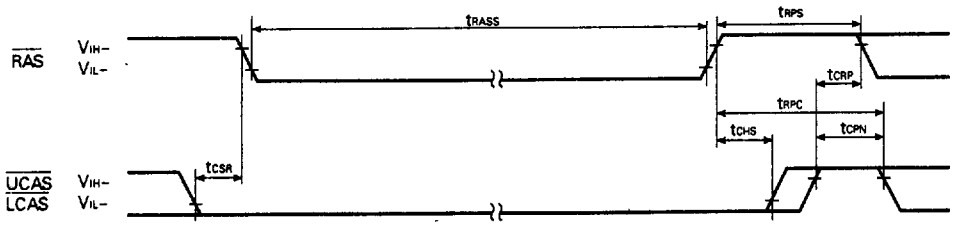


Remark In this cycle, the input data to Upper I/O is ineffective. The data out of that remains Hi-Z.

Hyper Page Mode Read and Write Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Self Refresh Cycle (Only for the μPD42S4210A)



Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Cautions on Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh

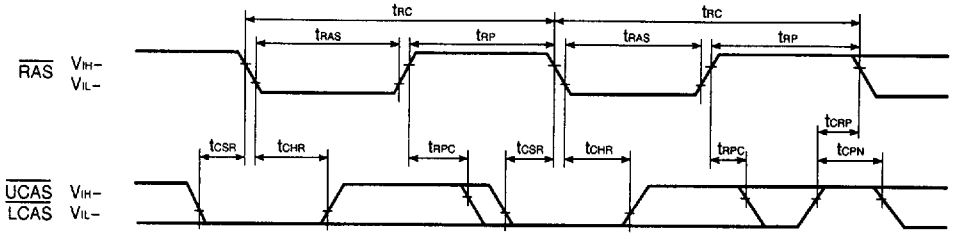
$\overline{CAS}$ before $\overline{RAS}$ self refresh can be used independently when used in combination with distributed $\overline{CAS}$ before $\overline{RAS}$ long refresh; However, when used in combination with burst $\overline{CAS}$ before $\overline{RAS}$ long refresh or with burst long $\overline{RAS}$ only refresh, the following cautions must be observed.

(1) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst $\overline{CAS}$ Before $\overline{RAS}$ Long Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{CAS}$ before $\overline{RAS}$ long refresh are used in combination, please perform $\overline{CAS}$ before $\overline{RAS}$ refresh 512 times within a 8 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

(2) Normal Combined Use of $\overline{CAS}$ Before $\overline{RAS}$ Self Refresh and Burst Long $\overline{RAS}$ Only Refresh
When $\overline{CAS}$ before $\overline{RAS}$ self refresh and burst $\overline{RAS}$ only refresh are used in combination, please perform $\overline{RAS}$ only refresh 512 times within a 8 ms interval just before and after setting $\overline{CAS}$ before $\overline{RAS}$ self refresh.

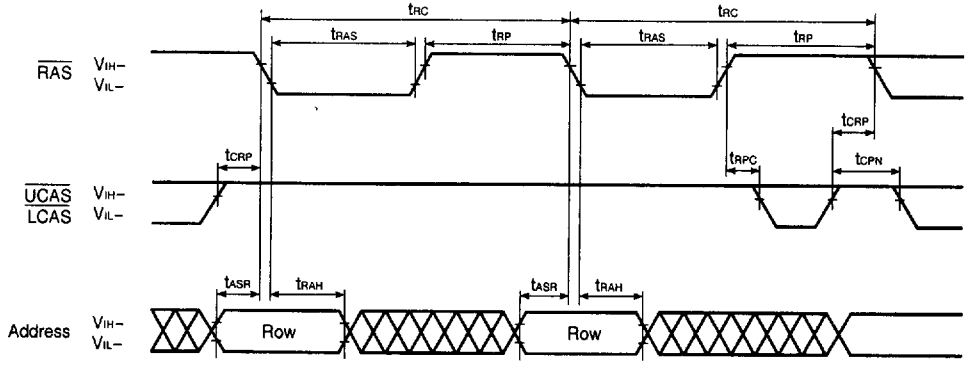
For details, please refer to **How to use DRAM** User's Manual.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



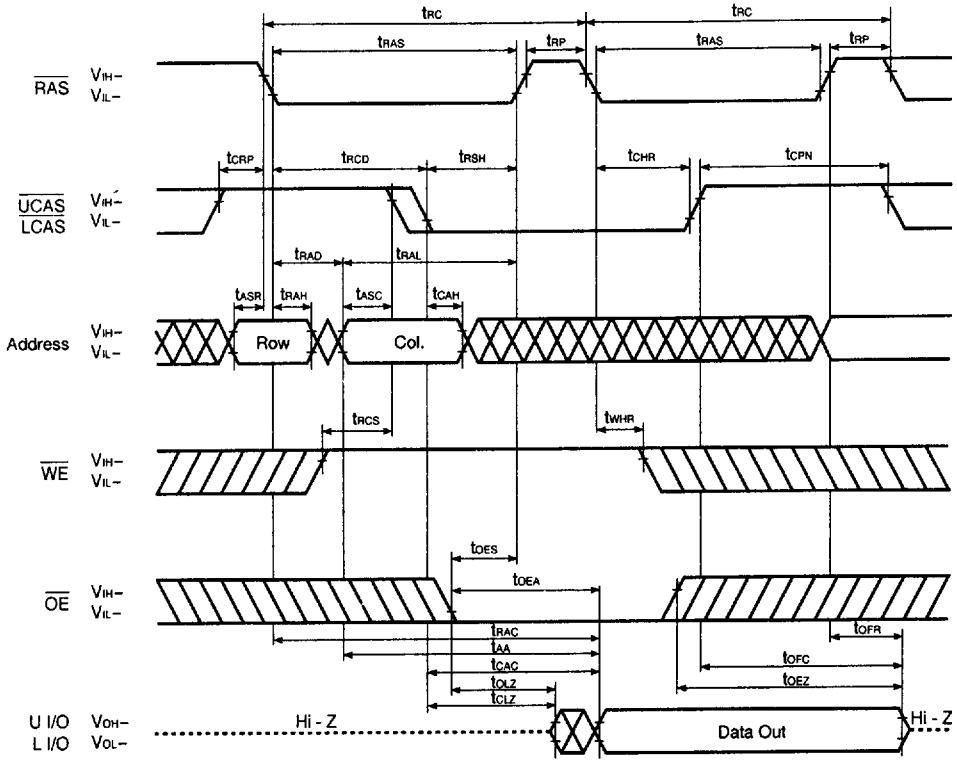
Remark Address, $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

$\overline{RAS}$ Only Refresh Cycle

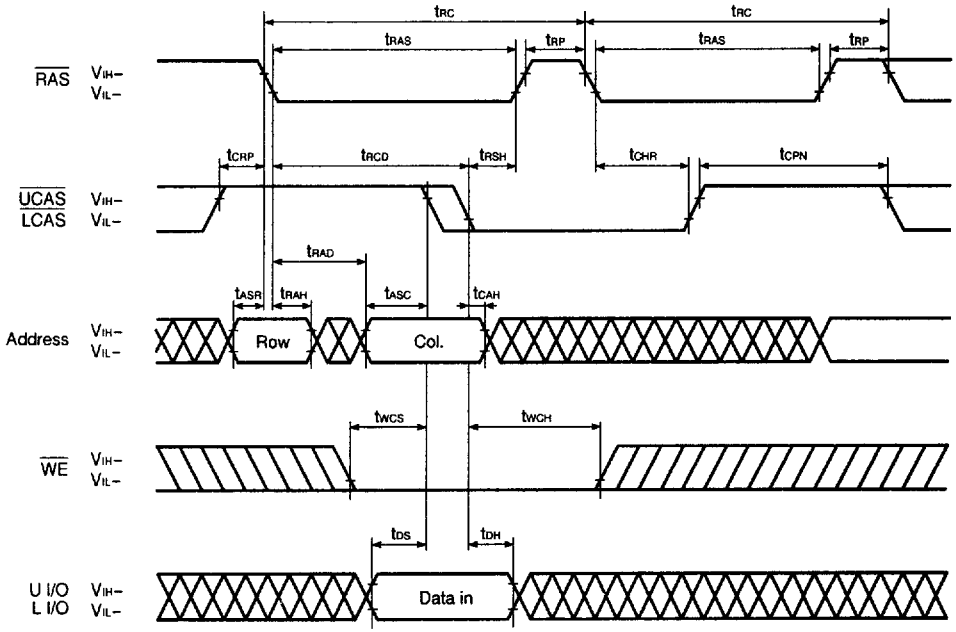


Remark $\overline{WE}$, $\overline{OE}$: Don't care L I/O, U I/O : Hi - Z

Hidden Refresh Cycle (Read)



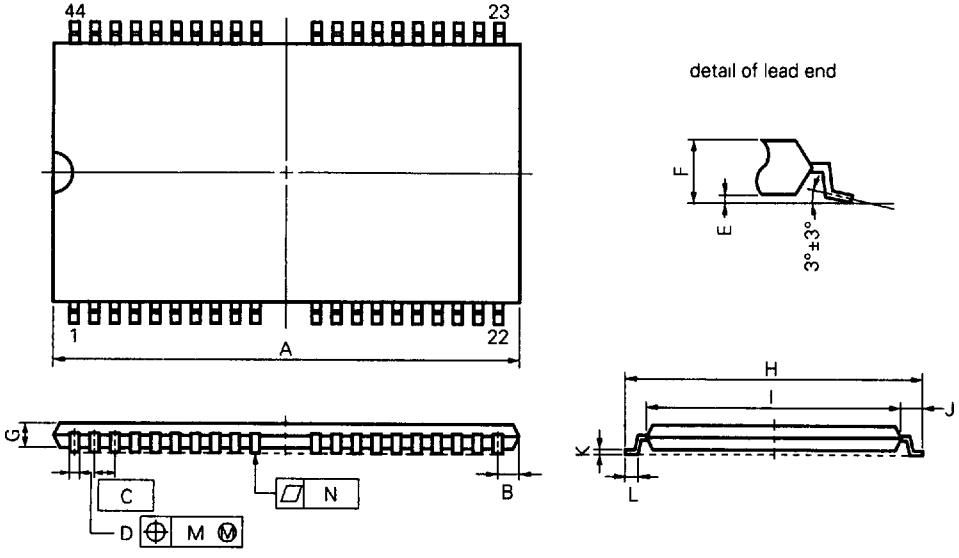
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

44 PIN PLASTIC TSOP(II) (400 mil)



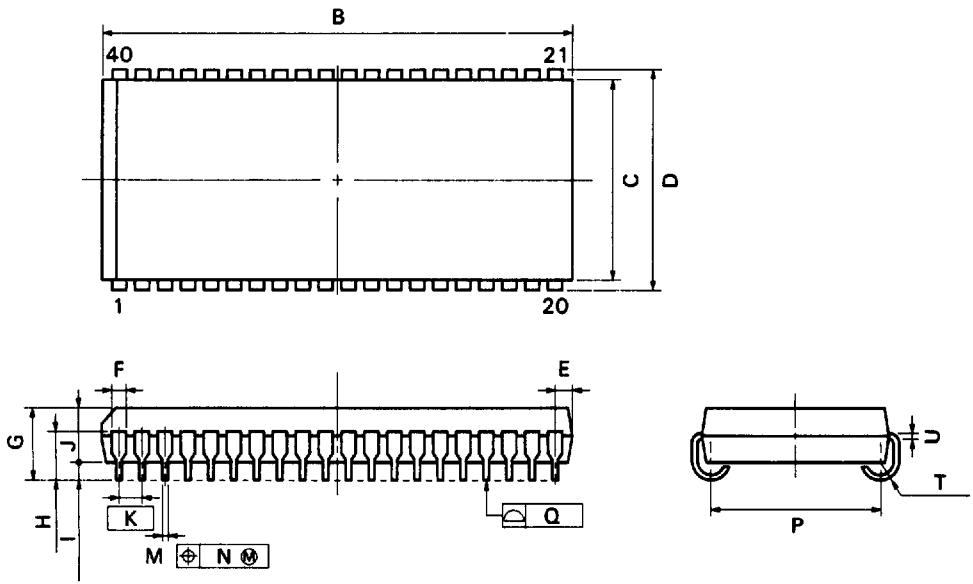
S44G5-80-7JF-1

NOTE

Each lead centerline is located within 0.13 mm (0 005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.81 MAX	0 741 MAX.
B	1.0 MAX.	0 040 MAX.
C	0.8 (T.P.)	0.031 (T.P)
D	0.30±0.10	$0.012^{+0\ 004}_{-0\ 005}$
E	0.05±0.05	0.002±0.002
F	1.1 MAX.	0.044 MAX.
G	0 97	0.038
H	11.76±0.2	0.463±0.008
I	10 16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0\ 009}_{-0\ 008}$
K	$0.125^{+0\ 10}_{-0\ 05}$	$0.005^{+0\ 004}_{-0\ 002}$
L	0.5±0.1	$0.020^{+0\ 004}_{-0\ 005}$
M	0.13	0 005
N	0.10	0.004

40PIN PLASTIC SOJ (400 mil)



P40LE-400A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$26.29^{+0.2}_{-0.35}$	$1.035^{+0.008}_{-0.014}$
C	10.16	0.400
D	11.18 ± 0.2	0.440 ± 0.008
E	1.08 ± 0.15	$0.043^{+0.006}_{-0.007}$
F	0.7	0.028
G	3.5 ± 0.2	0.138 ± 0.008
H	2.4 ± 0.2	$0.094^{+0.008}_{-0.008}$
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	0.40 ± 0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4 ± 0.20	0.370 ± 0.008
Q	0.15	0.006
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD42S4210A, 424210A.

Types of Surface Mount Device

μPD42S4210AG5-XX, 424210AG5-XX : 44-pin Plastic TSOP (II) (400 mil)
μPD42S4210ALE-XX, 424210ALE-XX : 40-pin Plastic SOJ (400 mil)