

TP5700A Telephone Speech Circuit

General Description

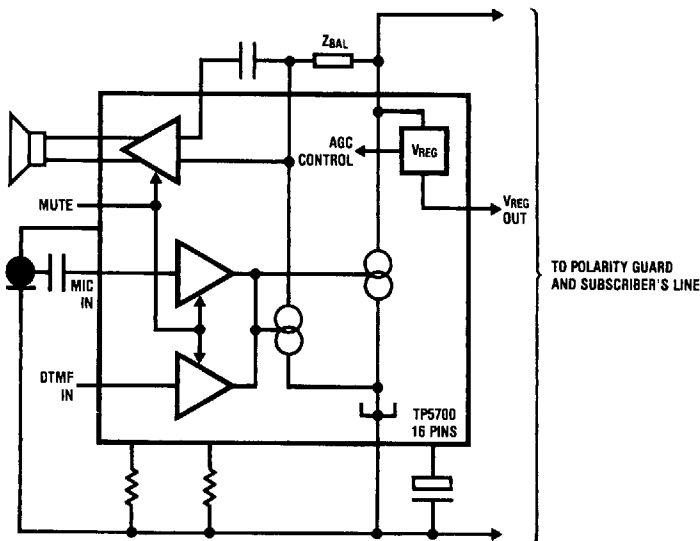
The TP5700A is a linear bipolar device which includes all the functions required to build the speech circuit of a telephone. It replaces the hybrid transformer, compensation circuit and sidetone network used in traditional designs. When used with an electret microphone (with integral FET buffer) and dynamic receiver, superior audio linearity, distortion and noise performance are obtained. Loop attenuation compensation is also included.

The low voltage design enables the circuit to work over a wide range of operating conditions, including long loops, extension telephones and subscriber carrier applications. Operating power is derived from the telephone line.

Features

- 5 mA–120 mA loop operation
- Voltage swing down to 1.0V
- Electret microphone amplifier
- Receive amplifier with push-pull outputs
- Automatic gain compensation for loop length
- Sidetone impedance independent of input impedance
- DTMF interface with muting
- Voltage regulator outputs for DTMF generator etc.
- Works in parallel with a standard phone on 20 mA loop
- Available in small outline surface mount package

Simplified Block Diagram



TL/H/5201-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V⁺ with Respect to V⁻ 20V
Voltage at Any Other Pin V⁺ + 0.3V to V⁻ - 0.3V

Operating Temperature, T_A -25°C to +70°C
Power Dissipation (Note 3) 1W
Storage Temperature, T_S -65°C to +150°C
Junction Temperature 150°C
Lead Temperature (Soldering, 10 seconds) 300°C

DC Electrical Characteristics

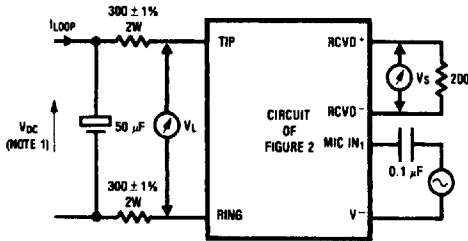
Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits printed in bold characters are guaranteed at T_A = 0°C to +60°C by correlation with 100% testing at T_A = 25°C. All other limits are assured by correlation with other production tests, and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{T-R}	Tip-Ring Voltage including nominal 1.4V polarity guard (See <i>Figure 1</i>)	I _{LOOP} = 5 mA		2.8	4.5	V
		= 20 mA		7		V
		= 50 mA		10.5		V
		= 80 mA		15		V
		= 120 mA				V
V _I	Minimum Instantaneous Voltage Swing	V ⁺ to V ⁻ I _{LOOP} = 5mA		1.0		V
TRANSMIT AMPLIFIER						
R _{XIN}	Input Resistance	From Pin 7 to V ⁻	15	30	50	kΩ
G _{XA}	Gain at 1 kHz	R _{AGC} = 0Ω to V ⁻ I _{LOOP} = 20 mA, T _A = 25°C only	33	35	37	dB
G _{XT}	Gain Variation v. T _A			±1		dB
G _{XI}	Gain Variation v. I _{LOOP}	I _{LOOP} = 20 to 100 mA		-6		dB
N _X	Transmit Noise	MIC IN ₁ = 0V		12	18	dBrnC
S/D _X	Signal/Total Harmonic Distortion	I _{LOOP} ≥ 20 mA V _L = 800 mVrms		2	10	%
G _{XM}	Gain Change when MUTED	MUTE IN ≥ V _{MON}		-55		dB
DTMF AMPLIFIER						
R _{DIN}	Input Resistance	From Pin 8 to V ⁻	10	20	55	kΩ
G _{XD}	Gain at 1 kHz	R _{AGC} = 0Ω to V ⁻ I _{LOOP} = 20 mA, T _A = 25°C only	3.5	5.5	7.5	dB
S/D _{XD}	Signal/Total Harmonic Distortion	I _{LOOP} = 20 mA V _L = 1.06 Vrms, T _A = 25°C only		3	10	%
G _{XD} T	Gain Variation v. T _A			±1		dB
G _{XD} I	Gain Variation v. I _{LOOP}	I _{LOOP} = 20 to 100 mA		-6		dB
MUTE INPUT						
I _{MIN}	Input Current	Pin 9 = 1.5V		40		μA
V _{MOFF}	MUTE OFF Input Voltage				0.5	V
V _{MON}	MUTE ON Input Voltage		1.5			V

DC Electrical Characteristics (Continued)

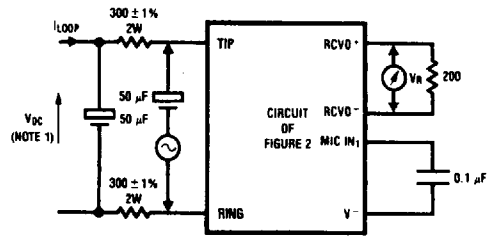
Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits printed in bold characters are guaranteed at $T_A = 0^\circ\text{C}$ to $+60^\circ\text{C}$ by correlation with 100% testing at $T_A = 25^\circ\text{C}$. All other limits are assured by correlation with other production tests, and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE AMPLIFIER						
R_{RIN}	Input Resistance	From Pin 12 to V^-	20	35	55	$k\Omega$
G_{RA}	Gain at 1 kHz	$R_{AGC} = 0\Omega$, MUTE IN $\leq V_{MOFF}$ $I_{LOOP} = 20\text{ mA}$, $T_A = 25^\circ\text{C}$ only	-5.5	-4	-2.5	dB
G_{RT}	Gain Variation v. T_A			± 0.5		dB
G_{RI}	Gain Variation v. I_{LOOP}	$I_{LOOP} = 20$ to 100 mA		-6		dB
G_{RM}	Gain Change when MUTED	MUTE IN $\geq V_{MON}$	-15	-20	-23	dB
N_R	Receive Noise	$V_{RCVIN} = 0\text{V}$		0	10	dBmC
S/DR	Signal/Total Harmonic Distortion	$V_R = 200\text{ mVrms}$ $I_{LOOP} \geq 20\text{ mA}$		2	10	%
V_{RC}	Output Clipping Level	$I_{LOOP} \geq 20\text{ mA}$		1		Vp-p
V_{ROS}	Output Offset Voltage				± 100	mV
SIDETONE CHARACTERISTICS						
STC	Sidetone Cancellation at 1kHz	$20\text{ mA} \leq I_{LOOP} \leq 100\text{ mA}$, (Note 2)	11	15		dB
VOLTAGE REGULATOR OUTPUTS						
V_{REG1}	Output Voltage, Pin 10	$I_{LOOP} \geq 20\text{ mA}$ MUTE IN $\leq V_{MOFF}$ MUTE IN $\geq V_{MON}$	2 3	3.2		V V
I_{REG1}	Maximum Output Current, Pin 10	MUTE IN $\leq V_{MOFF}$ MUTE IN $\geq V_{MON}$		200 2.7		μA mA
V_{REG2}	Output Voltage, Pin 11	$I_{LOOP} \geq 20\text{ mA}$	1.1	1.2		V
I_{REG2}	Maximum Output Current, Pin 11	$I_{LOOP} \geq 20\text{ mA}$	300	500		μA



TL/H/5201-2

1a. Test Circuit for Transmit and Sidetone



TL/H/5201-3

1b. Test Circuit for Receive

FIGURE 1. Test Circuits for Electrical Characteristics

Note 1. Adjust V_{DC} to set specified I_{LOOP} current.

Note 2. To measure Sidetone Cancellation, set oscillator in *Fig. 1a* for $V_L = 100\text{ mVrms}$; measure V_S . Then in *Fig. 1b* set oscillator = 100 mVrms ; measure V_R . $STC = 20 \log V_R/V_S$.

Note 3. For operation above 25°C , the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 70°C/W junction to ambient.

Functional Description

The TP5700A Telephone Speech Circuits are powered from the telephone Tip and Ring terminals via a full-wave rectifier bridge to protect against loop polarity reversals. The devices provide the following functions:

LINE REGULATOR

A DC regulator sinks current from the loop in order to maintain a DC slope resistance similar to that of a standard phone. R_{DC} provides an adjustment for the slope resistance.

MICROPHONE AMPLIFIER

A single-ended input amplifier on the TP5700A enables a low cost electret microphone to be used. This provides superior distortion, linearity and noise performance compared to a traditional carbon microphone. The electret should be capacitively coupled to the amplifier input. The acoustic sensitivity of the microphone is intended to be in the range of -60 to $-70\text{ dBV}/\mu\text{Bar}$.

Loss can be inserted if required by adding a resistive potentiometer either at MIC IN₁ or the connection between the pre-amp output and driver stage input. The driver stage pro-

Functional Description (Continued)

vides automatic gain compensation to reduce the gain as loop length decreases. The AGC range can be adjusted by means of R_{AGC} to limit the maximum loss on a short loop from 0 to 6 dB.

RECEIVE AMPLIFIER

This buffer amplifier provides the necessary gain or loss for the receive signal. RCV IN should be AC coupled to SIDETONE (pin 4). Automatic gain control is built into the amplifier to reduce the gain as loop length decreases. The AGC range is adjusted in common with the transmit AGC range with a range of adjustment for maximum loss from 0 to 6 dB. Push-pull complementary outputs provide balanced direct drive to a dynamic transducer, which may have an impedance as low as 100Ω. The effective receive gain can be reduced by adding a resistor in series with the transducer. The receive gain is automatically reduced by 20 dB when the MUTE input is pulled high.

SIDETONE CIRCUIT

The level of Sidetone cancellation may be adjusted by connecting an external balance impedance to SIDETONE (pin 4) and coupling this point to V^+ . For good sidetone cancellation the balance impedance should be approximately 10 times the subscriber line input impedance. Some typical component values to match a precise 600Ω termination for test purposes are shown in Figure 2. Use the component values shown in the Applications Section for better results over a wide range of telephone line impedances.

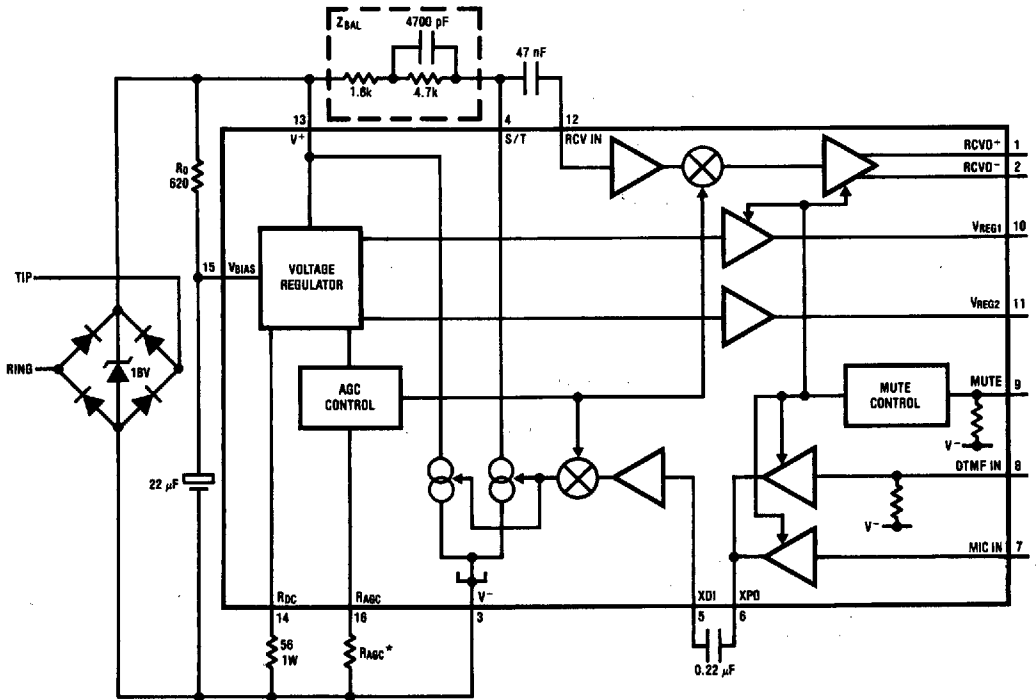
DTMF AMPLIFIER

An additional transmit amplifier is included to enable the open-emitter output of a conventional DTMF generator to be connected to the line via the transmit output stage. This path includes the transmit AGC section. When the MUTE input is pulled high, the DTMF input is enabled and the MIC input disabled. When MUTE IN is open-circuit or pulled to V^- the DTMF input is switched off and the MIC input is enabled.

VOLTAGE REGULATOR OUTPUTS

A precision band-gap voltage reference controls a regulator to provide bias for internal circuits. Two auxiliary outputs are also available. V_{REG1} is provided specifically for powering a low voltage pulse dialer or DTMF generator. In order to protect this output in low voltage situations where the instantaneous voltage across the Speech Circuit may swing below the V_{REG1} output voltage, an internal switch controls the maximum available output current. In speech mode, MUTE IN is low, V_{REG1} output will track approximately 1/2 the Tip-Ring voltage and the available output current is limited to 200 μA. This is adequate to power a DTMF generator in standby mode. When MUTE IN is pulled high to switch the Speech Circuit to the DTMF dialing mode, V_{REG1} is switched to a 3V regulated output and up to 2 mA may be drawn from it to power the active DTMF generator.

A 1.2V regulated output is also provided at V_{REG2} to power a low voltage 2-wire electret microphone such as the Primo EM80-PM12.



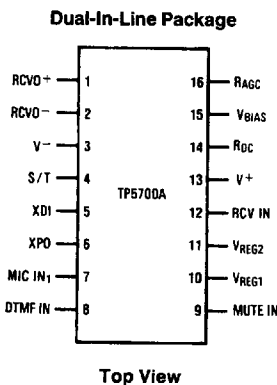
TL/H/5201-4

* See Figure 3

Note: ZBAL circuit shown is for test purposes with a resistive line termination. See Applications Information for suggested component values for normal reactive line applications.

FIGURE 2. TP5700A Telephone Speech Circuits

Connection Diagram



TL/H/5201-5

Order Number TP5700AM or TP5700AN
See NS Package M16B or N16A

Pin Descriptions

Pins 1, 2 RCVO⁺ and RCVO⁻

The push-pull complementary outputs of the receive amplifier. Dynamic transducers with a minimum impedance of 100 Ω can be directly driven by these outputs.

Pin 3 V⁻

This is the negative supply input to the device and should be connected to the negative output of the polarity guard. All other voltages on the device are referred to this pin.

Pin 4 S/T

This is the output of the Sidetone cancellation signal, which requires a balance impedance of approximately 10 times the subscriber's line impedance to be connected from this pin to V⁺ (pin 13).

Pin 5 XDI

The input to the line output driver amplifier. Transmit AGC is applied in this stage.

Pin 6 XPO

This is the transmit pre-amp output which is normally capacitively coupled to pin 5.

Pin 7 MIC IN₁

This is the inverting input to the transmit pre-amplifier and is intended to be capacitively coupled to an FET-buffered electret microphone.

Pin 8 DTMF IN

The DTMF input which has an internal resistor to V⁻ to provide the emitter load resistor for a CMOS DTMF generator. This input is only active when MUTE IN (pin 9) is pulled high.

Pin 9 MUTE IN

The MUTE Input, which must be pulled at least 1.5V higher than V⁻ to mute MIC IN and enable DTMF IN.

Pin 10 VREG1

The regulated output for biasing a pulse dialer or DTMF generator. A 4.7 μ F decoupling capacitor to V⁻ should be fitted if this output is used.

Pin 11 VREG2

A 1.2V regulated output suitable for powering a low-voltage electret microphone. A 1 μ F decoupling capacitor to V⁻ should be fitted if this output is used.

Pin 12 RCV IN

The receive AGC amplifier input.

Pin 13 V⁺

This is the positive supply input to the device and should be connected to the positive output of the polarity guard. The current through this pin is modulated by the transmit signal.

Pin 14 RDC

An external 1W resistor is required from this pin to V⁻ to control the DC input impedance of the circuit. The nominal value is 56 Ω for low voltage operation. Values up to 82 Ω may be used to increase the available transmit output voltage swing at the expense of low voltage operation.

Pin 15 VBIAS

This internal voltage bias line must be connected to V⁺ via an external resistor, R_O, and decoupled to V⁻ with a 22 μ F capacitor. R_O dominates the AC input impedance of the circuit and should be 620 Ω for a 600 Ω input impedance or 910 Ω for a 900 Ω input impedance.

Pin 16 RAGC

The range of transmit and receive gain variations between short and long loops may be adjusted by connecting a resistor from this pin to V⁻ (pin 3). *Figure 3* shows the relationship between the resistor value and the AGC range. This pin may be left open-circuit to defeat AGC action.

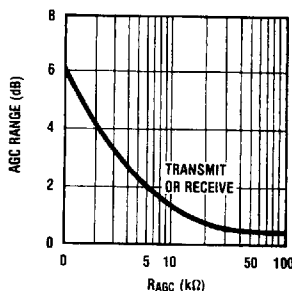


FIGURE 3

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Applications Information

The TP5700A and TP5700 are flexible circuits designed with several user adjustments to enable the performance to be optimized for different applications. The choice of transducer types and the cavities in which they are mounted will also greatly influence the acoustic performance of the telephone. Some of the consequences of circuit adjustments are as follows:

R_{DC} ADJUSTMENT

56Ω is the recommended value for R_{DC} if it is required to meet a maximum Tip-Ring voltage of 4.5V on a 20 mA loop (assuming no more than 1.4V is dropped across the polarity guard). If a higher Tip-Ring voltage is acceptable, R_{DC} may be increased, which will provide a small increase in the available transmit output voltage swing before clipping occurs. R_{DC} should be less than 82Ω to avoid exceeding the maximum rated voltage on a short loop.

R_{AGC} ADJUSTMENT

The available AGC range is more than adequate to compensate for the loss of most loops. R_{AGC} should be chosen only to partly compensate for the anticipated maximum loop loss, as over-compensation may tend to exaggerate the variations of sidetone with loop length.

SIDETONE ADJUSTMENT

The component values used for Z_{BAL} should be selected to provide a clear sidetone sound without excessive "hollowness." The capacitor value and ratio of the two resistors will fix the pole location. To avoid reducing the low voltage performance of the circuit the sum of the two resistors should not exceed 10 kΩ.

POWERING ELECTRET MICROPHONES

Electret microphones with integral FET buffers are available in both two-wire and three-wire versions and a range of op-

erating voltage ranges. There are four methods of powering the microphone.

1. The 1.2V V_{REG2} output provides the lowest voltage method for microphones rated down to 1V. V_{REG2} must be decoupled with a 1 μF capacitor to ground. (See Figure 5.)
2. If V_{REG1} is not required for DTMF generator operation, it may be used to provide up to 200 μA for microphone power.
3. V_{BIAS} (pin 15) may be used as a decoupled, but unregulated, supply for electrets requiring a higher operating voltage than V_{REG1} or V_{REG2}. The additional current drawn through R_O will, however, raise the minimum operating voltage of the Speech Circuit. If this method is used the decoupling capacitor must be increased to at least 100 μF to maintain good low frequency return loss. (See Figure 4.)
4. An electret type with a good power supply rejection ratio can be powered from V⁺, or a regulated and decoupled supply dropped from V⁺.

STONE DIALING TELEPHONE

Figure 4 shows the TP5700 directly interfacing to a low voltage DTMF generator. V_{REG1} supplies the necessary 2V minimum bias to enable the low voltage tone dialer to sense key closures and pull its MUTE output high. V_{REG1} then switches to a 3V regulated output to sustain the Tone Dialer during tone generation. The TP5700A DTMF input incorporates the necessary load resistor to V⁻ and provides gain plus AGC action to compensate for loop length. A muted tone level is heard in the receiver. For DTMF generators with a higher output level, a resistive potentiometer should

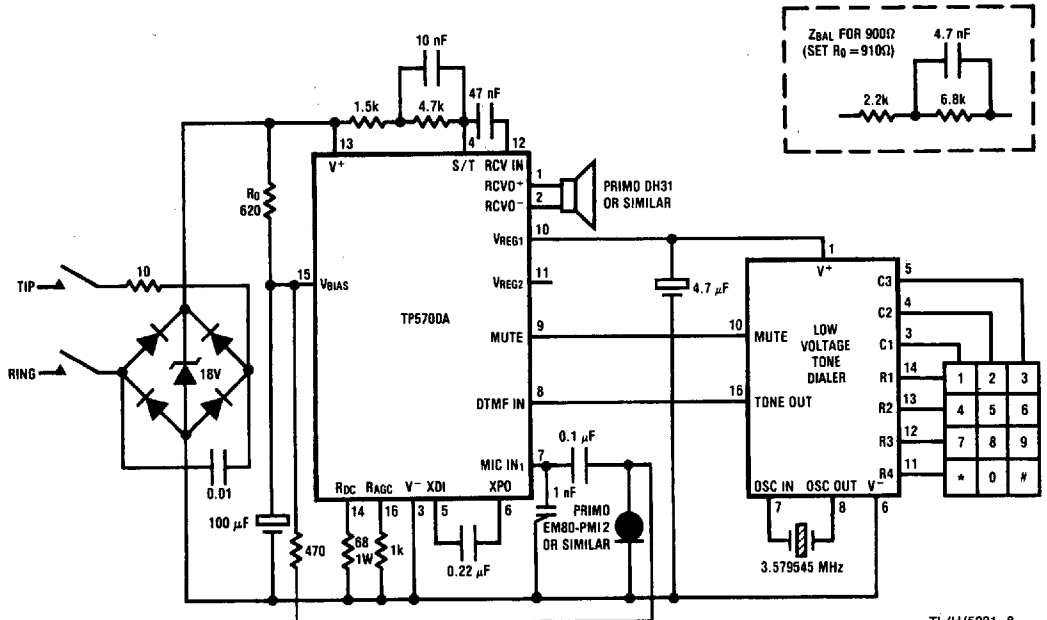


FIGURE 4. Typical Tone Dialing Telephone

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Applications Information (Continued)

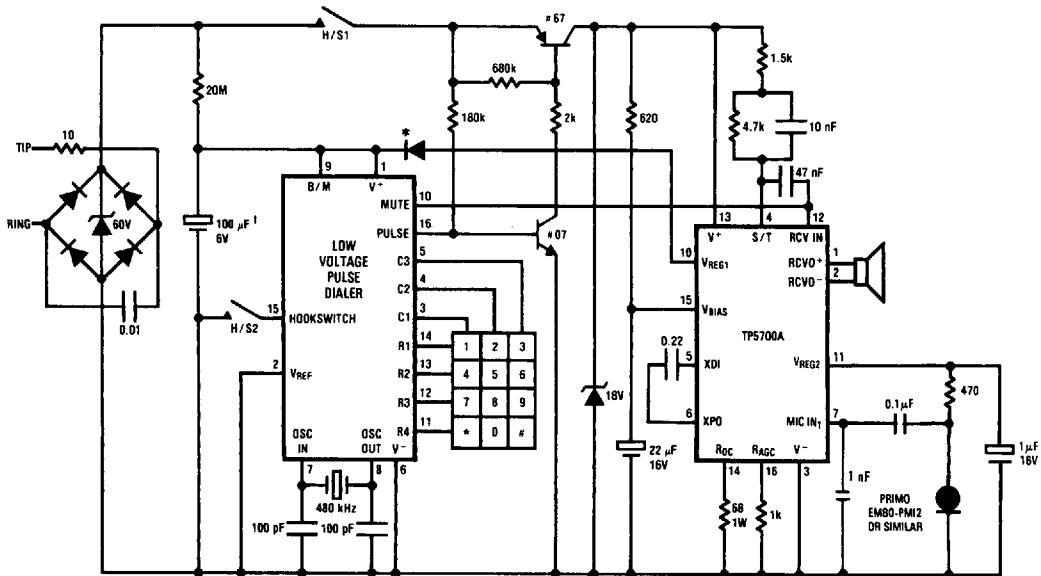
be added to reduce the level at the speech circuit DTMF Input. For application requiring higher DTMF level, the signal swing across the device can be raised by using 620Ω in series with 270Ω for R_O . The 270Ω has to be bypassed by a $10\ \mu\text{F}$ capacitor in order to maintain same AC off hook impedance.

PULSE DIALING TELEPHONE

The TP5700A can reduce the number of components required to build a pulse dialing telephone, as shown in Figure 5. The usual current source can be eliminated by using the V_{REG1} output to power a low-voltage (1.7V) series mode pulse dialer via a blocking diode. A low forward-voltage drop diode such as a Schottky type is necessary because

V_{REG1} is used in its non-regulated mode and its output voltage may fall to 2V on a 20 mA loop. A $100\ \mu\text{F}$ decoupling capacitor is required to hold up the pulse dialer supply voltage during dialing. This capacitor will take about one second to charge up when the telephone is first connected to the line, but thereafter the 20 M Ω resistor required to retain the last-number dialed memory will keep this capacitor charged. Partial muting is obtained by directly connecting the N-channel open-drain MUTE output of the pulse dialer to the RCY IN pin on the Speech Circuit.

A fully muted pulse dialer design requires the use of a shunt-mode dialer.



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*Low voltage drop diode (e.g. Schottky)

† Low leakage type

Indicates National Semiconductor discrete transistor process number

FIGURE 5. Typical Pulse Dialing Telephone

Application Information

A block diagram of the basic phase locked loop is shown in *Figure 1*.

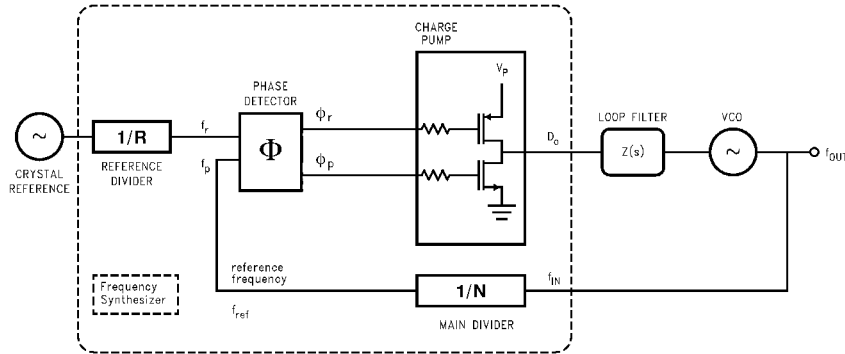


FIGURE 1. Basic Charge Pump Phase Locked Loop

LOOP GAIN EQUATIONS

A linear control system model of the phase feedback for a PLL in the locked state is shown in *Figure 2*. The open loop gain is the product of the phase comparator gain (K_ϕ), the VCO gain (K_{VCO}/s), and the loop filter gain $Z(s)$ divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in *Figure 3*, while the complex impedance of the filter is given in *Equation (1)*.

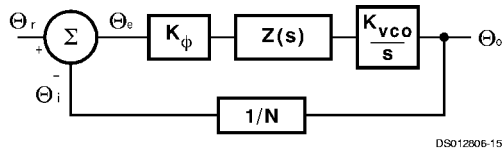


FIGURE 2. PLL Linear Model

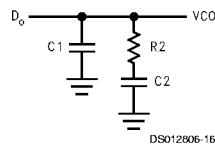


FIGURE 3. Passive Loop Filter

$$\begin{aligned} \text{Open loop gain} &= H(s)G(s) = \Theta_i/\Theta_e \\ &= K_\phi Z(s) K_{VCO}/Ns \\ Z(s) &= \frac{s(C1 \cdot R2) + 1}{s^2(C1 \cdot C2 \cdot R2) + sC1 + sC2} \quad (1) \end{aligned}$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \cdot \frac{C1 \cdot C2}{C1 + C2} \quad (2)$$

and

$$T2 = R2 \cdot C2 \quad (3)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω , the filter time constants $T1$ and $T2$, and the design constants K_ϕ , K_{VCO} , and N .

$$G(s) \cdot H(s)|_{s=j\omega} = \frac{-K_\phi \cdot K_{VCO} (1 + j\omega \cdot T2)}{\omega^2 C1 \cdot N (1 + j\omega \cdot T1)} \cdot \frac{T1}{T2} \quad (4)$$

From *Equations (2)*, *(3)* we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in *Equation (5)*.

$$\phi(\omega) = \tan^{-1}(\omega \cdot T2) - \tan^{-1}(\omega \cdot T1) + 180^\circ \quad (5)$$

A plot of the magnitude and phase of $G(s)H(s)$ for a stable loop, is shown in *Figure 4* with a solid trace. The parameter ϕ_p shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency ω_p of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, ω_p' , as double the frequency which gave us our original loop bandwidth, ω_p , the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6 dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase—just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of *Figure 4* over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase *Equation (4)* and *Equation (5)* will have to compensate by the corresponding “ $1/\omega$ ” or “ $1/\omega^2$ ” factor. Examination of equations *Equations (2)*, *(3)* and *Equation (5)* indicates the damping resistor variable $R2$ could be chosen to compensate the “ ω ” terms for the phase margin. This implies that another resistor of equal value to $R2$ will need to be switched in parallel with $R2$ during the initial lock period. We must also insure that the magnitude of the open loop gain, $H(s)G(s)$ is equal to zero at $\omega_p' = 2\omega_p$. K_{VCO} , K_ϕ , N , or the net product of these terms can be changed by a factor of 4, to counteract the ω^2 term present in the denominator of *Equation (2)* and *Equation (3)*. The K_ϕ term was chosen to complete the transformation because it can readily be

Application Information (Continued)

switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1 mA in the standard mode to 4 mA in Fastlock.

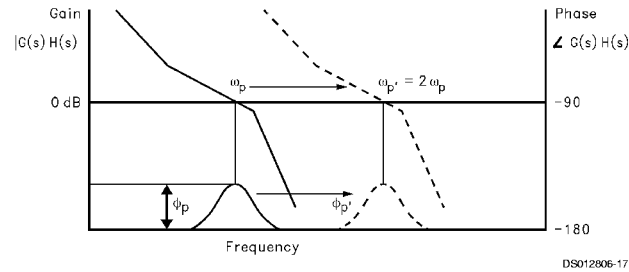


FIGURE 4. Open Loop Response Bode Plot

FASTLOCK CIRCUIT IMPLEMENTATION

A diagram of the Fastlock scheme as implemented in National Semiconductors LMX233XL PLL is shown in Figure 5. When a new frequency is loaded, and the RF Icp_o bit is set high the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second iden-

tical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending a MICROWIRE instruction with the RF Icp_o bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

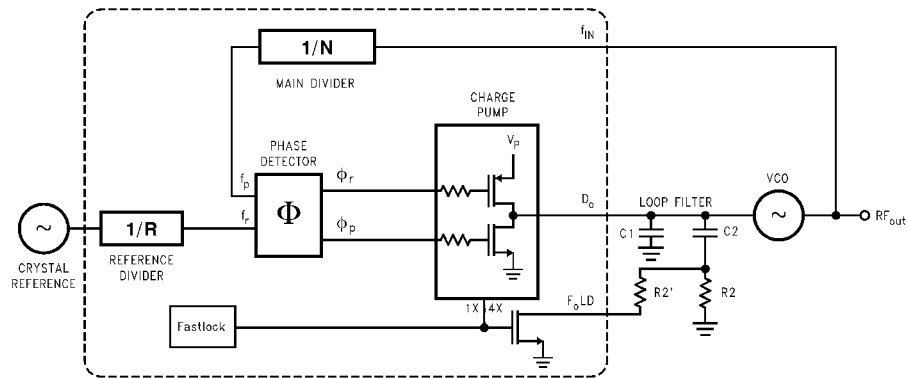
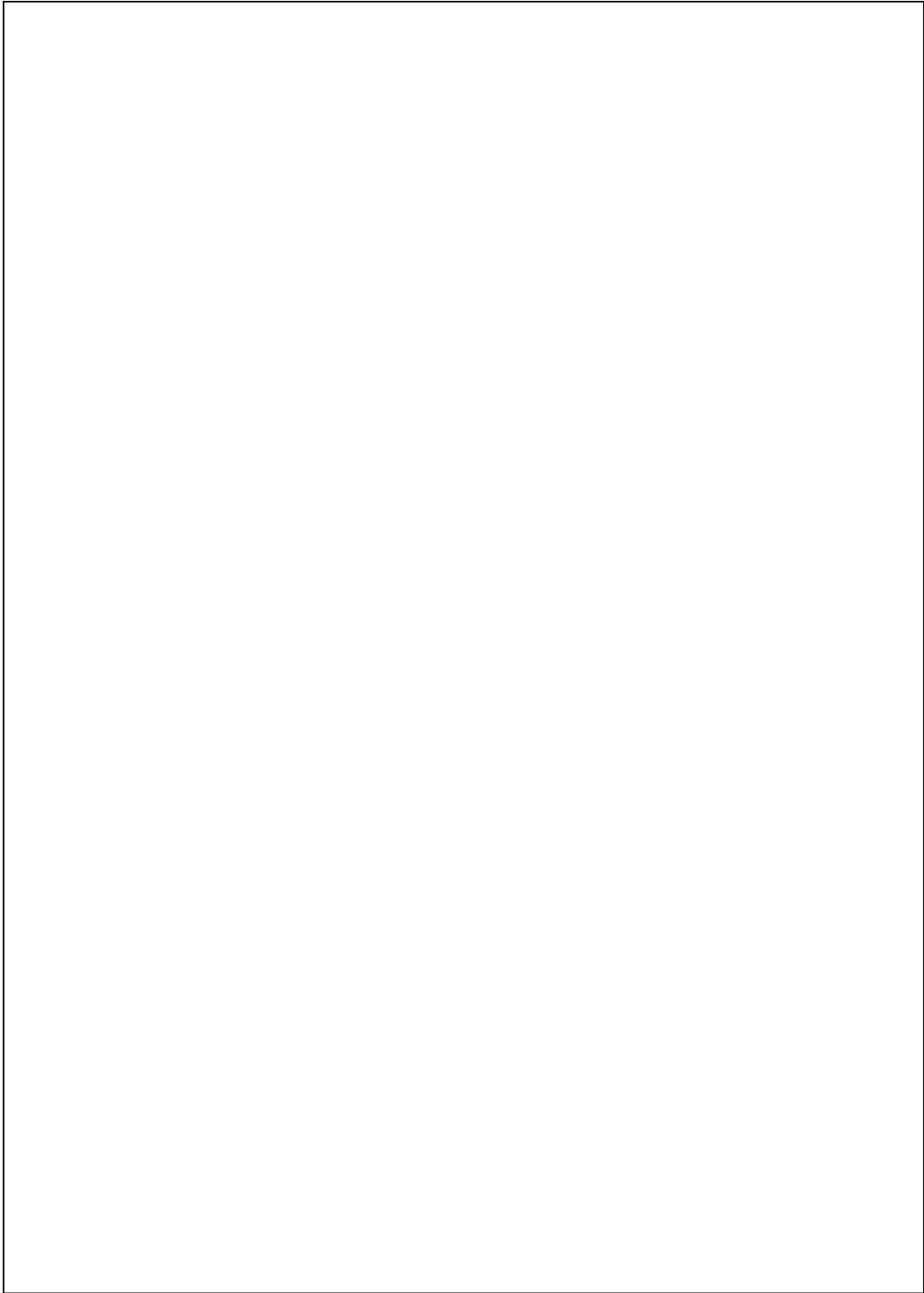
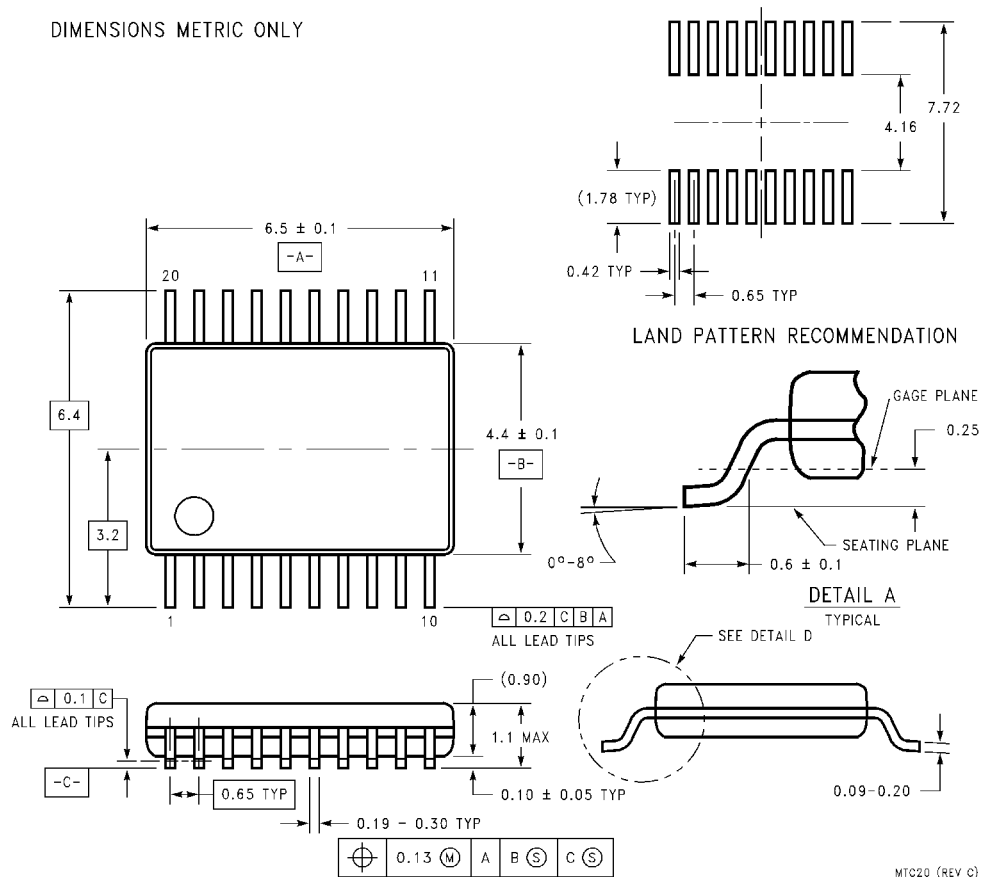


FIGURE 5. Fastlock PLL Architecture



Physical Dimensions inches (millimeters) unless otherwise noted

DIMENSIONS METRIC ONLY



20-Lead (0.173" Wide) Thin Shrink Small Outline Package (TM)
Order Number LMX2330LTM, LMX2331LTM or LMX2332LTM
 * For Tape and Reel (2500 units per reel)
Order Number LMX2330LTMX, LMX2331LTMX or LMX2332LTMX
NS Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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LMX2350/LMX2352 PLLatinum™ Fractional N RF / Integer N IF Dual Low Power Frequency Synthesizer

LMX2350 2.5 GHz/550 MHz
LMX2352 1.2 GHz/550 MHz

2352 family features very low current consumption; typically LMX2350 (2.5 GHz) 7.0 mA, LMX2352 (1.2 GHz) 5.5 mA at 3.0V. The LMX2350/2352 are available in a 24-pin TSSOP surface mount plastic package.

General Description

The LMX2350/2352 is part of a family of monolithic integrated fractional N/ Integer N frequency synthesizers designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using National's 0.5µ ABIC V silicon BiCMOS process. The LMX2350/2352 contains dual modulus prescalers along with modulo 15 or 16 fractional compensation circuitry in the RF divider. A 16/17 or 32/33 prescale ratio can be selected for the LMX2350, and the LMX2352 provides 8/9 or 16/17 prescale ratios. The IF circuitry for both the LMX2350 and LMX2352 contains an 8/9 prescaler, and is fully programmable. Using a fractional N phase locked loop technique, the LMX2350 /52 can generate very stable low noise control signals for UHF and VHF voltage controlled oscillators (VCO's).

For the RF PLL, a highly flexible 16 level programmable charge pump supplies output current magnitudes from 100µA to 1.6mA. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock™ mode. Serial data is transferred into the LMX2350/2352 via a three wire interface (Data, LE, Clock). Supply voltage can range from 2.7 V to 5.5 V. The LMX2350/

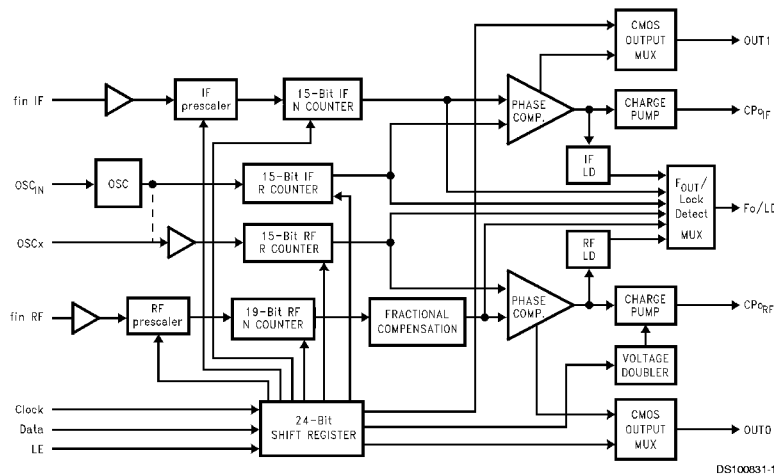
Features

- 2.7 V to 5.5 V operation
- Low current consumption
LMX2350: $I_{cc} = 7\text{mA typ at } 3\text{V}$
LMX2352: $I_{cc} = 5.5\text{mA typ at } 3\text{V}$
- Programmable or logical power down mode
 $I_{cc} = 5\text{ }\mu\text{A typ at } 3\text{V}$
- Modulo 15 or 16 fractional RF N divider supports ratios of 1, 2, 3, 4, 5, 8, 15, or 16
- Programmable charge pump current levels
RF 100µA to 1.6mA in 100µA steps
IF 100µA or 800 µA
- Digital filtered lock detect

Applications

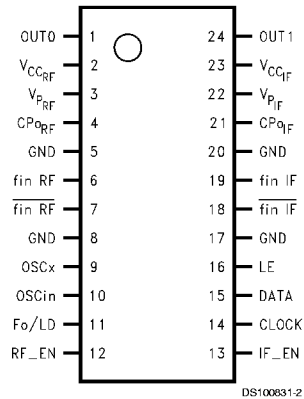
- Portable wireless communications (PCS/PCN, cordless)
- Dual mode cellular telephone systems
- Zero blind slot TDMA systems
- Spread spectrum communication systems (CDMA)
- Cable TV Tuners (CATV)

Block Diagram



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MICROWIRE™ is a trademark of National Semiconductor Corporation.
PLLatinum™ is a trademark of National Semiconductor Corporation.
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Connection Diagram



DS100831-2

Order Number LMX2350TM or LMX2352TM
NS Package Number MTC24

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	OUT0	O	Programmable CMOS output. Level of the output is controlled by IF_N [17] bit.
2	V _{ccRF}	-	RF PLL power supply voltage input. Must be equal to V _{ccIF} . May range from 2.7 V to 5.5 V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
3	V _{pRF}	-	Power supply for RF charge pump. Must be $\geq V_{ccRF}$ and V _{ccIF} .
4	CP _{oRF}	O	RF charge pump output. Connected to a loop filter for driving the control input of an external VCO.
5	GND	-	Ground for RF PLL digital circuitry.
6	fin RF	I	RF prescaler input. Small signal input from the VCO.
7	$\overline{\text{fin RF}}$	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
8	GND	-	Ground for RF PLL analog circuitry.
9	OSCx	I/O	Dual mode oscillator output or RF R counter input. Has a V _{cc} /2 input threshold when configured as an input and can be driven from an external CMOS or TTL logic gate. Can also be configured as an output to work in conjunction with OSCin to form a crystal oscillator. (See functional description 1.1 and programming description 3.1.)
10	OSCin	I	Oscillator input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit. (See functional description 1.1 and programming description 3.1.)
11	FoLD	O	Multiplexed output of N or R divider and RF/IF lock detect. Active High/Low CMOS output except in analog lock detect mode. (See programming description 3.1.5.)
12	RF_EN	I	RF PLL Enable. Powers down RF N and R counters, prescaler, and will TRI-STATE the charge pump output when LOW. Bringing RF_EN high powers up RF PLL depending on the state of RF_CTL_WORD. (See functional description 1.9.)
13	IF_EN	I	IF PLL Enable. Powers down IF N and R counters, prescaler, and will TRI-STATE the charge pump output when LOW. Bringing IF_EN high powers up IF PLL depending on the state of IF_CTL_WORD. (See functional description 1.9.)
14	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked into the 24-bit shift register on the rising edge.
15	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.