UT54ACS273E

Octal D-Flip-Flops with Clear

December, 2014
www.aeroflex.com/Logic
Datasheet

FEATURES

- Contains eight flip-flops with single-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers, shift registers and pattern generators
- 0.6µm CRH CMOS process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range from 3.0V to 5.5V
- Available QML Q or V processes
- 20-lead flatpack
- UT54ACS273E-SMD 5962-96578

DESCRIPTION

The UT54ACS273E is a positive-edge-triggered D-type flip-flop with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

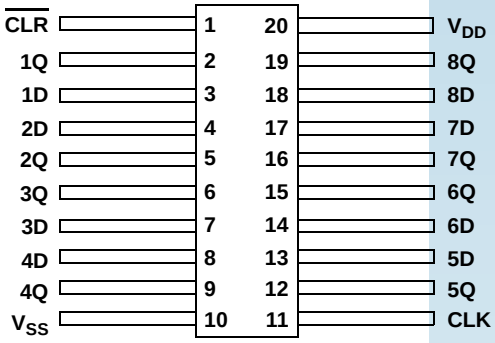
The device is characterized over full HiRel temperature range of -55°C to +125°C.

FUNCTION TABLE

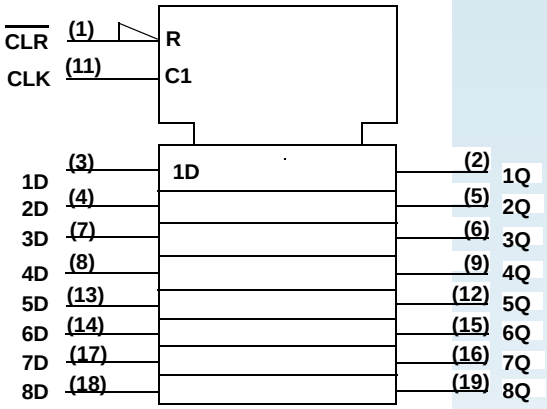
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D_X	Q_X
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No Change

PINOUT

20-Lead Flatpack
TopView

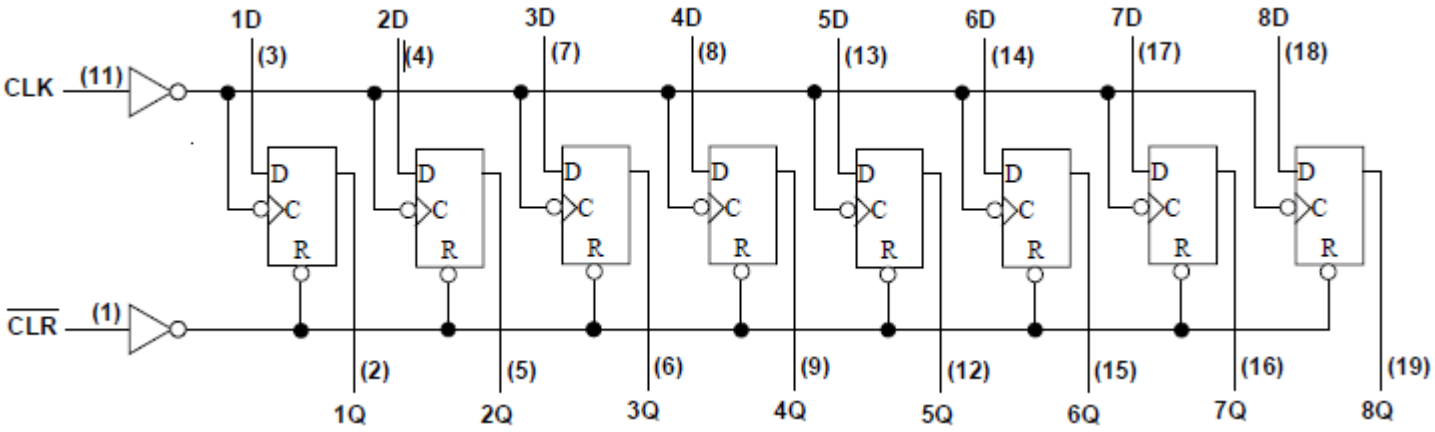


LOGIC SYMBOL



Note:
1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



OPERATIONAL ENVIRONMENT [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	108	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15	°C/W
I_I	DC input current	±10	mA
P_D[2]	Maximum package power dissipation permitted @ T_C = +125°C	3.2	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{J(max)} - T_{C(max)}) / \Theta_{JC}$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS273E[7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55°C < T_C < +125°C)

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1]	V_{DD} from3.0V to 5.5V		$0.3V_{DD}$	V
V_{IH}	High-level input voltage [1]	V_{DD} from3.0V to 5.5V	$0.7V_{DD}$		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	+1	µA
V_{OL}	Low-level output voltage [3]	I_{OL} = 100µA		0.25	V
V_{OH}	High-level output voltage [3]	I_{OH} = -100µA	V_{DD}-0.25		V
I_{OS1}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 4.5V to 5.5V	-200	+200	mA
I_{OS2}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-100	+100	mA
I_{OL1}	Low level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	+8		mA
I_{OL2}	Low level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	+6		mA
I_{OH1}	High level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2}	High level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-6		mA
P_{total1}	Power dissipation [2, 8, 10]	C_L = 50pF V_{DD} = 4.5V to 5.5V		1.5	mW/ MHz

P_{total2}	Power dissipation [2, 8, 10]	C_L = 50pF V_{DD} = 3.0V to 3.6V		0.7	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} V_{DD} from 3.0V to 5.5V		25	µA
C_{IN}	Input capacitance [5]	*f* = 1MHz V_{DD} = 0V		15	pF
C_{OUT}	Output capacitance [5]	*f* = 1MHz V_{DD} = 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/ MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.
8. Power dissipation specified per switching output.
9. Guaranteed by characterization, but not tested.
10. Power does not include power contribution of any TTL output sink current.

AC ELECTRICAL CHARACTERISTICS FOR THE UT54ACS273E[2]

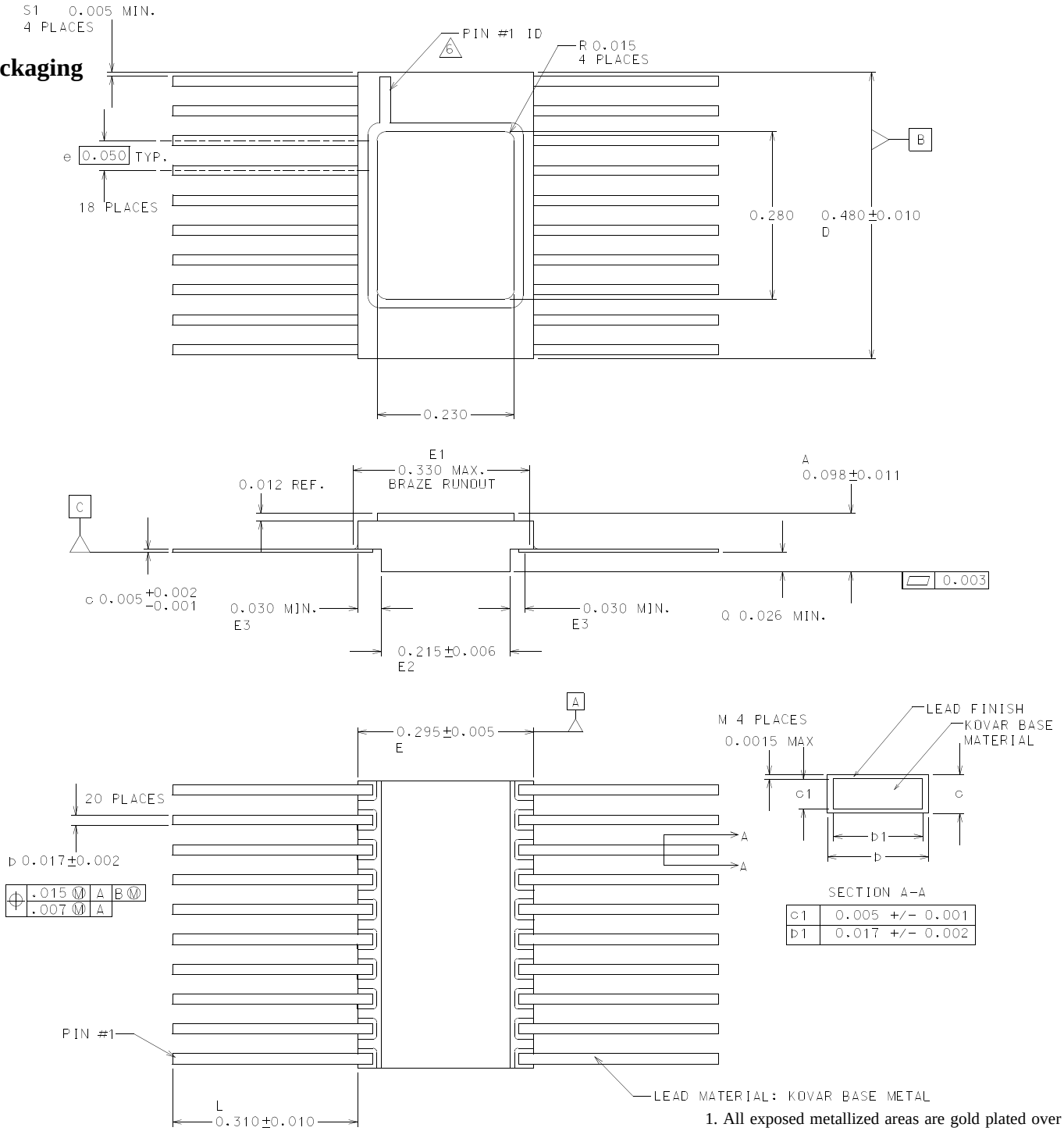
(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[1]; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	V_{DD}	MINIMUM	MAXIMUM	UNIT
t_{PLH1}	CLK to Q	C_L = 50pF	4.5V to 5.5V	4	10.5	ns
			3.0V to 3.6V	4	15.5	
t_{PHL1}	CLK to Q	C_L = 50pF	4.5V to 5.5V	4	11	ns
			3.0V to 3.6V	4	16.5	
t_{PHL2}	$\overline{CLR}$ to Q	C_L = 50pF	4.5V to 5.5V	5	12	ns
			3.0V to 3.6V	5	17	
f_{MAX}	Maximum clock frequency	C_L = 50pF	4.5V to 5.5V		83	MHz
			3.0V to 5.5V		63	
t_{SU1}	Data setup time before CLK ↑	C_L = 50pF	3.0V to 5.5V	2		ns
t_{SU2}	$\overline{CLR}$ inactive setup time before CLK↑	C_L = 50pF	3.0V to 5.5V	1		ns
t_H	Data hold time after CLK ↑	C_L = 50pF	3.0V to 5.5V	2		ns
t_{W1}	Minimum pulse width CLK high or low	C_L = 50pF	4.5V to 5.5V	4.5		ns
			3.0V to 5.5V	6.5		
t_{W2}	Minimum pulse width $\overline{CLR}$ low	C_L = 50pF	3.0V to 5.5V	4.5		ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.

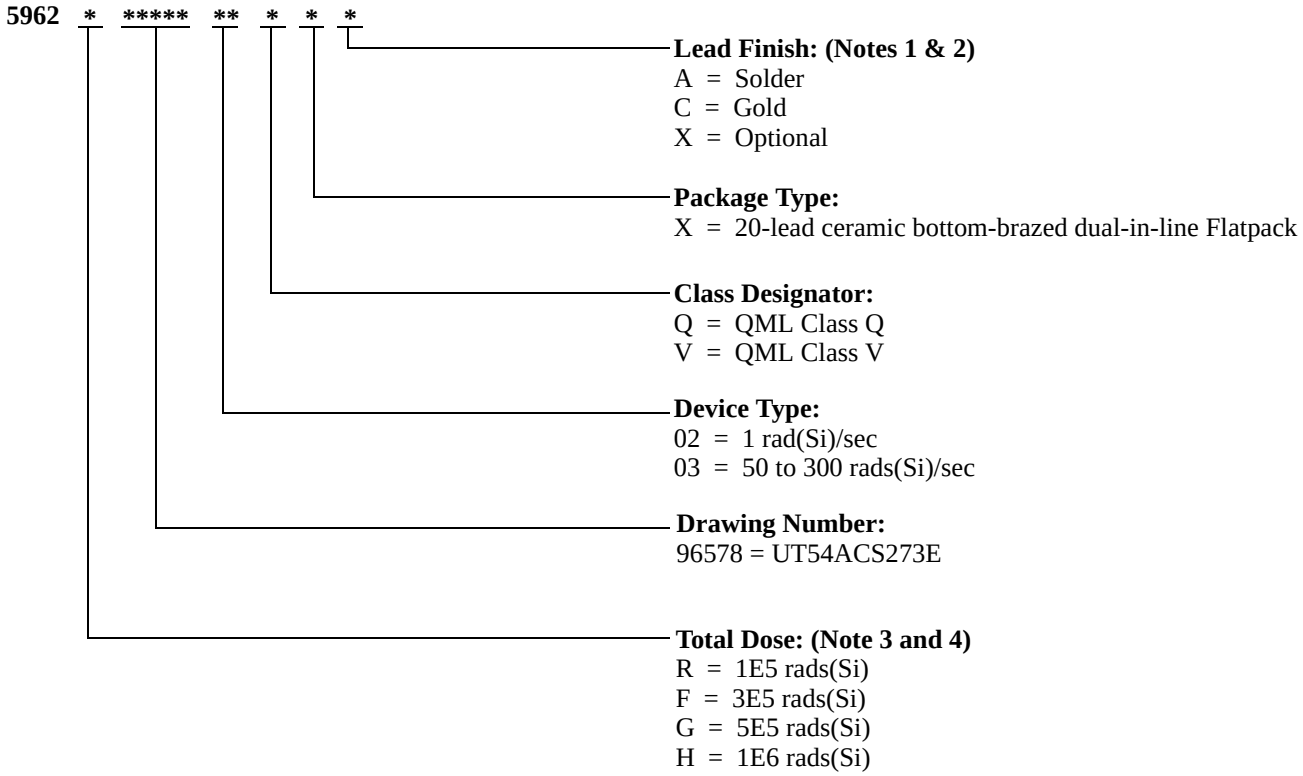
Packaging



1. All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-PRF-38535.
4. Dimension symbol is in accordance with MIL-PRF-38533.
5. Lead position and colanarity are not measured.

Figure 1. 20-lead Flatpack

Ordering Information: UT54ACS273E: SMD



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced HiRel

This product is controlled for export under the U.S. Department of Commerce (DoC). A license may be required prior to the export of this product from the United States.

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Datasheet Revision History

Revision Date	Description of Change
November 2014 Version 1.0.0	**Initial Release of Data Sheet**