

LH51256

CMOS 256K (32K × 8) Static RAM

T-46-23-14

FEATURES

- 32,768 × 8 bit organization
- Access times:
100/120 ns (MAX.)
- Power consumption:
Operating: 248 mW (MAX.)
($T_A = -40$ to 85°C , minimum cycle)
Standby: 16.5 μW (MAX.)
($T_A = 0$ to 60°C)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
28-pin, 600-mil DIP
28-pin, 450-mil SOP

DESCRIPTION

The LH51256 is a 256K bit static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

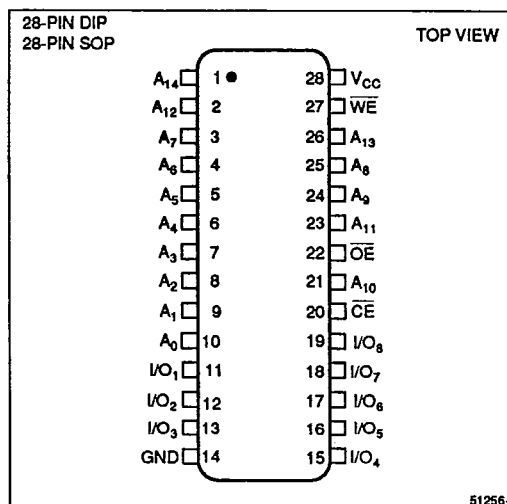


Figure 1. Pin Connections for DIP
and SOP Packages

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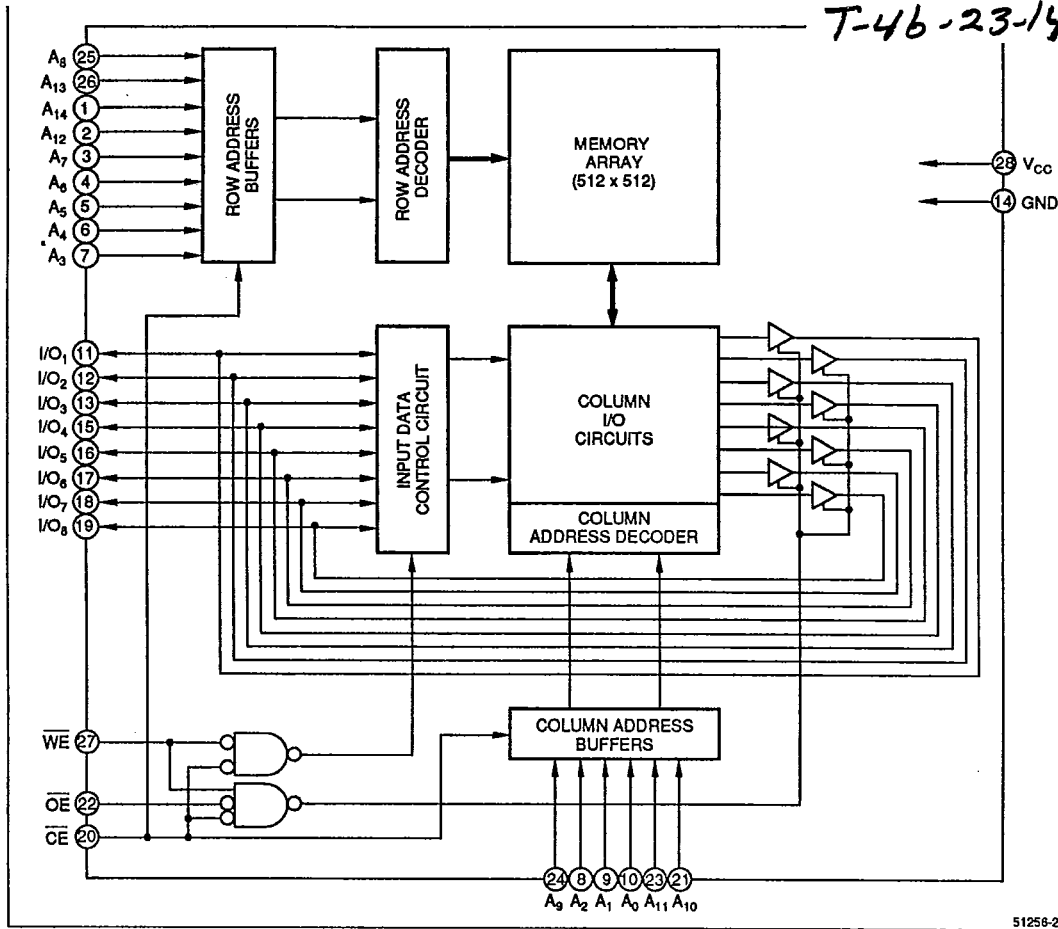


Figure 2. LH51256 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₄	Address Input
CE	Chip Enable input
WE	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data I/O
V _{cc}	Power supply
GND	Ground

TRUTH TABLE

CE	WE	OE	MODE	I/O ₁ - I/O ₈	I _{cc}	NOTE
H	X	X	Non selected	High-Z	Standby (I _{sb})	1
L	L	X	Write	Data in	Operating (I _{cc})	1
L	H	L	Read	Data out	Operating (I _{cc})	
L	H	H	Output disable	High-Z	Operating (I _{cc})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	-0.3 to +7.0	V	1
Input voltage	V _{IN}	-0.3 to +7.0	V	1
Operating temperature	T _{opr}	-40 to +85	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input voltage	V _{IH}	2.2		V _{CC} + 0.3	V
	V _{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I _{LI}	V _{CC} = 5.5V, V _{IN} = 0 to V _{CC}			1	μA
Output leakage current	I _{LO}	$\overline{CE}$ or $\overline{OE}$ = V _{IH} , V _{IO} = 0 to V _{CC}			1	μA
Operating current	I _{CC}	$\overline{CE}$ = V _{IL} , Outputs open			45	mA
Standby current	I _{SB1}	$\overline{CE}$ = V _{IH}			10	mA
	I _{SB}	$\overline{CE} \geq V_{CC} - 0.2$ V, T _A = 0 to +60°C			3	μA
		$\overline{CE} \geq V_{CC} - 0.2$ V, T _A = -40 to +85°C			10	μA
Output voltage	V _{OL}	I _{OL} = 2.1 mA			0.4	V
	V _{OH}	I _{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10		LH51256/N-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	100		120		ns	
Address access time	t _{AA}		100		120	ns	
$\overline{CE}$ access time	t _{ACE}		100		120	ns	
Output enable time	t _{OE}		50		60	ns	
Output hold time	t _{OH}	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t _{LZ}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t _{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t _{HZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t _{OHZ}	0	30	0	30	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

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2) WRITE CYCLE ($V_{CC} = 5V \pm 10\%$, $T_A = -40$ to $+85^\circ\text{C}$)

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PARAMETER	SYMBOL	LH51256/N-10		LH51256/N-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	100		120		ns	
$\overline{\text{CE}}$ Low to end of write	t _{CLW}	90		100		ns	
Address valid to end of write	t _{AW}	90		100		ns	
Address setup time	t _{AS}	5		5		ns	
Write recovery time	t _{WR}	15		15		ns	
Write pulse width	t _{WP}	50		50		ns	
Input data setup time	t _{DW}	30		30		ns	
Input data hold time	t _{DH}	10		10		ns	
$\overline{\text{WE}}$ High to output active	t _{OW}	0		0		ns	1
$\overline{\text{WE}}$ Low to output in High-Z	t _{WZ}	0	30	0	30	ns	1
$\overline{\text{OE}}$ High to output in High-Z	t _{OHZ}	0	30	0	30	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ± 500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C _L = 100 pF (Includes scope and jig capacitance)

CAPACITANCE ¹ ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C _{IN}	V _{IN} = 0 V			7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS ($T_A = -40$ to $+85^\circ\text{C}$ except as noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V _{CCDR}	$\overline{\text{CE}} \geq V_{CCDR} - 0.2\text{V}$	2.0			V	
Data retention current	I _{CCDR}	V _{CCDR} = 3 V $\overline{\text{CE}} \geq V_{CCDR} - 0.2\text{V}$, $T_A = 0$ to $+60^\circ\text{C}$, V _{IN} = 0 to V _{CCDR}			1	μA	
		V _{CCDR} = 3 V $\overline{\text{CE}} \geq V_{CCDR} - 0.2\text{V}$, $T_A = -40$ to $+85^\circ\text{C}$, V _{IN} = 0 to V _{CCDR}			6	μA	
$\overline{\text{CE}}$ setup time	t _{CDR}		0			ns	
$\overline{\text{CE}}$ hold time	t _H		t _{RC}			ns	1

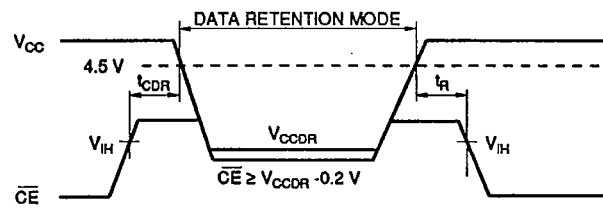
NOTE:

1. t_{RC} = Read cycle time

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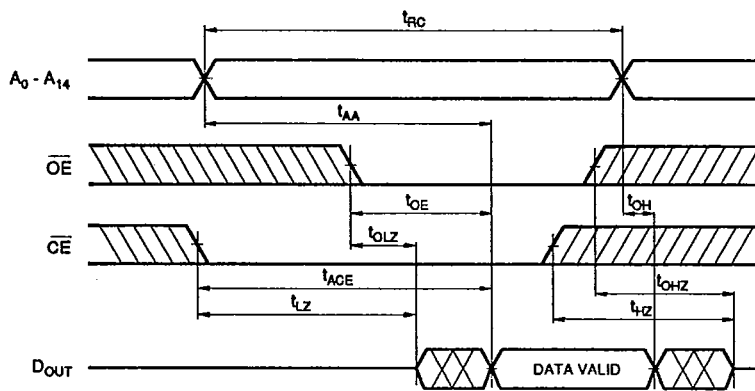
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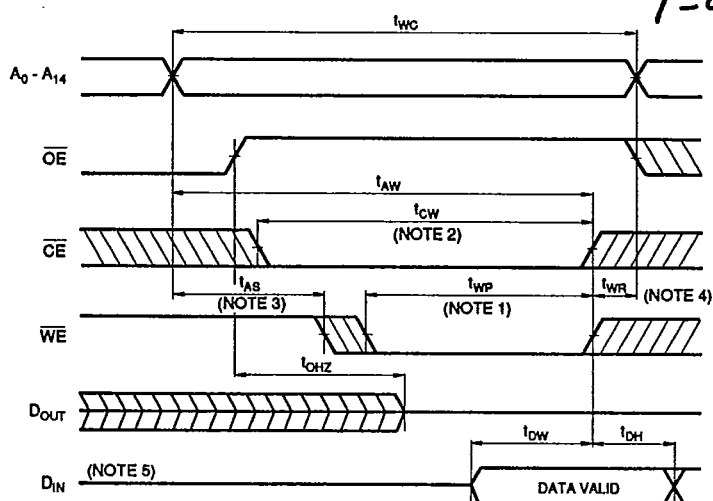
Figure 3. Low Voltage Data Retention

NOTE: $\overline{WE} = \text{"HIGH"}$

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Figure 4. Read Cycle

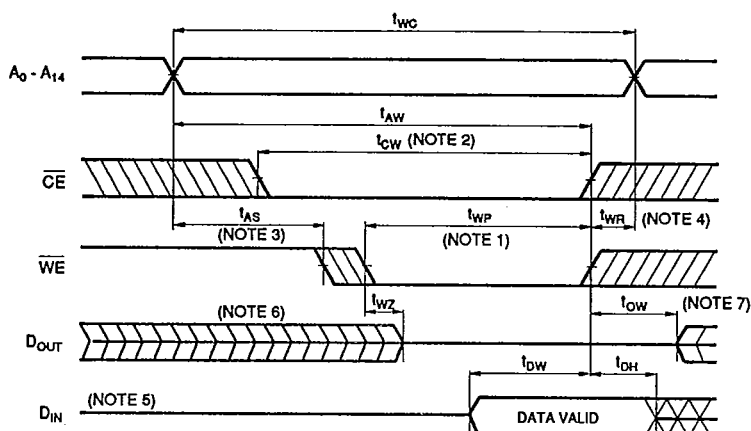
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NOTES:

1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE} = \text{LOW}$ and $\overline{WE} = \text{LOW}$.
2. t_{CW} is defined as the time from the $\overline{CE}$ low transition to the end of write.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)

NOTES:

1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE} = \text{LOW}$ and $\overline{WE} = \text{LOW}$.
2. t_{CW} is defined as the time from the $\overline{CE}$ low transition to the end of write.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

ORDERING INFORMATION

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LH51256 Device Type	X Package	- ## Speed	
		┌ 10 100 └ 12 120	Access Time (ns)
			┌ Blank 28-pin, 600-mil DIP (DIP28-P-600) └ N 28-pin, 450-mil SOP (SOP28-P-450)
CMOS 256K (32K x 8) Static RAM			

Example: LH51256N-10 (CMOS 256K (32K x 8) Static RAM, 100 ns, 28-pin, 450-mil SOP)

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