PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

M5M29KB/T800AVP

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 5.0V-ONLY, BLOCK ERASE FLASH MEMORY

DESCRIPTION

The MITSUBISHI Mobile FLASH M5M29KB/T800AVP is 5.0V-only high speed 8,388,608-bit CMOS boot block Flash Memories with alternating BGO (Back Ground Operation) feature. The BGO feature of the device allows Program or Erase operations to be performed in one bank while the device simultaneously allows Read operations to be performed on the other bank. This BGO feature is suitable for mobile and personal computing, and communication products. The M5M29KB/T800AVP is fabricated by CMOS technology for the peripheral circuits and DINOR(Divided bit line NOR) architecture for the memory cells, and are available in 48pin TSOP(I) .

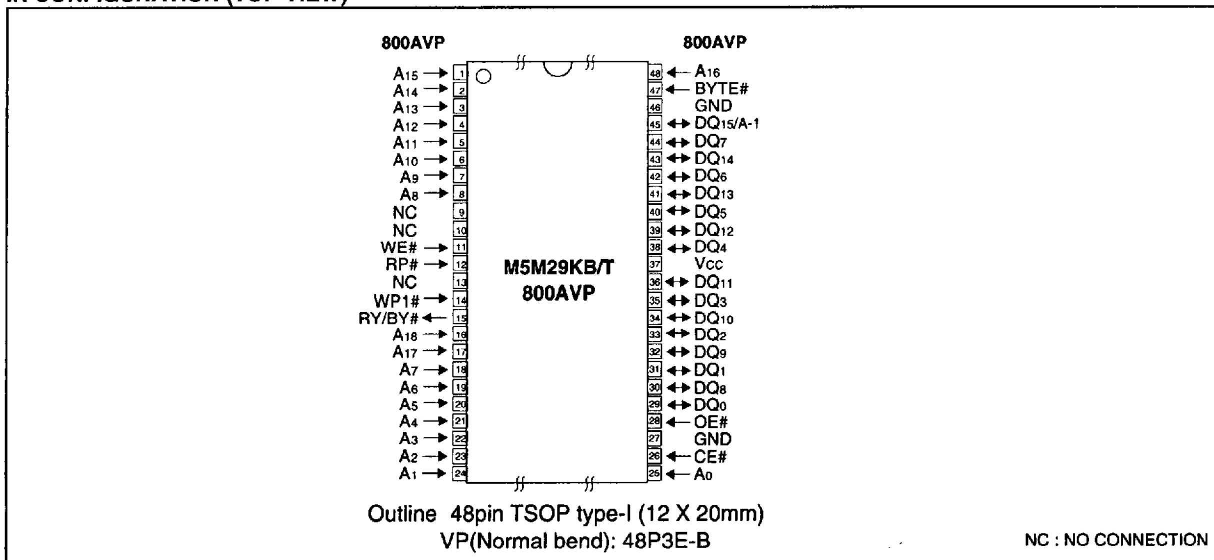
FEATURES

- Organization .... 524,288 word x 16bit
  .... 1,048,576 word x 8 bit
- Supply voltage .... Vcc = 4.5~5.5V
- Access time .... -80 80ns
  .... -11 100ns
- Power Dissipation
  - Read .... 110 mW (Max. at 5MHz)
  - (After Automatic Power saving) .... 0.25mW (typ.)
  - Program/Erase .... 220 mW (Max.)
  - Standby .... 0.25mW (typ.)
  - Deep power down mode .... 0.25mW (typ.)
- Auto program for Bank(I)
  - Program Time .... 4ms (typ.)
  - Program Unit
    - (Byte Program) 1word/1byte
    - (Page Program) 128word/256byte
- Auto program for Bank(II)
  - Program Time .... 4ms (typ.)
  - Program Unit 128word/256byte
- Auto Erase
  - Erase time .... 40 ms (typ.)
  - Erase Unit
    - Bank(I) Boot Block .... 8Kword/16Kbyte x 1
    - Parameter Block .... 4Kword/8Kbyte x 6
    - Bank(II) Main Block .... 32Kword/64Kbyte x 15
- Program/Erase cycles 100Kcycles
- Boot Block
  - M5M29KB800AVP .... Bottom Boot
  - M5M29KT800AVP .... Top Boot
- Other Functions
  - Soft Ware Command Control
  - Selective Block Lock
  - Erase Suspend/Resume
  - Program Suspend/Resume
  - Status Register Read
  - Alternating Back Ground Program/Erase Operation Between Bank(I) and Bank(II)
- Package
  - 48-Lead, 12mm x 20mm TSOP (type-I)

APPLICATION

Code Storage PC BIOS
Digital Cellular Phone/Telecommunication

PIN CONFIGURATION (TOP VIEW)



Outline 48pin TSOP type-I (12 X 20mm)
VP(Normal bend): 48P3E-B

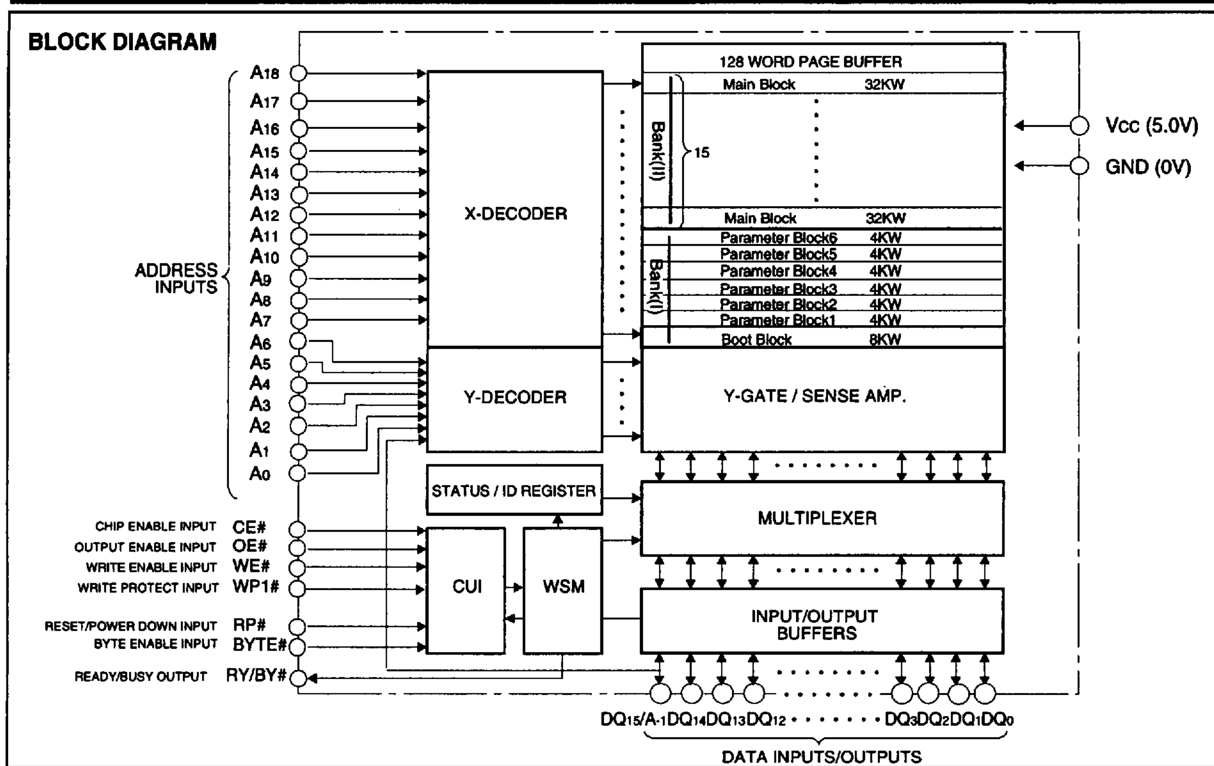
6249825 0040139 293

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 5.0V-ONLY, BLOCK ERASE FLASH MEMORY

BLOCK DIAGRAM



FUNCTION

The M5M29KB/T800AVP includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and byte/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.
A Deep Powerdown mode is enabled when the RP# pin is at GND, minimizing power consumption.

Read

The M5M29KB/T800AVP has three read modes, which accesses to the memory array, the Device Identifier and the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from deep powerdown, the M5M29KB/T800AVP automatically resets to read array mode. In the read array mode, low level input to CE# and OE#, high level input to WE# and RP#, and address signals to the address inputs (A0-A18:Word mode, A-1, A0-A18:Byte mode) output the data of the addressed location to the data input/output (D0-D15:Word mode, D0-D7:Byte mode).

Write

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. They also enable block erase and program. The CUI is written by bringing WE# to low level, while CE# is at low level and OE# is at high level. Address and data are latched on the earlier rising edge of WE# and CE#. Standard micro-processor write timings are used.

Alternating Background Operation (BGO)

The M5M29KB/T800AVP allows to read array from one bank while the other bank operates in software command write cycling or the erasing / programming operation in the background. Read array operation with the other bank in BGO is performed by changing the bank address without any additional command. When the bank address points the bank in the erasing / programming operation, the data is read out from the status register. The access time with BGO is the same as the normal read operation.

Output Disable

When OE# is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

Standby

When CE# is at VIH, the device is in the standby mode and its power consumption is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase or program, the internal control circuits remain active and the device consume normal active power until the operation completes.

Deep Power-Down

When RP# is at VIL, the device is in the deep powerdown mode and its power consumption is substantially low. During read modes, the memory is deselected and the data input/output are in a high-impedance(High-Z) state. After return from powerdown, the CUI is reset to Read Array , and the Status Register is cleared to value 80H.
During block erase or program modes, RP# low will abort either operation. Memory array data of the block being altered become invalid.

6249825 0040140 T05

Automatic Power-Saving (APS)
The Automatic Power-Saving minimizes the power consumption during read mode. The device automatically turns to this mode when any addresses or CE# isn't changed more than 200ns after the last alternation. The power consumption becomes the same as the stand-by mode. While in this mode, the output data is latched and can be read out. New data is read out correctly when addresses are changed.

SOFTWARE COMMAND DEFINITIONS
The device operations are selected by writing specific software command into the Command User Interface.

Read Array Command (FFH)
The device is in Read Array mode on initial device power up and after exit from deep powerdown, or by writing FFH to the Command User Interface. After starting the internal operation the device is set to the read status register mode automatically.

Read Device Identifier Command (90H)
Read Device Identifier Code Command(90H) is written to the command latch for reading device identifier codes. Following the command write, the manufacturer code and the device code can be read from address 0000H and 0001H, respectively.

Read Status Register Command (70H)
The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.
The contents of Status Register are latched on the later falling edge of OE# or CE#. So CE# or OE# must be toggled every status read.

Clear Status Register Command (50H)
The Erase Status, Program Status and Block Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

Block Erase / Confirm Command (20H/D0H)
Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required. The WSM executes iterative erase pulse application and erase verify operation.

Program Commands

A)Word/Byte Program (40H)
Word/Byte program is executed by a two-command sequence. The Word/Byte Program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation. The Word/Byte Program Command is Valid for only Bank(I).

B)Page Program for Data Blocks (41H)
Page Program for Bank(I) and Bank(II) allows fast programming of 128words/256bytes of data. Writing of 41H initiates the page program operation for the Data area. From 2nd cycle to 129th cycle (Word mode)/257th cycle (Byte mode), write data must be serially inputted. Address A6-A0 (Word mode)/A6-A0,A-1 (Byte mode) have to be incremented from 00H to 7FH/FFH. After completion of data loading, the WSM controls the program pulse application and verify operation.

C)Single Data Load to Page Buffer (74H)
/ Page Buffer to Flash (0EH/D0H)
Single data load to the page buffer is performed by writing 74H followed by a second write specifying the column address and data. Distinct data up to 256byte can be loaded to the page buffer by this two-command sequence. On the other hand, all of the loaded data to the page buffer is programed simultaneously by writing Page Buffer to Flash command of 0EH followed by the confirm command of D0H. After completion of programing the data on the page buffer is cleared automatically.
These commands are valid for only Bank(I) alike Word/Byte Program.

Clear Page Buffer Command (55H)
Loaded data to the page buffer is cleared by writing the Clear Page Buffer command of 55H followed by the Confirm command of D0H. This command is valid for clearing data loaded by Single Data Load to Page Buffer command.

Suspend/Resume Command (B0H/D0H)
Writing the Suspend command of B0H during block erase operation interrupts the block erase operation and allows read out from another block of memory. Writing the Suspend command of B0H during program operation interrupts the program operation and allows read out from another block of memory. The Bank address is required when writing the Suspend/Resume Command. The device continues to output Status Register data when read, after the Suspend command is written to it. Polling the WSM Status and Suspend Status bits will determine when the erase operation or program operation has been suspended. At this point, writing of the Read Array command to the CUI enables reading data from blocks other than that which is suspended. When the Resume command of D0H is written to the CUI, the WSM will continue with the erase or program processes.

DATA PROTECTION

The M5M29KB/T800AVP provides selectable block locking of memory blocks. Each block has an associated nonvolatile lock-bit which determines the lock status of the block. In addition, the M5M29KB/T800AVP has a master Write Protect pin (WP1#) which prevents any modifications to memory blocks whose lock-bits are set to "0", when WP1# is low. When WP1# is high, all blocks can be programmed or erased regardless of the state of the lock-bits, and the lock-bits are cleared to "1" by erase. See the BLOCK LOCKING table on P.8 for details.

Power Supply Voltage
When the power supply voltage (Vcc) is less than 3.2V, the device is set to the Read-only mode.
A delay time of 2 us is required before any device operation is initiated. The delay time is measured from the time Vcc reaches Vccmin (4.5V).
During power up, RP#=GND is recommended. Falling in Busy status is not recommended for possibility of damaging the device.

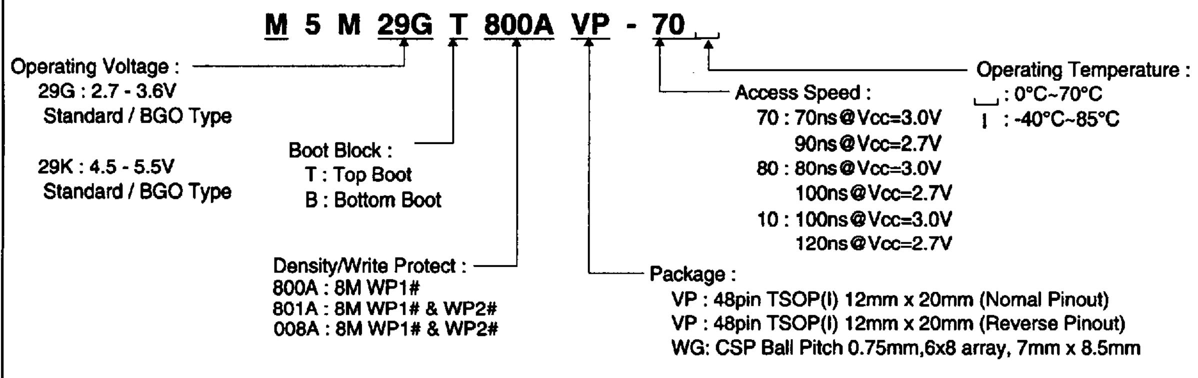
MEMORY ORGANIZATION
The M5M29KB/T800AVP has one 8Kword boot block, six 4Kword parameter blocks, for Bank(I) and fifteen 32Kword main blocks for Bank(II). A block is erased independently of other blocks in the array.

6249825 0040141 941

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 5.0V-ONLY, BLOCK ERASE FLASH MEMORY



Varied Combination

M5M29GB800AVP	-70*,80,10* -8I*,1I
M5M29GB800ARV	-70*,80,10* -8I*,1I
M5M29GT800AVP	-70*,80,10* -8I*,1I
M5M29GT800ARV	-70*,80,10* -8I*,1I
M5M29GB801AWG	(-8I specification)
M5M29GB008AWG	(-8I specification)
M5M29GT801AWG	(-8I specification)
M5M29GT008AWG	(-8I specification)
M5M29KB800AVP	-70*,80,10* -8I*,1I
M5M29KT800AVP	-70*,80,10* -8I*,1I

* : T.B.D (To Be Decided)

6249825 0040142 888

MEMORY ORGANIZATION

x8 (Bytemode)	x16 (Wordmode)	Block	Bank
F0000H-FFFFFH	78000H-7FFFFH	32Kword MAIN BLOCK	BANK(II)
E0000H-EFFFFH	70000H-77FFFH	32Kword MAIN BLOCK	BANK(II)
D0000H-DFFFFH	68000H-6FFFFH	32Kword MAIN BLOCK	BANK(II)
C0000H-CFFFFH	60000H-67FFFH	32Kword MAIN BLOCK	BANK(II)
B0000H-BFFFFH	58000H-5FFFFH	32Kword MAIN BLOCK	BANK(II)
A0000H-AFFFFH	50000H-57FFFH	32Kword MAIN BLOCK	BANK(II)
90000H-9FFFFH	48000H-4FFFFH	32Kword MAIN BLOCK	BANK(II)
80000H-8FFFFH	40000H-47FFFH	32Kword MAIN BLOCK	BANK(II)
70000H-7FFFFH	38000H-3FFFFH	32Kword MAIN BLOCK	BANK(II)
60000H-6FFFFH	30000H-37FFFH	32Kword MAIN BLOCK	BANK(II)
50000H-5FFFFH	28000H-2FFFFH	32Kword MAIN BLOCK	BANK(II)
40000H-4FFFFH	20000H-27FFFH	32Kword MAIN BLOCK	BANK(II)
30000H-3FFFFH	18000H-1FFFFH	32Kword MAIN BLOCK	BANK(II)
20000H-2FFFFH	10000H-17FFFH	32Kword MAIN BLOCK	BANK(II)
10000H-1FFFFH	08000H-0FFFFH	32Kword MAIN BLOCK	BANK(II)
0E000H-0FFFFH	07000H-07FFFH	4Kword PARAMETER BLOCK	BANK(I)
0C000H-0DFFFH	06000H-06FFFH	4Kword PARAMETER BLOCK	BANK(I)
0A000H-0BFFFH	05000H-05FFFH	4Kword PARAMETER BLOCK	BANK(I)
08000H-09FFFH	04000H-04FFFH	4Kword PARAMETER BLOCK	BANK(I)
06000H-07FFFH	03000H-03FFFH	4Kword PARAMETER BLOCK	BANK(I)
04000H-05FFFH	02000H-02FFFH	4Kword PARAMETER BLOCK	BANK(I)
00000H-03FFFH	00000H-01FFFH	8Kword BOOT BLOCK	BANK(I)
A_{18}-A_{-1}(Bytemode)	A_{18}-A_0(Wordmode)		

M5M29KB800AVP Memory Map

x8 (Bytemode)	x16 (Wordmode)	Block	Bank
FC000H-FFFFFH	7E000H-7FFFFH	8Kword BOOT BLOCK	BANK(I)
FA000H-FBFFFH	7D000H-7DFFFH	4Kword PARAMETER BLOCK	BANK(I)
F8000H-F9FFFH	7C000H-7CFFFH	4Kword PARAMETER BLOCK	BANK(I)
F6000H-F7FFFH	7B000H-7BFFFH	4Kword PARAMETER BLOCK	BANK(I)
F4000H-F5FFFH	7A000H-7AFFFH	4Kword PARAMETER BLOCK	BANK(I)
F2000H-F3FFFH	79000H-79FFFH	4Kword PARAMETER BLOCK	BANK(I)
F0000H-F1FFFH	78000H-78FFFH	4Kword PARAMETER BLOCK	BANK(I)
E0000H-EFFFFH	70000H-77FFFH	32Kword MAIN BLOCK	BANK(II)
D0000H-DFFFFH	68000H-6FFFFH	32Kword MAIN BLOCK	BANK(II)
C0000H-CFFFFH	60000H-67FFFH	32Kword MAIN BLOCK	BANK(II)
B0000H-BFFFFH	58000H-5FFFFH	32Kword MAIN BLOCK	BANK(II)
A0000H-AFFFFH	50000H-57FFFH	32Kword MAIN BLOCK	BANK(II)
90000H-9FFFFH	48000H-4FFFFH	32Kword MAIN BLOCK	BANK(II)
80000H-8FFFFH	40000H-47FFFH	32Kword MAIN BLOCK	BANK(II)
70000H-7FFFFH	38000H-3FFFFH	32Kword MAIN BLOCK	BANK(II)
60000H-6FFFFH	30000H-37FFFH	32Kword MAIN BLOCK	BANK(II)
50000H-5FFFFH	28000H-2FFFFH	32Kword MAIN BLOCK	BANK(II)
40000H-4FFFFH	20000H-27FFFH	32Kword MAIN BLOCK	BANK(II)
30000H-3FFFFH	18000H-1FFFFH	32Kword MAIN BLOCK	BANK(II)
20000H-2FFFFH	10000H-17FFFH	32Kword MAIN BLOCK	BANK(II)
10000H-1FFFFH	08000H-0FFFFH	32Kword MAIN BLOCK	BANK(II)
00000H-0FFFFH	00000H-07FFFH	32Kword MAIN BLOCK	BANK(II)
A_{18}-A_{-1}(Bytemode)	A_{18}-A_0(Wordmode)		

M5M29KT800AVP Memory Map

6249825 0040143 714

BUS OPERATIONS

Bus Operations for Word-Wide Mode (BYTE#=VIH)

Mode \ Pins		CE#	OE#	WE#	RP#	DQ0-15	RY/BY#
Read	Array	VIL	VIL	VIH	VIH	Data out	VOH (Hi-Z)
	Status Register	VIL	VIL	VIH	VIH	Status Register Data	X 1)
	Lock Bit Status	VIL	VIL	VIH	VIH	Lock Bit Data (DQ6)	X
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code	VOH (Hi-Z)
Output disable		VIL	VIH	VIH	VIH	Hi-Z	X
Stand by		VIH	X 2)	X	VIH	Hi-Z	X
Write	Program	VIL	VIH	VIL	VIH	Command/Data in	X
	Erase	VIL	VIH	VIL	VIH	Command	X
	Others	VIL	VIH	VIL	VIH	Command	X
Deep Power Down		X	X	X	VIL	Hi-Z	VOH (Hi-Z)

Bus Operations for Byte-Wide Mode (BYTE#=VIL)

Mode \ Pins		CE#	OE#	WE#	RP#	DQ0-7	RY/BY#
Read	Array	VIL	VIL	VIH	VIH	Data out	VOH (Hi-Z)
	Status Register	VIL	VIL	VIH	VIH	Status Register Data	X 1)
	Lock Bit Status	VIL	VIL	VIH	VIH	Lock Bit Data (DQ6)	X
	Identifier Code	VIL	VIL	VIH	VIH	Identifier Code	VOH (Hi-Z)
Output disable		VIL	VIH	VIH	VIH	Hi-Z	X
Stand by		VIH	X 2)	X	VIH	Hi-Z	X
Write	Program	VIL	VIH	VIL	VIH	Command/Data in	X
	Erase	VIL	VIH	VIL	VIH	Command	X
	Others	VIL	VIH	VIL	VIH	Command	X
Deep Power Down		X	X	X	VIL	Hi-Z	VOH (Hi-Z)

1) X at RY/BY# is VOL or VOH(Hi-Z).
*The RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation.
A pull-up resistor of 10K-100K Ohms is required to allow the RY/BY# signal to transition high indicating a Ready WSM condition.
2) X can be VIH or VIL for control pins.

6249825 0040144 650

SOFTWARE COMMAND DEFINITION

Command List

Command	1st bus cycle			2nd bus cycle			3rd - 257th bus cycles (Byte Mode) 3rd - 129th bus cycles (Word Mode)		
	Mode	Address	Data 1) (DQ7-0) (DQ15-0)	Mode	Address	Data (DQ7-0) (DQ15-0)	Mode	Address	Data (DQ7-0) (DQ15-0)
Read Array	Write	X	FFH						
Device Identifier	Write	X	90H	Read	IA 2)	ID 2)			
Read Status Register	Write	Bank 3)	70H	Read	Bank 3)	SRD 4)			
Clear Status Register	Write	X	50H						
Clear Page Buffer	Write	X	55H	Write	X	D0H 1)			
Byte/Word Program 5)	Write	Bank(I) 5)	40H	Write	WA 6)	WD 6)			
Page Program 7)	Write	Bank 3)	41H	Write	WA0 7)	WD0 7)	Write	WAn 7)	WDn 7)
Single Data Load to Page Buffer 5)	Write	Bank(I) 5)	74H	Write	WA 6)	WD 6)			
Page Buffer to Flash 5)	Write	Bank(I) 5)	0EH	Write	WA 8)	D0H 1)			
Block Erase / Confirm	Write	Bank 3)	20H	Write	BA 9)	D0H 1)			
Suspend	Write	Bank 3)	B0H						
Resume	Write	Bank 3)	D0H						
Read Lock Bit Status	Write	X	71H	Read	BA 9)	DQ6 10)			
Lock Bit Program / Confirm	Write	Bank 3)	77H	Write	BA 9)	D0H 1)			
Erase All Unlocked Blocks 11)	Write	X	A7H	Write	X	D0H 1)			

1) In the word-wide mode, upper byte data (DQ8 - DQ15) is ignored.
2) IA = ID Code Address : A0 = VIL (Manufacturer's Code) : A0 = VIH (Device Code), ID = ID Code.
3) Bank = Bank Address (Bank(I) or Bank(II)). A18 - A15.
4) SRD = Status Register Data.
5) Byte/Word Program, Single Data Load and Page Buffer to Flash Command is valid for only Bank(I).
6) WA = Write Address, WD = Write Data.
7) WA0,WAn = Write Address, WD0,WDn = Write Data.
BYTE# = VIL : Write Address and Write Data must be provided sequentially from 00H to FFH for A6 - A-1. Page size is 256Byte (256byte x 8bit), and also A18 - A7(Block Address, Page Address) must be valid.
BYTE# = VIH : Write Address and Write Data must be provided sequentially from 00H to 7FH for A6 - A0. Page size is 128word (128word x 16bit), and also A18 - A7(Block Address, Page Address) must be valid.
8) WA = Write Address.
Upper page address, A18 - A7(Block Address, Page Address) must be valid.
9) BA = Block Address : Bank(I) : A18 - A12.
Bank(II) : A18 - A15.
10) DQ6 provides Block Lock Status, DQ6 = 1 : Block Unlock, DQ6 = 0 : Block Locked.
11) Read Status Register command (70H) is required to detect the completion of Erase All Unlocked Blocks. 70H command has to be written at least after 1.8s from issuing A7H.

6249825 0040145 597

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

BLOCK LOCKING

800A		Lock Bit (Internally)	Write Protection Provided				Note
			BANK(I)		BANK(II)	Lock Bit	
RP#	WP1#		Boot	Parameter	Data		
V_{IL}	X	X	Locked	Locked	Locked	Locked	Deep Power Down Mode
V_{IH}	V_{IL}	0	Locked	Locked	Locked	Locked	
		1	Locked	Unlocked	Unlocked	Locked	
	V_{IH}	X	Unlocked	Unlocked	Unlocked	Unlocked	All Blocks Unlocked

DQ6 provides Lock Status of each block after writing the Read Lock Status command (71H).
WP# pin must not be switched during performing Read / Write operations or WSM Busy (WSMS = 0).

STATUS REGISTER

Symbol	Status	Definition	
		"1"	"0"
SR.7 (DQ_7)	Write State Machine Status	Ready	Busy
SR.6 (DQ_6)	Suspend Status	Suspended	Operation in Progress / Completed
SR.5 (DQ_5)	Erase Status	Error	Successful
SR.4 (DQ_4)	Program Status	Error	Successful
SR.3 (DQ_3)	Block Status after Program	Error	Successful
SR.2 (DQ_2)	*Reserved*	-	-
SR.1 (DQ_1)	*Reserved*	-	-
SR.0 (DQ_0)	*Reserved*	-	-

*The RY/BY# is an open drain output pin and indicates status of the internal WSM. When low,it indicates that the WSM is Busy performing an operation. A pull-up resistor of 10K-100K Ohms is required to allow the RY/BY# signal to transition high indicating a Ready WSM condition.

*DQ3 indicates the block status after the page programming, byte/word programming and page buffer to flash. When DQ3 is "1", the page has the over-programed cell . If over-program occurs, the device is block fail. However if DQ3 is "1", please try the block erase to the block. The block may revive.

6249825 0040146 423

PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

M5M29KB/T800AVP

8,388,608-BIT (1048,576-WORD BY 8-BIT / 524,288-WORD BY16-BIT)
CMOS 5.0V-ONLY, BLOCK ERASE FLASH MEMORY

DEVICE IDENTIFIER CODE

Code \ Pins	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Hex. Data
Manufacturer Code	VIL	0	0	0	1	1	1	0	0	1CH
Device Code (-T800A)	VIH	1	1	1	1	0	0	1	0	F2H
Device Code (-B800A)	VIH	1	1	1	1	0	1	0	0	F4H

In the word-wide mode, the upper data(D15-8) is "0".
A1~A8, A10~A18, CE#,OE# = VIL, WE# = VIH, D15/A-1 = VIL (BYTE# = L)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Vcc voltage	With respect to Ground	-0.2	7.0	V
VI1	All input or output voltage except Vcc,A9,RP# 1)	With respect to Ground	-0.6	7.0	V
Ta	Ambient temperature		-40	85	°C
Tbs	Temperature under bias		-50	95	°C
Tstg	Storage temperature		-65	125	°C
I OUT	Output short circuit current			100	mA

1) Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+1.5V for periods <20ns.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CIN	Input capacitance (Address, Control Pins)	Ta = 25°C, f = 1MHz, Vin = Vout = 0V			8	pF
COUT	Output capacitance	Ta = 25°C, f = 1MHz, Vin = Vout = 0V			12	pF

DC ELECTRICAL CHARACTERISTICS (Ta = -40~ 85°C, Vcc = 4.5V ~ 5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ1)	Max	
ILI	Input leakage current	0V≤VIN≤VCC				±1.0	µA
ILO	Output leakage current	0V≤VOUT≤VCC				±10	µA
ISB1	Vcc standby current	VCC = 5.5V, VIN=VIL/VIH, CE# = RP# =WP# = VIH			100	300	µA
ISB2	Vcc standby current	VCC = 5.5V, VIN=GND or VCC, CE# = RP# = WP#= VCC±0.3V			50	100	µA
ISB3	Vcc deep powerdown current	VCC = 5.5V, VIN=VIL/VIH, RP# = VIL			100	300	µA
ISB4	Vcc deep powerdown current	VCC = 5.5V, VIN=GND or VCC, RP# =GND±0.3V			50	100	µA
ICC1	Vcc read current for Word or Byte	VCC = 5.5V, VIN=VIL/VIH, CE# = VIL, RP#=OE#=VIH, IOUT = 0mA	5MHz		10	20	mA
ICC1	Vcc read current for Word or Byte	VCC = 5.5V, VIN=VIL/VIH, CE# = VIL, RP#=OE#=VIH, IOUT = 0mA	1MHz		2	4	mA
ICC2	Vcc Write current for Word or Byte	VCC = 5.5V,VIN=VIL/VIH, CE# =WE#= VIL, RP#=OE#=VIH				30	mA
ICC3	Vcc program current	VCC = 5.5, VIN=VIL/VIH, CE# = RP# =WP# = VIH				40	mA
ICC4	Vcc erase current	VCC = 5.5V, VIN=VIL/VIH, CE# = RP# =WP# = VIH				40	mA
ICC5	Vcc suspend current	VCC = 5.5V, VIN=VIL/VIH, CE# = RP# =WP# = VIH				200	µA
VIL	Input low voltage			– 0.5		0.8	V
VIH	Input high voltage			2.0		Vcc+0.5	V
VOL	Output low voltage	IOL = 5.8mA				0.45	V
VOH1	Output high voltage	IOH = –2.5mA		0.85Vcc			V
VOH2	Output high voltage	IOH = –100µA		Vcc-0.4			V
VLKO	Low Vcc Lock-Out voltage 2)			2.5		3.5	V

All currents are in RMS unless otherwise noted.
1) Typical values at Vcc=5.0V, Ta=25°C
2) To protect against initiation of write cycle during Vcc power-up/ down, a write cycle is locked out for Vcc less than VLKO.
If Vcc is less than VLKO, Write State Machine is reset to read mode. When the Write State Machine is in Busy state, if Vcc is less than VLKO, the alteration of memory contents may occur.

6249825 0040147 36T

AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~85°C, Vcc = 4.5V ~5.5V)

Read-Only Mode

Symbol		Parameter	Limits									Unit
			M5M29KB/T800A-70			M5M29KB/T800A-80			M5M29KB/T800A-10			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tRC	tAVAV	Read cycle time	70			80			100			ns
ta (AD)	tAVQV	Address access time			70			80			100	ns
ta (CE)	tELQV	Chip enable access time			70			80			100	ns
ta (OE)	tGLQV	Output enable access time			40			40			50	ns
tCLZ	tELQX	Chip enable to output in low-Z	0			0			0			ns
tDF(CE)	tEHQZ	Chip enable high to output in high Z			25			25			25	ns
tOLZ	tGLQX	Output enable to output in low-Z	0			0			0			ns
tDF(OE)	tGHQZ	Output enable high to output in high Z			25			25			25	ns
tPHZ	tPLQZ	RP# low to output high-Z			150			150			150	ns
ta(BYTE)	tFL/HQV	BYTE# access time			70			80			100	ns
tBHZ	tFLQZ	BYTE# low to output high-Z			25			25			25	ns
tOH	tOH	Output hold from CE#, OE#, addresses	0			0			0			ns
tBCD	tELFL/H	CE# low to BYTE# high or low			5			5			5	ns
tBAD	tAVFL/H	Address to BYTE# high or low			5			5			5	ns
tOEH	tWHGL	OE# hold from WE# high	70			80			100			ns
tPS	tPHEL	RP# recovery to CE# low	500			500			500			ns

Timing measurements are made under AC waveforms for read operations.

AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~85°C, Vcc = 4.5V ~5.5V)

Write Mode (WE# control)

Symbol		Parameter	Limits									Unit
			M5M29KB/T800A-70			M5M29KB/T800A-80			M5M29KB/T800A-10			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tWC	tAVAV	Write cycle time	70			80			100			ns
tAS	tAVWH	Address set-up time	50			50			50			ns
tAH	tWHAX	Address hold time	0			0			0			ns
tDS	tDVWH	Data set-up time	50			50			50			ns
tDH	tWHDX	Data hold time	0			0			0			ns
tCS	tELWL	Chip enable set-up time	0			0			0			ns
tCH	tWHEH	Chip enable hold time	0			0			0			ns
tWP	tWLWH	Write pulse width	50			60			70			ns
tWPH	tWHWL	Write pulse width high	20			20			30			ns
tGHWL	tGHWL	OE# hold to WE# Low	70			80			100			ns
tBS	tFL/HWH	Byte enable high or low set-up time	50			50			50			ns
tBH	tWHFL/H	Byte enable high or low hold time	70			80			100			ns
tBLS	tPHHWH	Block Lock set-up to write enable high	70			80			100			ns
tBLH	tQVPH	Block Lockhold from valid SRD	0			0			0			ns
tDAP	tWHRH1	Duration of auto-program operation		4	80		4	80		4	80	ms
tDAE	tWHRH2	Duration of auto-block erase operation		40	600		40	600		40	600	ms
tWHRL	tWHRL	Write enable high to RY/BY# low			70			80			100	ns
tPS	tPHWL	RP# high recovery to write enable low	500			500			500			ns

Read timing parameters during command write operations mode are the same as during read-only operations mode.
Typical values at Vcc=5.0V, Ta=25°C

6249825 0040148 2T6

AC ELECTRICAL CHARACTERISTICS (Ta = -40 ~ 85°C, Vcc = 4.5V ~ 5.5V)

Write Mode (CE# control)

Symbol		Parameter	Limits									Unit
			M5M29KB/T800A-70			M5M29KB/T800A-80			M5M29KB/T800A-10			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tWC	tAVAV	Write cycle time	70			80			100			ns
tAS	tAVWH	Address set-up time	50			50			50			ns
tAH	tEHAX	Address hold time	0			0			0			ns
tDS	tDVWH	Data set-up time	50			50			50			ns
tDH	tEHDX	Data hold time	0			0			0			ns
tWS	tWLEL	Write enable set-up time	0			0			0			ns
tWH	tEHWH	Write enable hold time	0			0			0			ns
tCEP	tELEH	CE# pulse width	50			60			70			ns
tCEPH	tEHEL	CE# pulse width high	20			20			30			ns
tGHEL	tGHEL	OE# hold to CE# Low	70			80			100			ns
tBS	tFL/HWH	Byte enable high or low set-up time	50			50			50			ns
tBH	tEHFL/H	Byte enable high or low hold time	70			80			100			ns
tBLS	tPHHEH	Block Lock set-up to write enable high	70			80			100			ns
tBLH	tQVPH	Block Lockhold from valid SRD	0			0			0			ns
tDAP	tEHRH1	Duration of auto-program operation		4	80		4	80		4	80	ms
tDAE	tEHRH2	Duration of auto-block erase operation		40	600		40	600		40	600	ms
tEHRL	tEHRL	CE# high to RY/BY# low			70			80			100	ns
tPS	tPHEL	RP# high recovery to write enable low	500			500			500			ns

Read timing parameters during command write operation mode are the same as during read-only operation mode.
Typical values at Vcc=5.0V, Ta=25°C

Erase and Program Performance

Parameter	Min	Typ	Max	Unit
Main Block Erase Time		40	600	ms
Boot Block Erase Time		20	600	ms
Parameter Block Erase Time		16	600	ms
Main Block Write Time (Page Mode)		1.0	1.8	sec
Page Write Time		4	80	ms

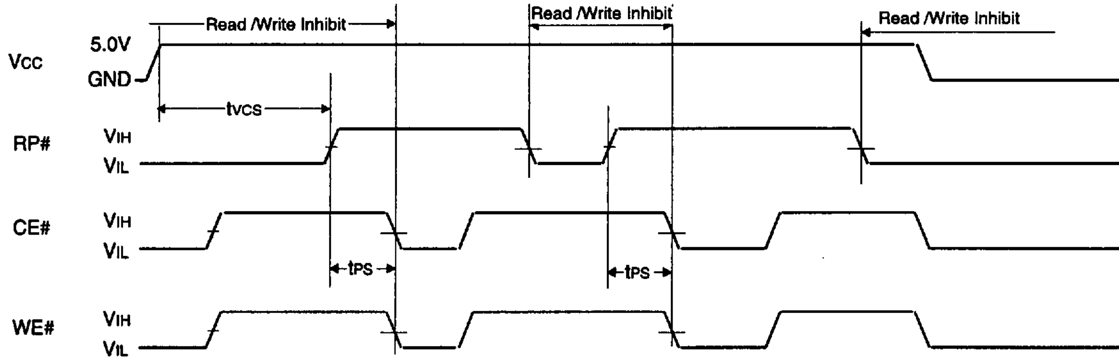
Vcc Power Up / Down Timing

Symbol	Parameter	Min	Typ	Max	Unit
tVCS	RP# =VIH set-up time from Vccmin	2			µs

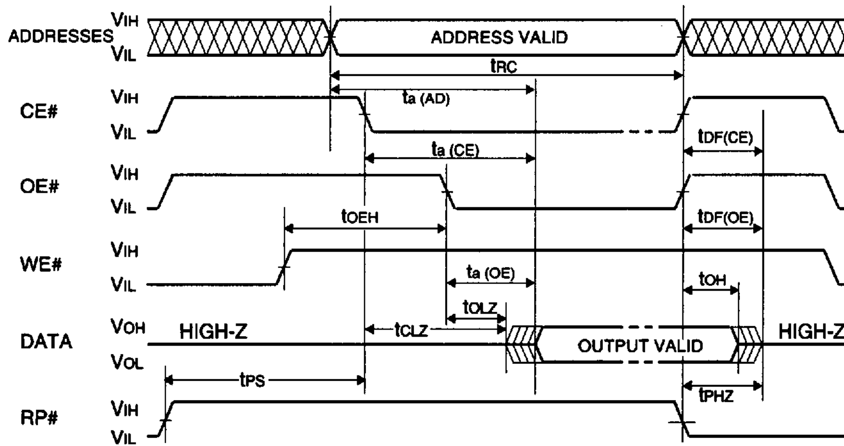
During power up/down, by the noise pulses on control pins, the device has possibility of accidental erasure or programming.
The device must be protected against initiation of write cycle for memory contents during power up/down.
The delay time of min.2µsec is always required before read operation or write operation is initiated from the time Vcc reaches Vccmin during power up/down.
By holding RP# VIL, the contents of memory is protected during Vcc power up/down.
During power up, RP# must be held VIL for min.2µs from the time Vcc reaches Vccmin.
During power down, RP# must be held VIL until Vcc reaches GND.
RP# doesn't have latch mode ,therefore RP# must be held VIH during read operation or erase/program operation.

6249825 0040149 132

Vcc POWER UP / DOWN TIMING



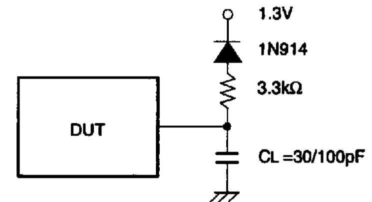
AC WAVEFORMS FOR READ OPERATION AND TEST CONDITIONS



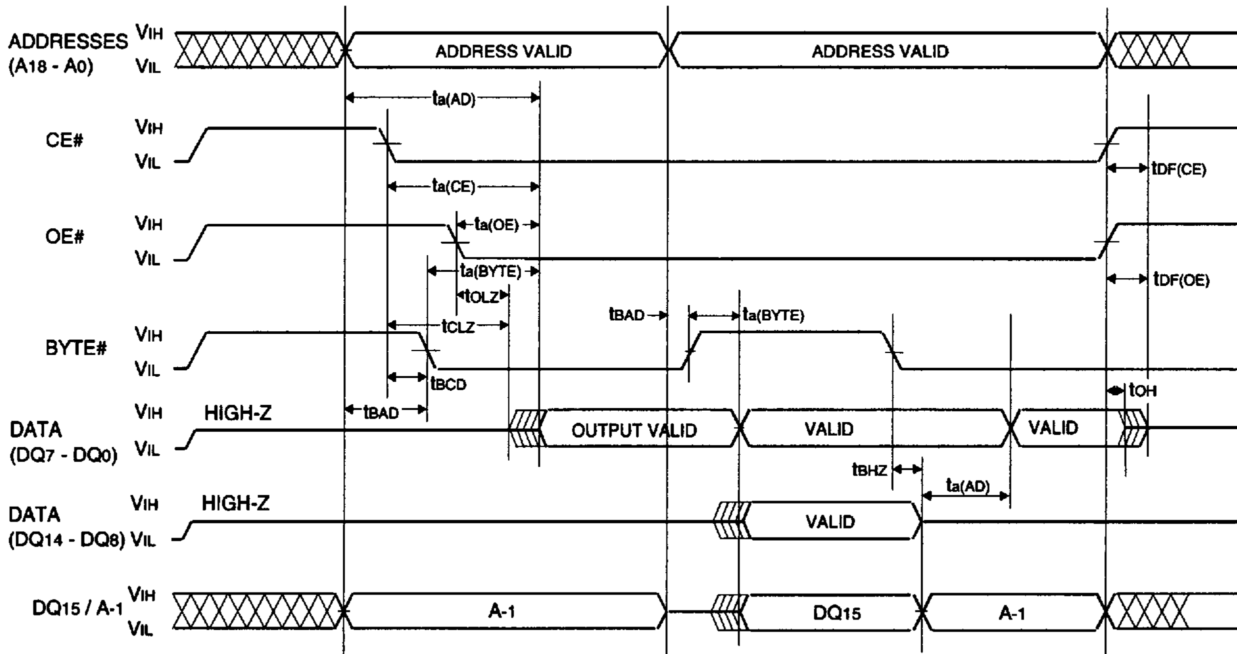
TEST CONDITIONS
FOR AC CHARACTERISTICS

Input voltage : V_{IL} = 0V, V_{IH} = 3.0V
Input rise and fall times : ≤5ns (70,80ns)
≤10ns (100ns)
Reference voltage
at timing measurement : 1.5V

Output load : 1TTL gate +
CL(100pF for 100ns)
CL(30pF for 70,80ns)
or



BYTE AC WAVEFORMS FOR READ OPERATION



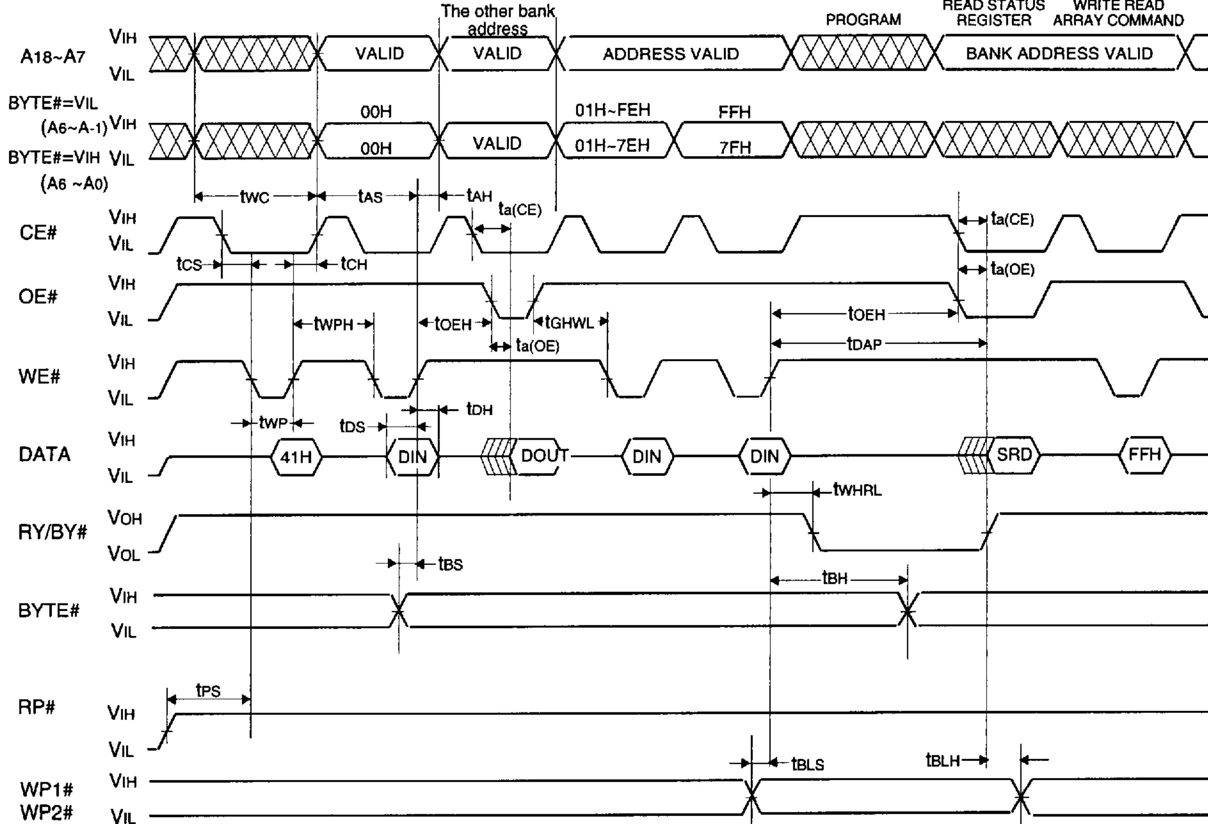
When BYTE#=V_{IH}, CE#=OE#=V_{IL} , DQ_{15}/A_{-1} is output status. At this time, input signal must not be applied.

6249825 0040150 954

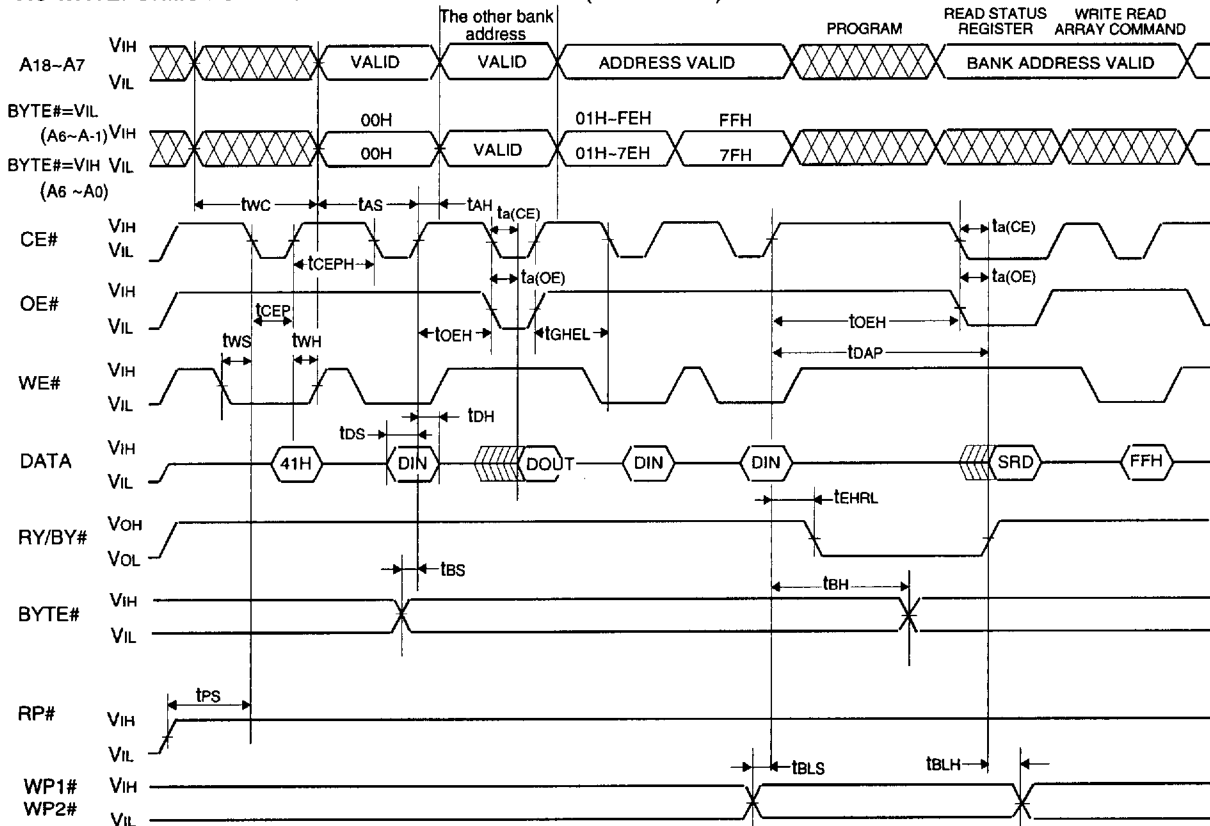
PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

AC WAVEFORMS FOR PAGE PROGRAM OPERATION (WE# control)

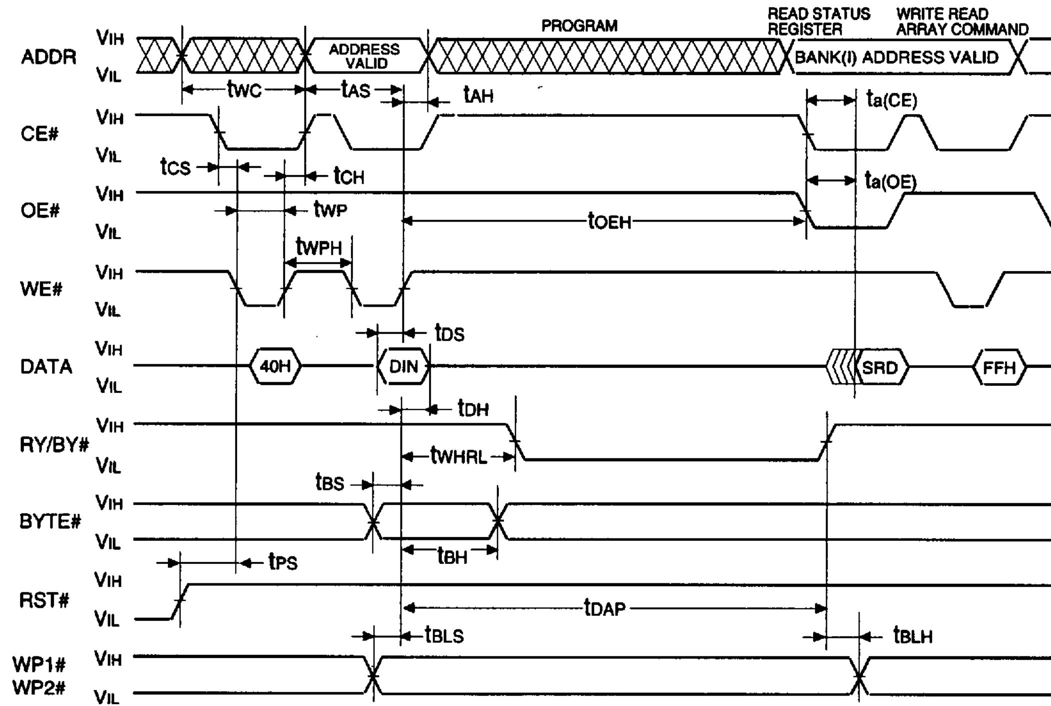


AC WAVEFORMS FOR PAGE PROGRAM OPERATION (CE# control)

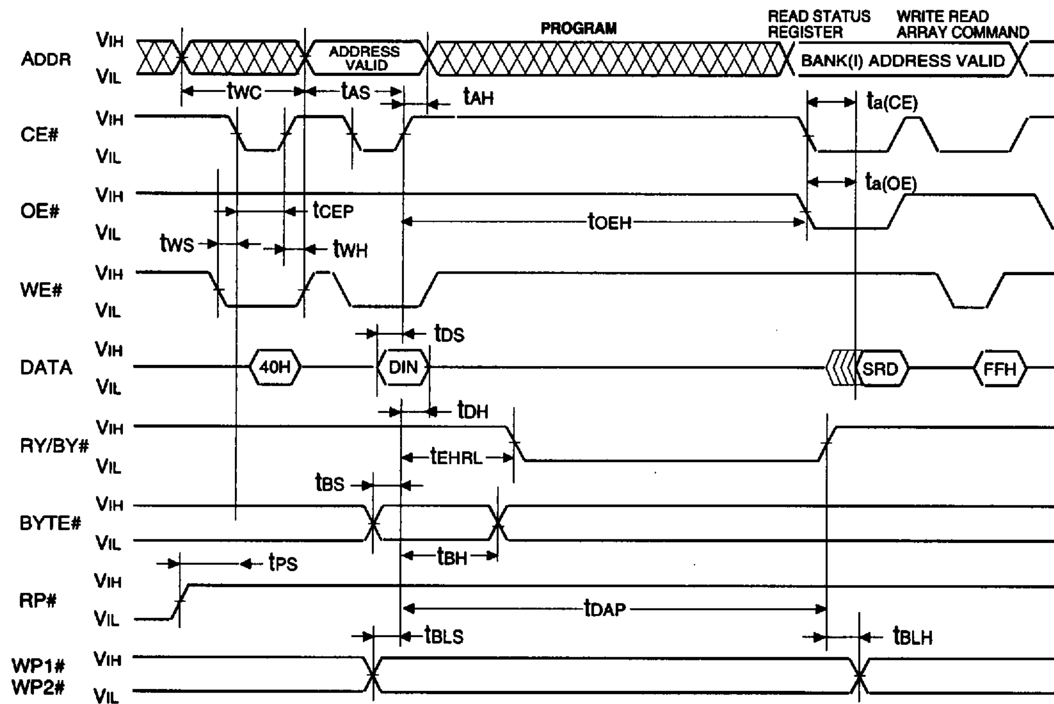


6249825 0040151 890

AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION (WE# control) (to only BANK(I))



AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION (CE# control) (to only BANK(I))



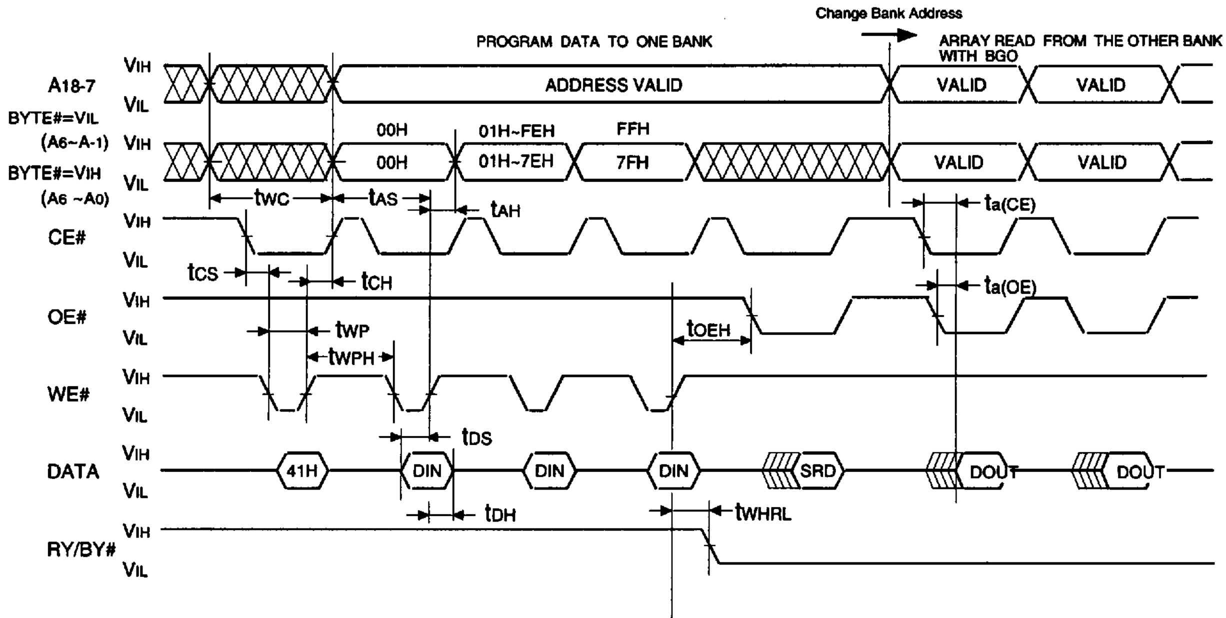
6249825 0040152 727

AC WAVEFORMS FOR ERASE OPERATIONS (WE# control)

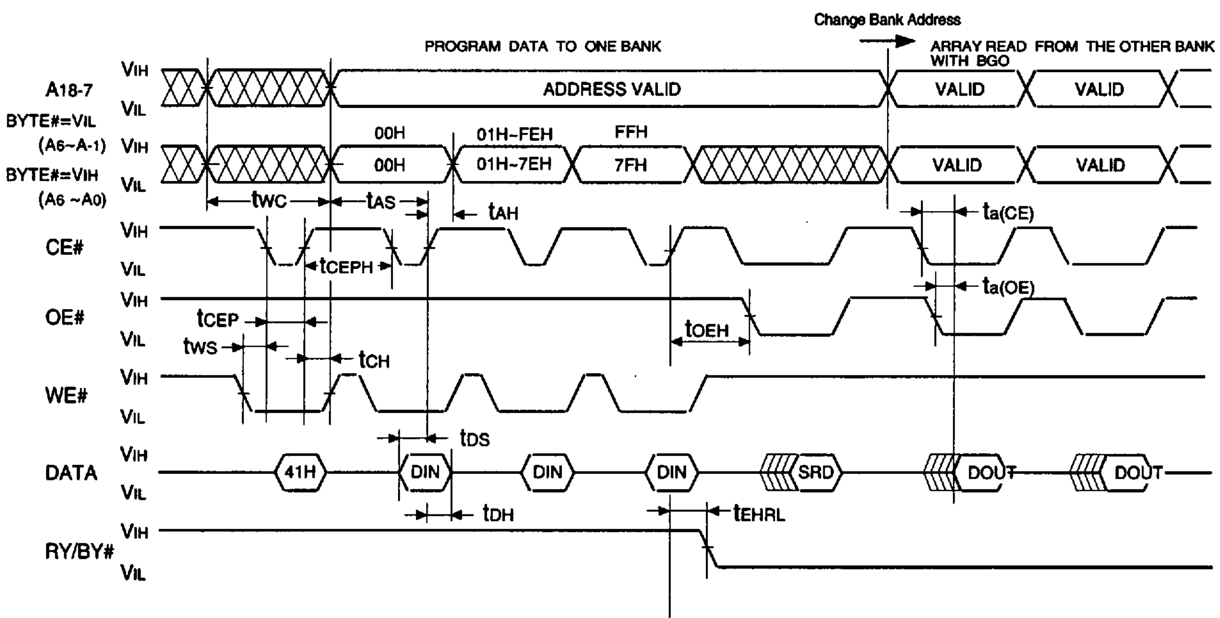
AC WAVEFORMS FOR ERASE OPERATIONS (CE# control)

6249825 0040153 663

AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (WE# control)

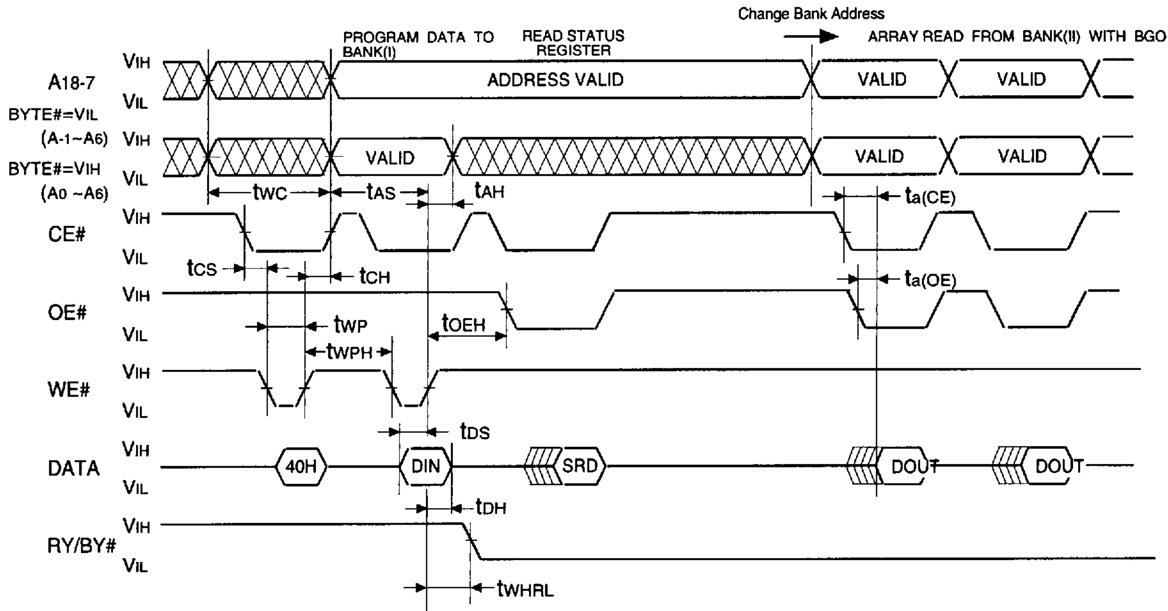


AC WAVEFORMS FOR PAGE PROGRAM OPERATION WITH BGO (CE# control)

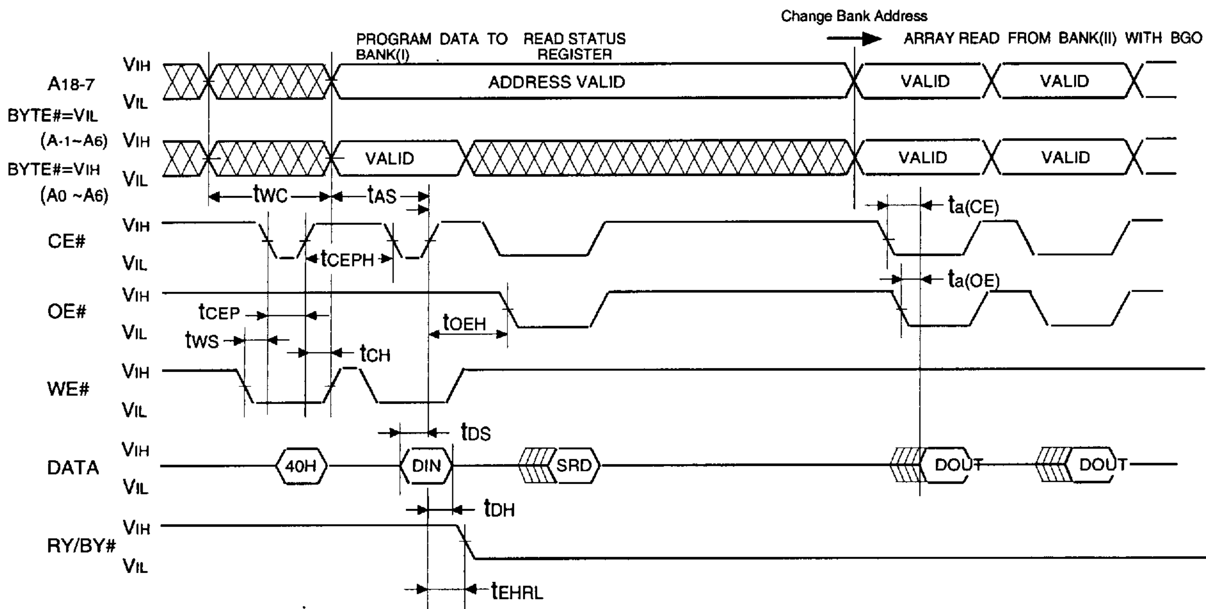


6249825 0040154 5TT

AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION WITH BGO (WE# control)

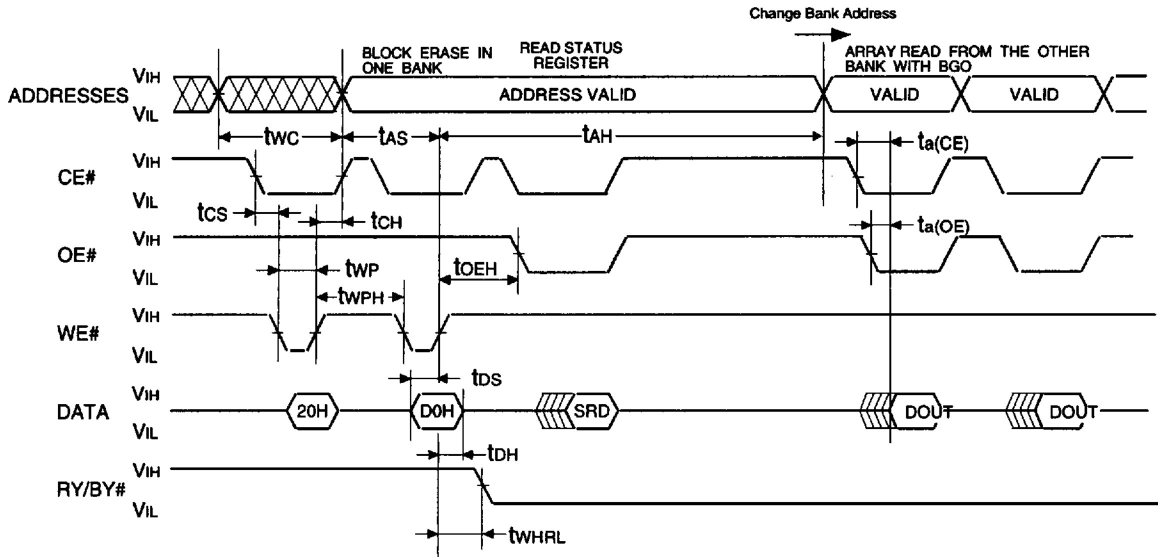


AC WAVEFORMS FOR BYTE / WORD PROGRAM OPERATION WITH BGO (CE# control)

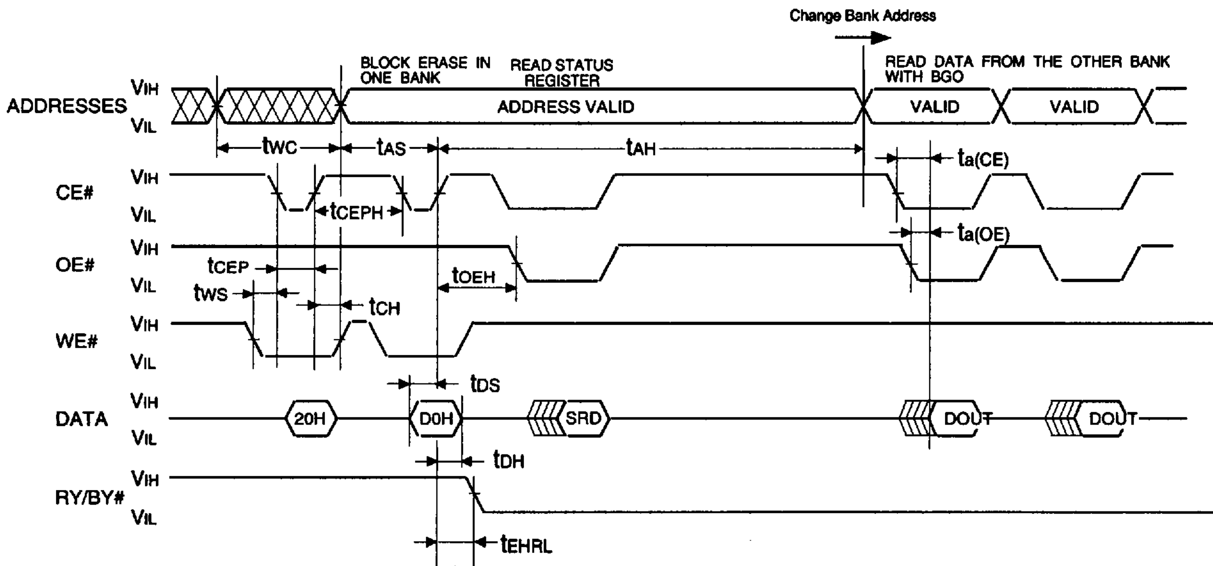


6249825 0040155 436

AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (WE# control)

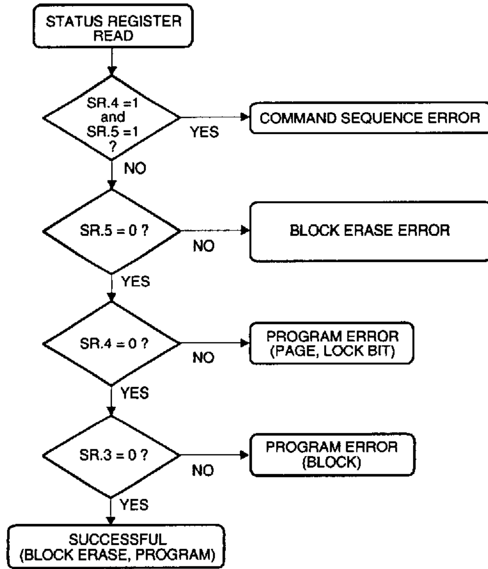


AC WAVEFORMS FOR BLOCK ERASE OPERATION WITH BGO (CE# control)

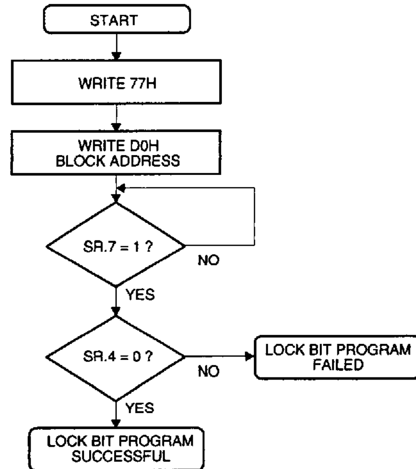


6249825 0040156 372

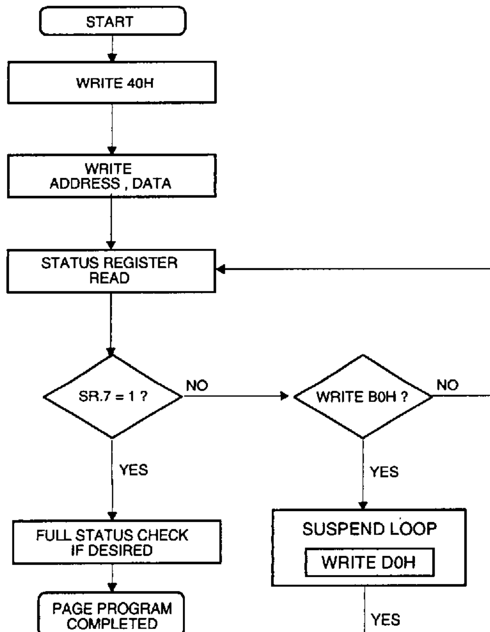
FULL STATUS CHECK PROCEDURE



LOCK BIT PROGRAM FLOW CHART

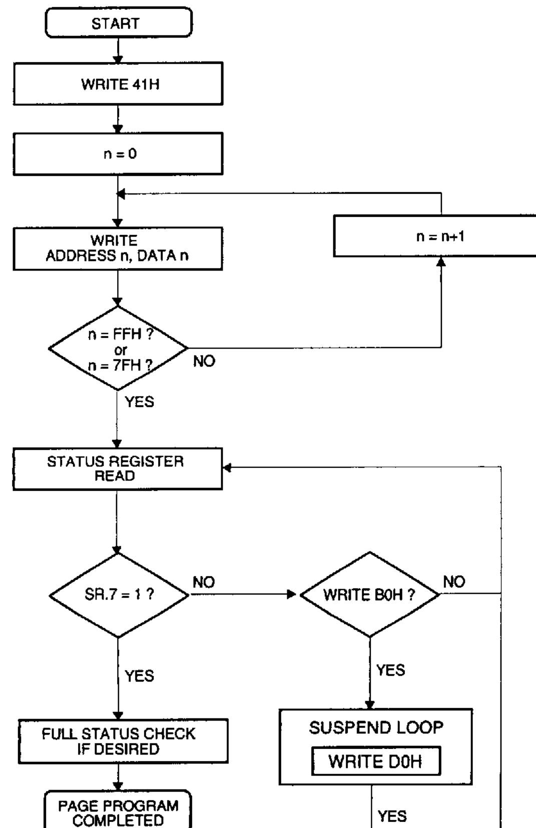


BYTE PROGRAM FLOW CHART



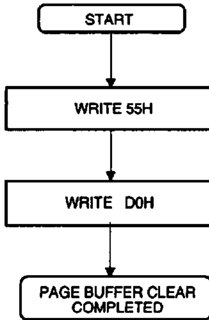
* Byte program is admitted to only BANK(I).

PAGE PROGRAM FLOW CHART

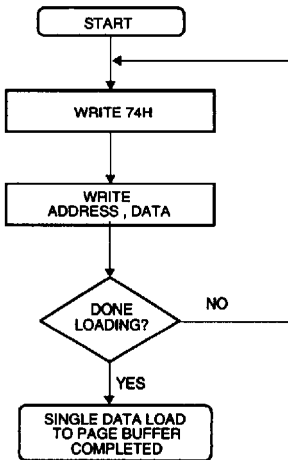


6249825 0040157 209

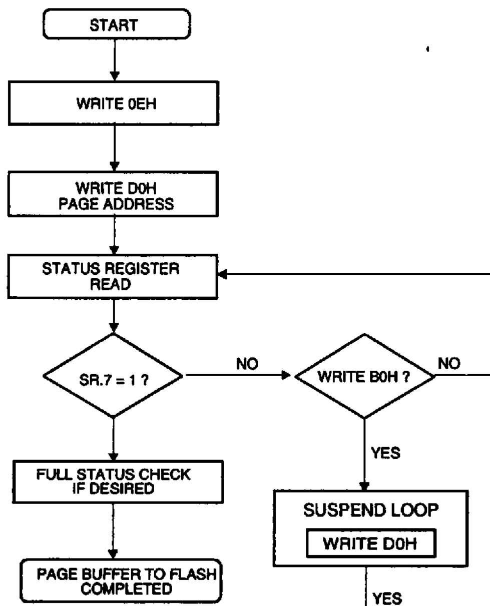
CLEAR PAGE BUFFER



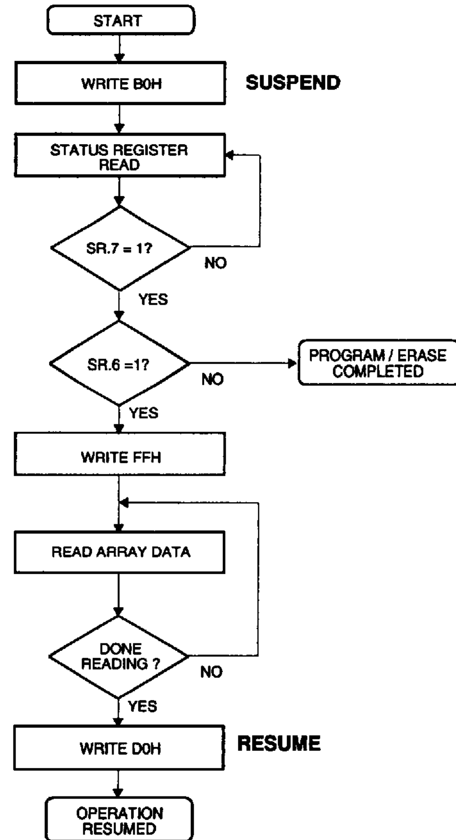
SINGLE DATA LOAD TO PAGE BUFFER



PAGE BUFFER TO FLASH

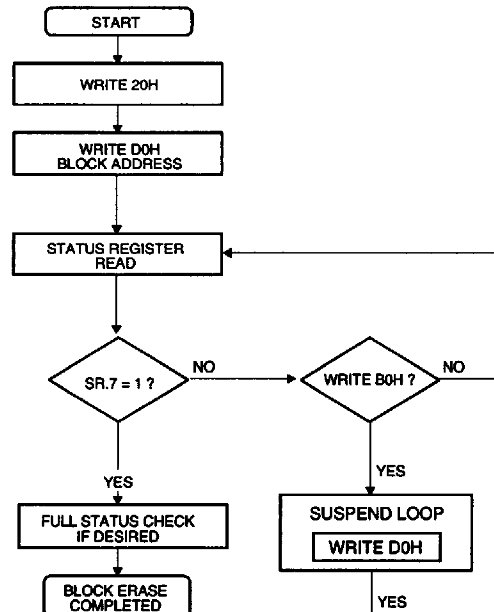


SUSPEND / RESUME FLOW CHART



* The bank address is required when writing this command. Also, there is no need to suspend the erase or program operation when reading data from the other bank.

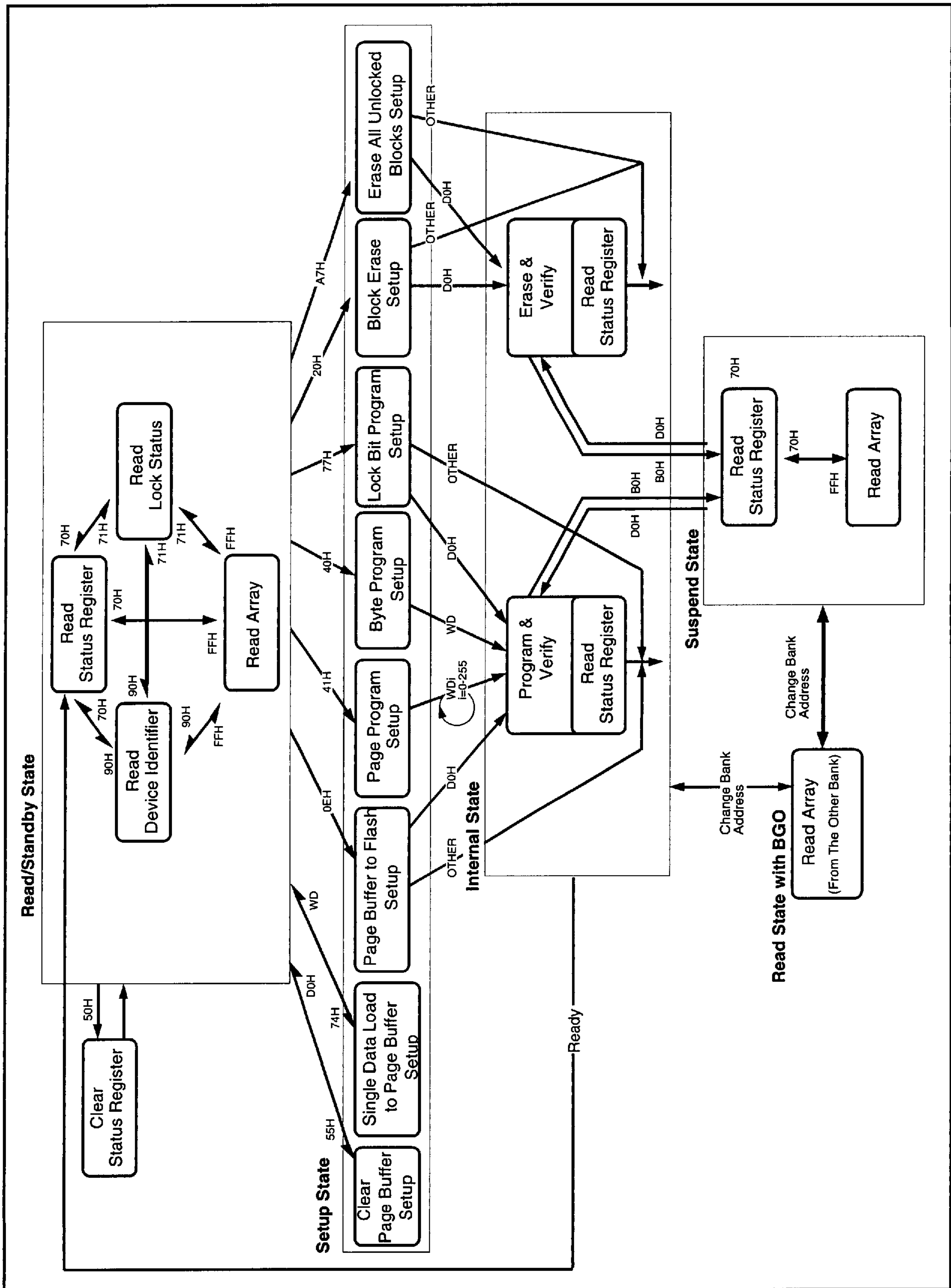
BLOCK ERASE FLOW CHART



PRELIMINARY

Notice : This is not a final specification.
Some parametric limits are subject to change.

OPERATION STATUS and EFFECTIVE COMMAND



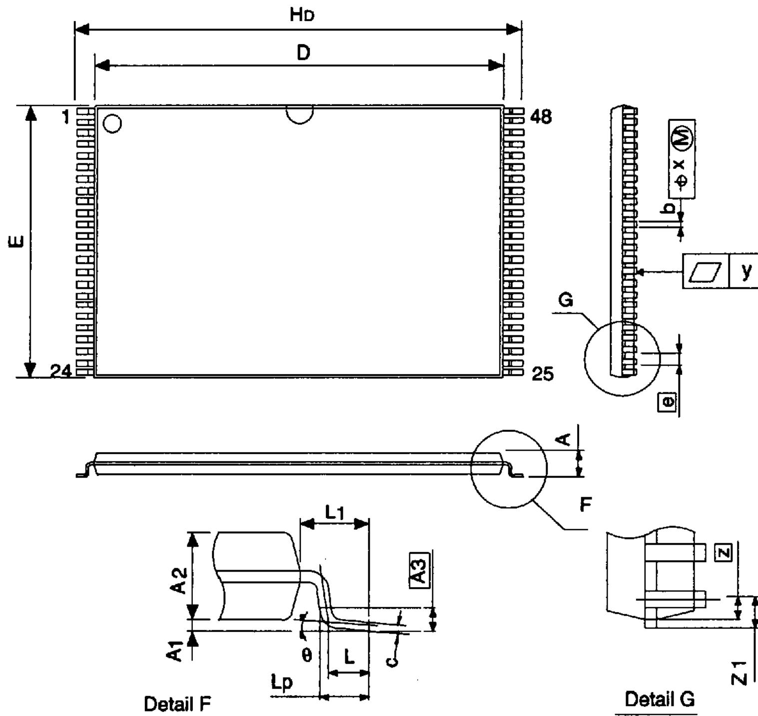
6249825 0040159 081

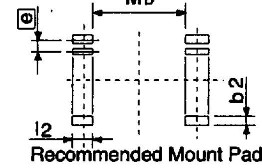
PACKAGE DIMENSIONS 48P3E (48pin 12 x 20 mm TSOP(I))

48P3E-B

Plastic 48pin 12x20mm TSOP(I)

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
TSOP I 48-P-1220-0.50	—		Cu Alloy





Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.2
A1	0.05	0.125	0.2
A2	—	1.0	—
b	0.15	0.2	0.3
c	0.105	0.125	0.175
D	18.3	18.4	18.5
E	11.9	12.0	12.1
e	—	0.5	—
HD	19.8	20.0	20.2
L	0.4	0.5	0.6
L1	—	0.8	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
Z	—	0.25	—
Z1	—	—	0.4
x	—	—	0.1
y	—	—	0.1
θ	0°	—	10°
b2	—	0.225	—
l2	0.9	—	—
MD	—	18.6	—

6249825 0040160 8T3

67479