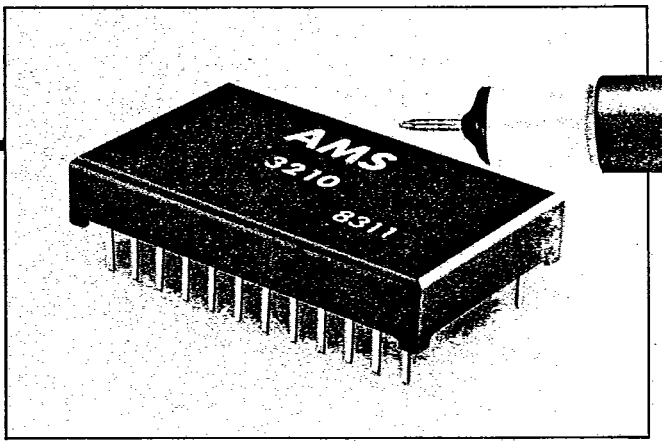
aptek microsystems

AMS 3210



Small, wide dynamic range DTMF Receiver

DESCRIPTION

Combines the latest advances in CMOS/LSI technology with the stability and accuracy inherent in hybrids. CMOS switched capacitor filter technology, for tone decoder, plus proven hybrid technology, provides rugged input protection, stable gain setting, high dial tone rejection. Combination results in a unit easy to use and which will perform to specifications throughout its lifetime.

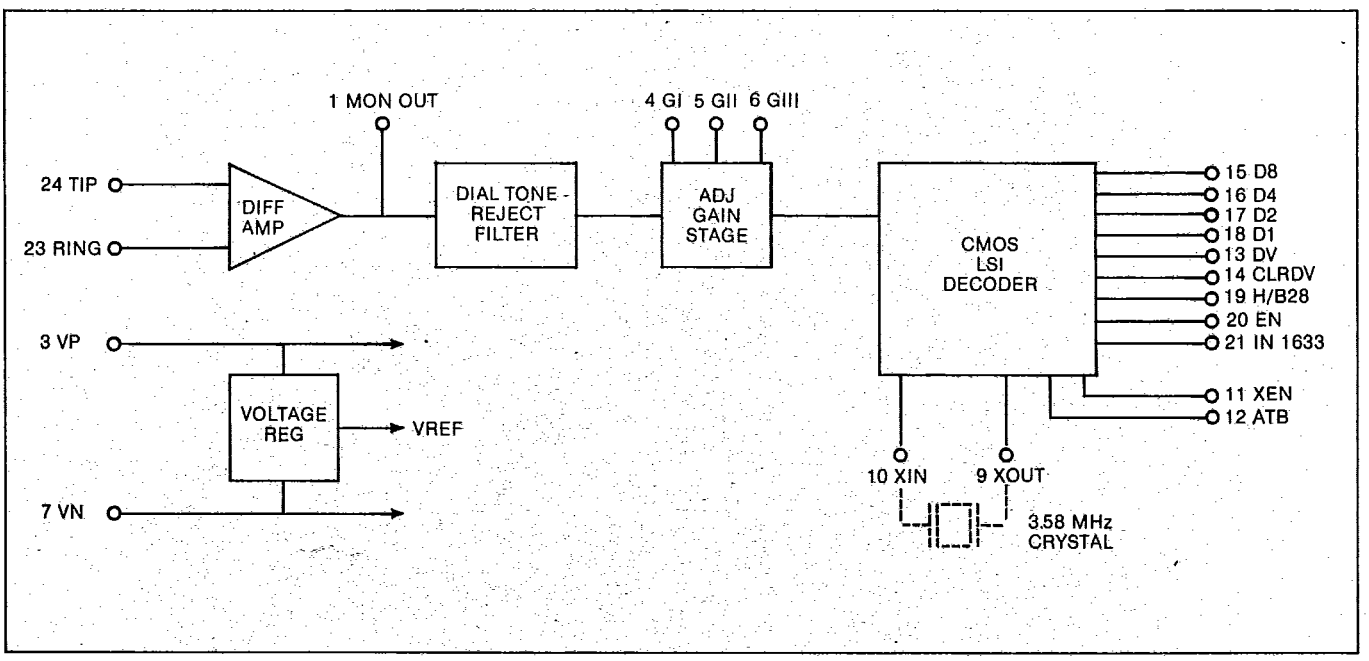
FEATURES

- Small size
- Wide dynamic range (>30 dB)
- Adjustable sensitivity
- Differential input
- 12 dB signal to noise ratio (typ.)
- Single supply operation
- Excellent dial tone rejection

APPLICATIONS

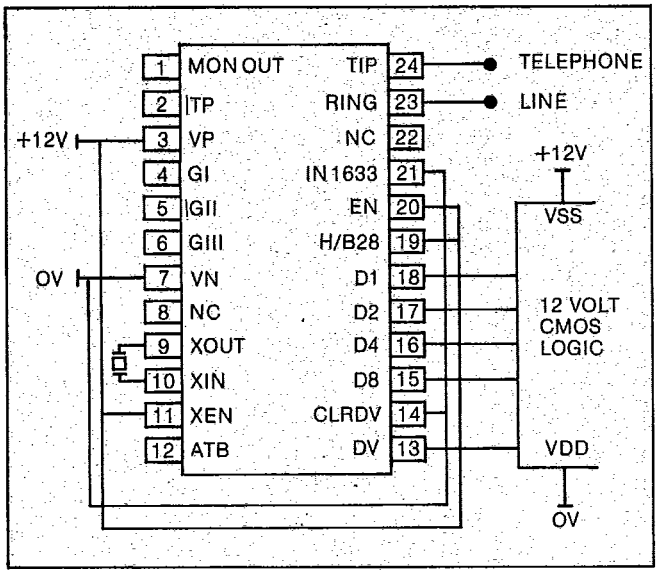
- End to end signalling
- Remote control systems
- Mobile radio
- PABX
- Key Systems

BLOCK DIAGRAM



Pin Description

TYPICAL CONNECTION DIAGRAM



OUTPUT TRUTH TABLE

Digit	H/B28=H				H/B28=L			
	D8	D4	D2	D1	D8	D4	D2	D1
1	L	L	L	H	L	L	L	L
2	L	L	H	L	L	L	L	H
3	L	L	H	H	L	L	H	L
4	L	H	L	L	L	H	L	L
5	L	H	L	H	L	H	L	H
6	L	H	H	L	L	H	H	L
7	L	H	H	H	H	L	L	L
8	H	L	L	L	H	L	L	H
9	H	L	L	H	H	L	H	L
0	H	L	H	L	H	H	L	H
*	H	L	H	H	H	H	L	L
#	H	H	L	L	H	H	H	L
A	H	H	L	H	L	L	H	H
B	H	H	H	L	L	H	H	H
C	H	H	H	H	H	L	H	H
D	L	L	L	L	H	H	H	H

PIN	NAME	DESCRIPTION
1	MON OUT	Provides signal which is one tenth differential input
2	TP	Internal test point
3	VP	Positive supply voltage
4	GI	Gain Adjust I
5	GII	Gain Adjust II, resistor from GI to GII increases sensitivity (see below)
6	GIII	Gain Adjust III, resistor from GII to GIII decreases sensitivity (see below)
7	VN	Negative Supply Voltage (ground)
8	NC	
9	XOUT	Crystal Out, 3.579 MHz crystal connected from pin 9 to pin 10
10	XIN	Crystal In (Tie to VP if external oscillator is used)
11	XEN	Enable Internal Oscillator. Tie to VP if crystal is used, tie to VN if external oscillator is used
12	ATB	Alternate Time Base. If XEN = H, ATB is clock output, If XEN = L, ATB is clock input from other 3210
13	DV	Data Valid. Indicates tone burst has been detected by going to high logic level. Will remain high until tone is removed or CLRDV is pulsed high
14	CLRDV	Clear Data Valid. Pulsing this pin to a high logic level will reset DV
15 16 17 18	D8 D4 D2 D1	Digital outputs. Provide a coded representation of the signal received when DV is high. Code is selected by H/B28 (pin 19)
19	H/B28	Code Select. When tied to VP output on D8-D1 is hexadecimal; when tied to VN, output is binary coded 2 of 8. Output truth table shows codes on D8-D1
20	EN	Output Enable. When pin is logic high, output codes on D8-D1 are enabled. When logic low, outputs D8-D1 assume high impedance state
21	IN1633	Inhibit 1633. When pin is logic high, 3210 will detect only digits 0-9, # and *. When logic low, 3210 will detect all 16 tone pair combinations
22	NC	
23	RING	More negative of analog inputs
24	TIP	More positive of analog inputs

GAIN INCREASE	RESISTANCE GI-GII	GAIN DECREASE	RESISTANCE GII-GIII
3.0 dB	100K	3.5 dB	1 Meg
5.3	50K	6.3	470K
7.1	33K	8.0	330K
9.3	22K	10.3	220K
11.6	15K	12.7	150K
14.3	10K	15.6	100K

Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

(all voltages referred to VN) Operation above absolute maximum ratings may permanently damage device.

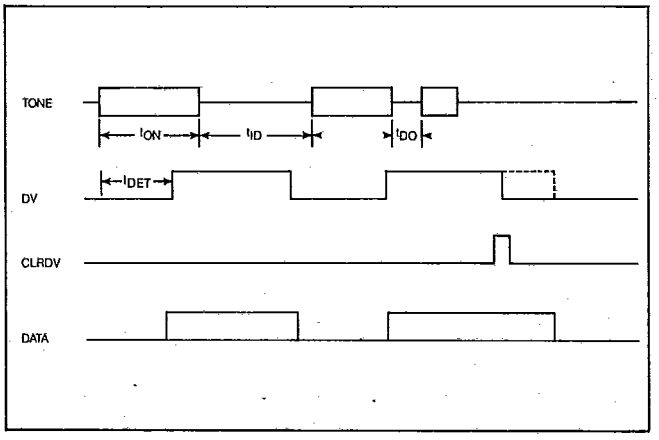
Rating	Min	Max	Units
Supply Voltage		16	Volts
Tip Voltage	−200	+200	Volts
Ring Voltage	−200	+200	Volts
Digital Input Voltage	VP+.5	VN−.5	Volts
DC Current Into Any Input		±1.0	mA
Operating Temperature Range	0	70	°C
Storage Temperature Range	−40	100	°C
Lead Temperature (Soldering, 10 sec.)		300	°C
Power Dissipation		1	Watt

DC ELECTRICAL CHARACTERISTICS

Test Conditions T_A = 0°−70°C, VP-VN = 12V, Unless Otherwise Specified

Parameter	Symbol	Min	Typ	Max	Units	Notes
Operating Voltage	VP-VN	10.8	12	13.2	V	
Operating Supply Current	I_P		18	25	mA	
Differential Input Voltage Tip to Ring	V_{IN}	−10		+60	V	For linear operation
Peak Input Voltage Tip to VN	V_{TIP}	−70		+70	V	For linear operation
Ring to VN	V_{RING}	−60		+10	V	For linear operation
Output Impedance				10	Ohms	Monitor Output
Digital Output Low Level	V_{OL}	0		0.5	V	I_O=−1mA, D1-D8, DV, ATB
Digital Output High Level	V_{OH}	11.5		12	V	I_O=1mA, D1-D8, DV, ATB
Digital Input Low Level	V_{IL}	0		3.6	V	CLRDV, IN1633, ATB, EN
		0		1.0	V	H/B28. XEN
Digital Input High Level	V_{IH}	8.4		12		
3-State Output Leakage	I_{O3}		±10^{-4}	±10	μADC	EN=LOW

TIMING DIAGRAM



AC ELECTRICAL AND TIMING PARAMETERS

Unless Otherwise Specified T_A = 0°−70°C, VP-VN = 12V ±10%; No Gain Adjust

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Valid Signal Level		−25		+6	dBm	Referred to 600 ohms each tone
Signal to Noise Ratio		14			dB	Note 1
Working Twist (V_L/V_H)		+8 −6			dB	
Recognition Bandwidth		±(1.5%+2)		±3.5%	Hz	Percentage of Center Frequency
Dial Tone Tolerance		+18			dB	Relative to input tone level, Note 2
60 Hz Tolerance		+15			dBm	
Must Detect Tone Burst	t_{ON}	40			mSec	
Must Detect Pause	t_{ID}	40			mSec	
Must Not Detect Pause	t_{DO}			20	mSec	
Minimum Detection Time	t_{DET}			20	mSec	
Power Supply Noise Tolerance		25			mVp-p	
Differential Input Impedance		540	600		KOhm	
Peak Input Voltage Tip to VN Ring to VN Tip to Ring		 −70 −60 −10		 +70 +10 +60	 V V V	For linear operation
Common Mode Rejection		60			dB	Tip and Ring to Monitor Output
Gain, Tip and Ring to Monitor Out		−20.2	−20	−19.8	dB	

Notes:
1. Band limited white noise (300Hz-3400Hz) tone burst 50 ms on 50 ms off
2. For dial tone frequencies 200-480 Hz

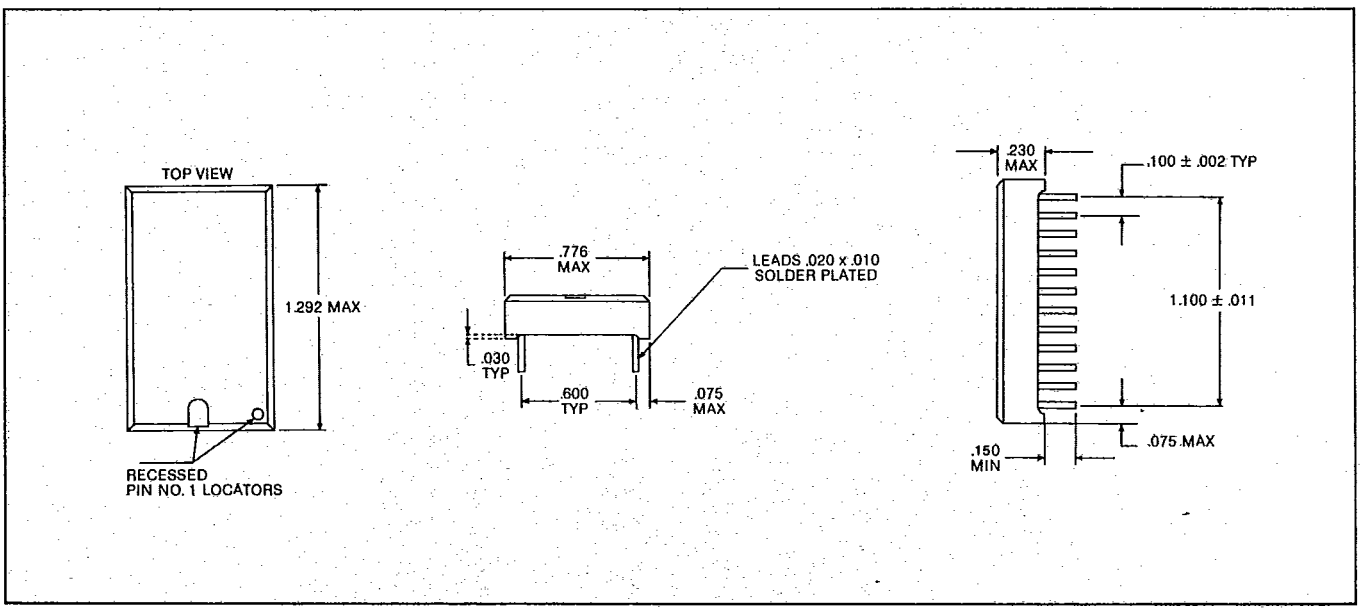
Functional Description

The AMS 3210 accepts standard DTMF frequencies normally generated by a pushbutton telephone and produces an output directly compatible with standard CMOS. The input signal is received on TIP and RING, which provide a balanced differential input impedance of 600 KOhm. (Output of this stage is available for other functions.) Signal is fed to a high pass filter which provides high dial tone rejection and 60Hz immunity. High-pass filter output is AC-coupled to a user-adjustable gain/attenuation stage.

Internal integrated circuit decoder provides band-split, tone detection and timing functions on the signal from the gain stage, produces output code selected by H/B28, and raises DV, signifying tone is present and output data levels are valid. Data output pins D8-D1 may be placed in a high impedance state for tri-state bus operation by taking signal EN to a logic low. CLRDV can reset DV until a new tone is detected by pulsing to a logic high. Or with CLRDV low, DV will return to a low state when the 3210 detects that the valid tone pair is no longer present.

Multiple devices may be operated from one crystal through use of XEN and ATB. The first is operated with a crystal attached to XIN and XOUT with XEN tied to VP. This causes ATB to be a clock output. Other devices using the same crystal have XEN tied low, XIN high, and use ATB as an input for the clock signal generated by the single crystal.

PACKAGE DESCRIPTION



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