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LR40994 Pulse Dialer CMOS LSI

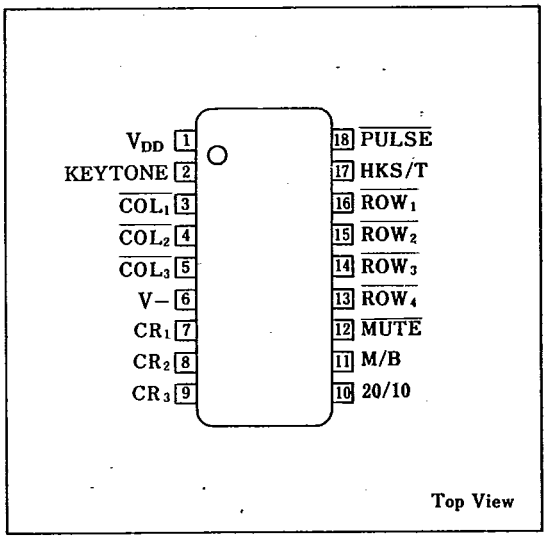
Description

The LR40994 is a monolithic CMOS LSI which uses a CR oscillator and provides the features required for a pulse dialer with redial.

Features

1. Make ratio: 34/40% pin-selectable
2. Pulse rate: 10/20pps pin-selectable
3. Pulse output: "0" true
4. Mute output: "0" true
5. 17-digit redial with either * or # input
6. Inter digital pause: 1000ms (10 pps)
7. Keytone output
8. Uses a ceramic oscillator as frequency reference
9. Direct telephone line operation
10. Uses either a standard 2-of-7 matrix keyboard or a single contact keyboard
11. Mute signal generated on pulse signal
12. 18-pin dual-in-line package

Pin Connections



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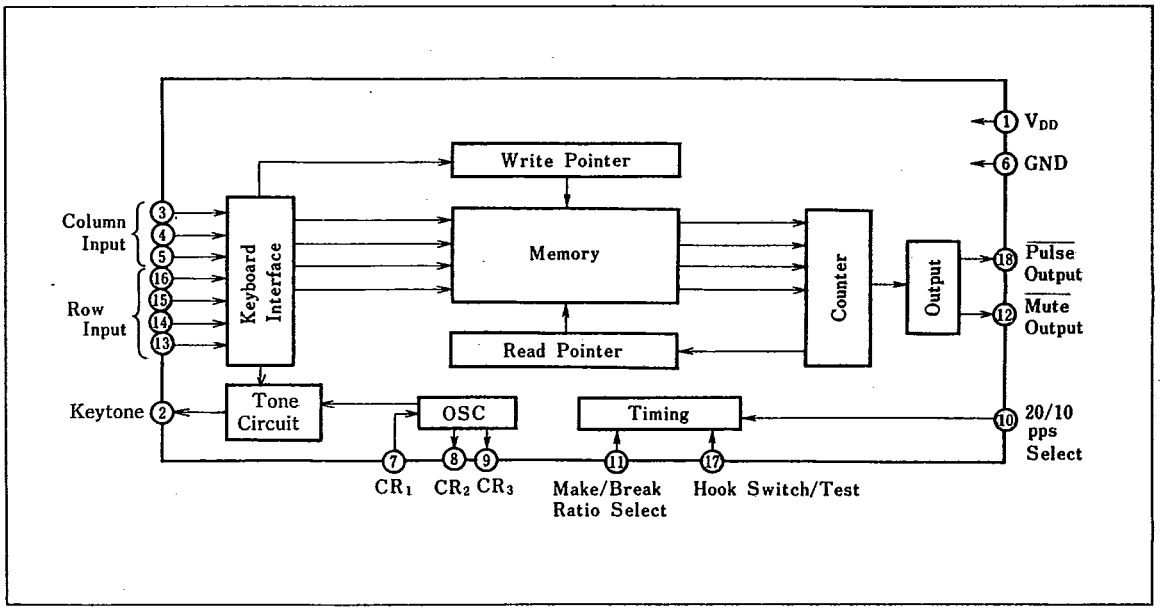
Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}	−0.3 to +6.2	V	1
Operating temperature	T_{opr}	−30 to +60	℃	
Storage temperature	T_{stg}	−55 to +150	℃	
Maximum power dissipation	P_D	500	mW	2
Maximum pin voltage	V_{IN1}	−0.3	V	3
	V_{IN2}	+0.3	V	4

Note 1 : Referenced to GND.
Note 2 : Ta=25℃.
Note 3 : The maximum applicable voltage on any pin with respect to GND.
Note 4 : The maximum applicable voltage on any pin with respect to V_{DD}.

■ Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	2.5 to 6.0	V

■ DC Characteristics

(Ta=−30 to +60℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Key contact resistance	R_{KI}				1	kΩ	
Key board capacitance	C_{KI}				30	pF	
Input voltage	K_{IH}	2-of-7 input mode	$0.8V_{DD}$		V_{DD}	V	1
	K_{IL}		GND		$0.2V_{DD}$	V	
$\overline{\text{MUTE}}$ sink current	I_{ML}	V_{DD}=2.5V, V_{OUT}=0.5V	500			μA	2
$\overline{\text{PULSE}}$ sink current	I_P	V_{DD}=2.5V, V_{OUT}=0.5V	1.0			mA	3
Tone Output Sink Current	I_{TL}	V_{DD}=2.5V, V_{OUT}=0.5V	250			μA	4
Tone Output Source Corrent	I_{TH}	V_{DD}=2.5V, V_{OUT}=V_{IN}=0.5V	250			μA	4
Memory retention current	I_{MR}	All outputs in no-load state		0.7	2.5	μA	
Operating current	I_{OP}	All outputs in no-load state		100	150	μA	
Key pull-up resistance	K_{IRU}	V_{DD}=6.0V		100		kΩ	
Key pull-down resistance	K_{IRD}	V_{IN}=4.8V		4		kΩ	
ON-HOOK pull-up resistance	R_{OH}			100		kΩ	
$\overline{\text{MUTE}}$, $\overline{\text{PULSE}}$ leakage	I_{LKG}	V_{DD}=6.0V, V_{OUT}=6.0V		0.001	1	μA	

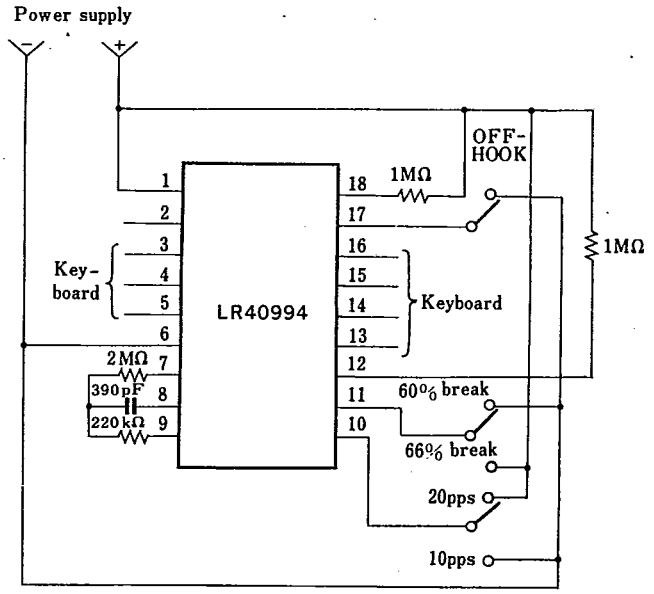
Note 1: Applies to key input pins ($\overline{ROW_1}$-$\overline{ROW_4}$, $\overline{COL_1}$-$\overline{COL_3}$)
Note 2: Applies to $\overline{\text{MUTE}}$ output pin.
Note 3: Applies to $\overline{\text{PULSE}}$ output pin.
Note 4: Applies to KEYTONE pin.

AC Characteristics

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Oscillator frequency	Fosc		4		kHz	1
Key input debounce time	t_{PB}		10		ms	3, 4
Key input time	t_{KD}	40			ms	4, 5
2× key input rollover time	t_{KR}	5			ms	4
Oscillation start time	t_{OS}		1		ms	
Mute valid time after final pulse output	t_{MD}		5		ms	3, 4
Output pulse rate	Pr		10		pps	2
On-Hook time required to clear memory	t_{OH}	300			ms	4
Pre-digital pause	t_{PDP}		$1000+t_M$		ms	3,4,7
Inter-digital pause	t_{IDP}		$1000+t_M$		ms	3,4,7
Frequency stability	Δf		±4		%	8
Frequency stability	Δf		±4		%	9
Tone output frequency	F_{TONE}		1		kHz	4,6

Note 1: External CR values are: R_S=2MΩ, R=220kΩ, C=390pF.
Note 2: Pin 10 connected to V_{DD} selects 20pps.
Note 3: If the output pulse rate is 20pps, the time will be 1/2 of that shown.
Note 4: These values are in proportion to the oscillation frequency.
Note 5: Debounce time and crystal oscillation start-up time < 40ms
Note 6: If the output pulse rate is 20pps, the tone output will be 2kHz.
Note 7: t_m (Make time)=100ms-t_B.
Note 8: V_{DD}=2.5 to 3.5V.
Note 9: V_{DD}=3.5 to 6.0V.

Test Ciruit



Functional Description

The LR40994 is a monolithic CMOS integrated circuit which uses an inexpensive CR oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with redial. It operates directly off the telephone line supply and converts 2-of-7 keyboard inputs into pulse signals simulating a rotary telephone dial. When not outpulsing, the LR40994 consumes only microamperes of current.

Keyboard logic is totally static so that the LR40994 will not introduce noise into the telephone system. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function.

When Off-Hook, the LR40994 senses a key down condition, verifies that only one key is depressed and then enters the key's code into an on-chip memory.

The FIFO (First In First Out) memory will store up to 17 digits, and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit starts a pre-digital pause counter and clears the memory buffer. At the end of the pre-digital pause, outpulsing begins. As digits are entered during the outpulsing period they will also be stored in the memory. Outpulsing will continue until all entered digits have been dialed. The first 17 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either # or *, provided that the receiver has been On-Hook for the minimum t_{OH} (refer to the AC Characteristics section).

When On-Hook, key inputs will not be recognized because the oscillator is disabled. This oscillator inhibit prevents the circuit from drawing excessive current when On-Hook.

The LR40994 generates a 1kHz tone signal (with the 10pps pulse rate selected) when a key is depressed.

Pin Description

V_{DD} (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to GND and is supplied from a 150μA current source. This voltage must be regulated to less than 6.0 volts.

Tone Output (Pin 2)

The tone signal output pin is a CMOS complementary output that drives an external bipolar transistor. This pin generates a tone signal (1kHz when 10pps is selected, 2kHz for 20pps) in recognition of a key depression.

Keyboard Inputs (Pins 3, 4, 5, 13, 14, 15, 16)

The LR40994 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or GND being simultaneously presented to both a single row and column.

When in On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. To be accepted, the input must remain valid continuously for 10ms of debounce time.

$\overline{\text{Pulse}}$ Output (Pin 18)

The Pulse output is an open-drain N-channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by disconnecting and connecting the network.

The LR40994 $\overline{\text{Pulse}}$ output is an open circuit during make and pulls to the GND supply during break.

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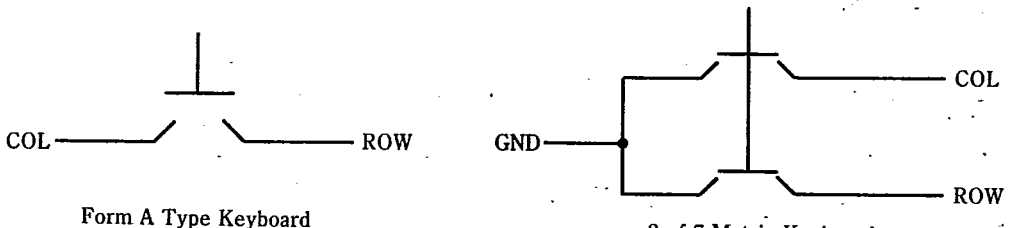


Form A Type Keyboard

2-of-7 Matrix Keyboard
Negative Common

Fig. 1 Keyboard configurations

Oscillator (Pins 7, 8, 9)

The LR40994 contains on-chip inverters to provide an oscillator which will operate with a minimum of external components. Figure 2 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K=R_s/R$ equal to 10.

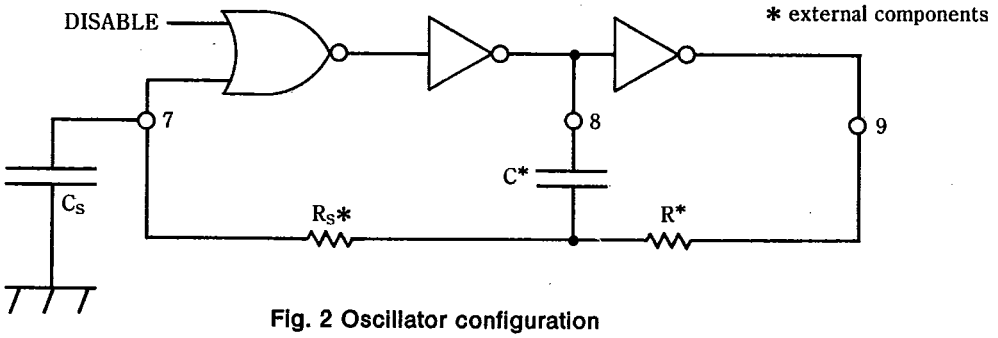


Fig. 2 Oscillator configuration

The oscillator period is given by:

$T=RC[1.386+(3.5KC_s/C-(2K/(K+1))$
$\ln (K/(1.5K+0.5))]$

where C_s is the stray capacitance on pin 7. Accuracy and stability will be enhanced with this capacitance minimized.

GND (Pin 6)

This is the negative supply pin and is normally tied to V_{REF} (See V_{REF} paragraph).

20/10 pps (Pin 10)

Tying this pin M/B to GND will select an output pulse rate of 10 pps. Tying to V_{DD} will select 20 pps.

Make/Break Select (Pin 11)

The Make/Break ratio may be selected by connecting the M/B pin to either the V_{DD} or GND supply. The two popular ratios from which the user can choose are indicated below.

INPUT	MAKE	BREAK
V_{DD} (Pin 1)	34%	66%
GND (Pin 6)	40%	60%

$\overline{\text{Mute}}$ Output (Pin 12)

The $\overline{\text{Mute}}$ output is a complementary CMOS transistor designed to drive an external bipolar transistor. This circuitry is used to mute the receiver during outpulsing.

As shown in Timing Diagram, the LR40994 Mute output turns on (pulls to the GND supply) at the beginning of the pre-digital pause and turns off (goes to an open circuit) following the last break. The delay from the end of the last break until the Mute output turns off is the mute overlap, specified as t_{MO}.

Test/On-Hook Switch Input (Pin 17)

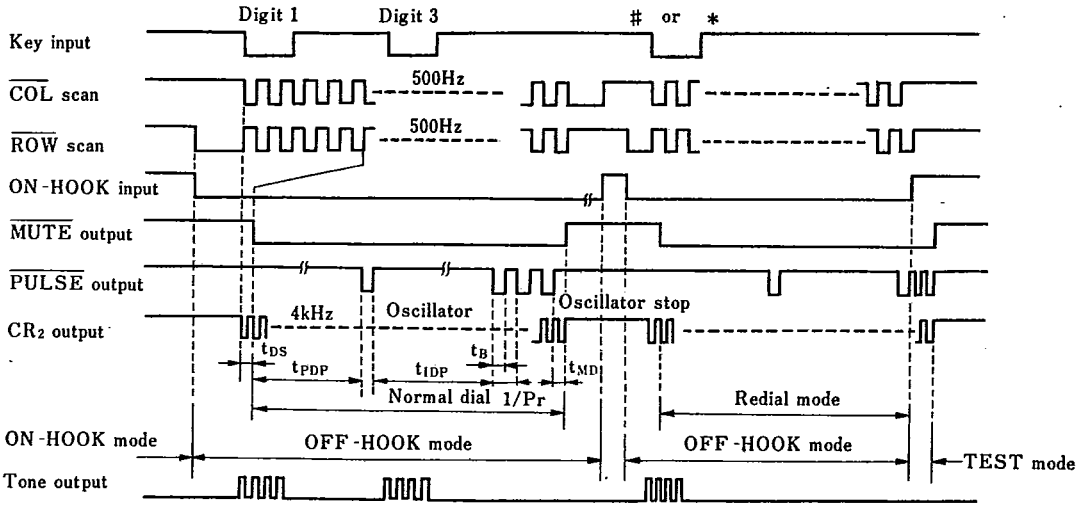
The "Test" or "On-Hook" input of the LR40994 has a 100kΩ pull-up to the positive supply. A V_{DD} input or allowing the pin to float sets the circuit into On-Hook or test mode while a GND input sets it in the Off-Hook or normal Mode.

When Off-Hook, the LR40994 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the LR40994 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 × the normal rate (M/B ratio is then 50/50). This features provides a means of rapidly testing the device and is also an efficient method by which the circuitry can be reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is de-activated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transistion on the Mute Output will insure that the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

■ Timing Diagram



System Configuration Example

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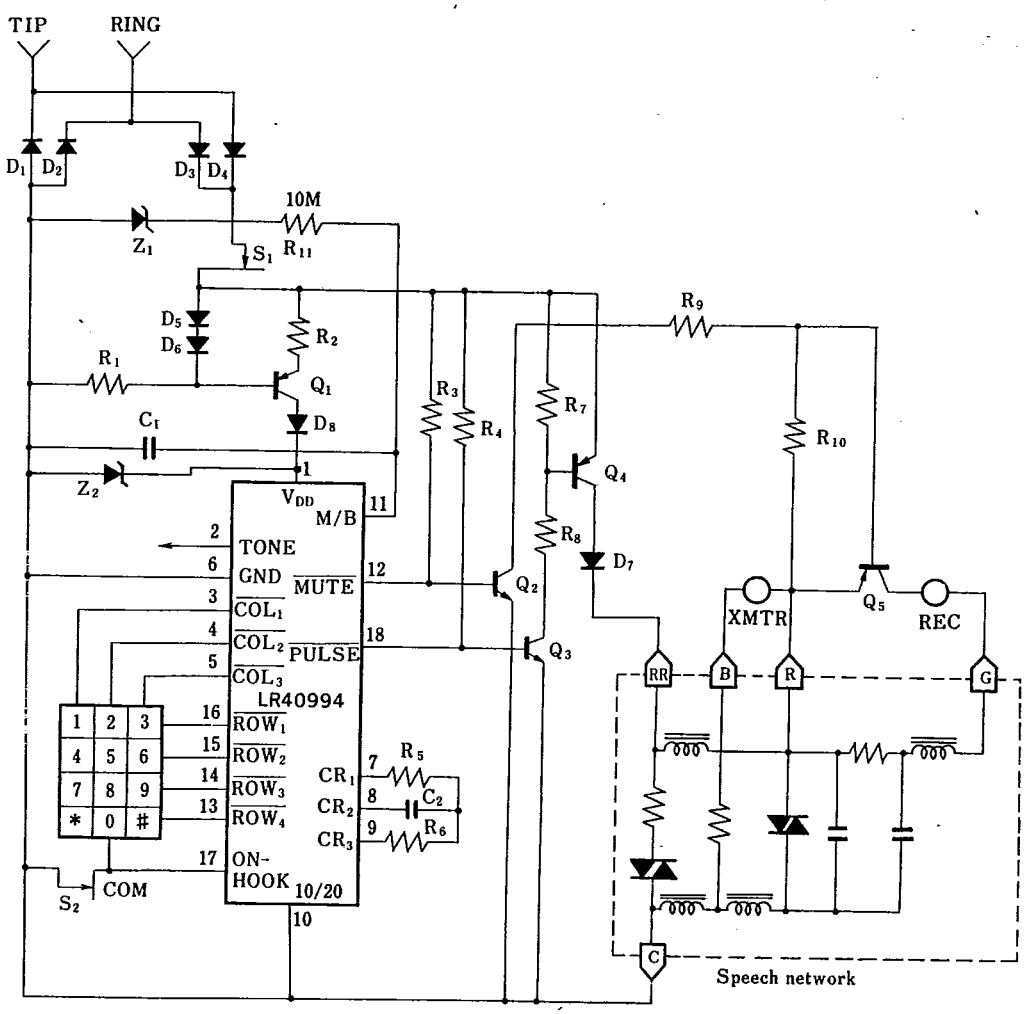

R_1 = 560kΩ
R_2 = 1.4kΩ
R_3 = 470kΩ
R_4 = 330kΩ
R_5 = 2MΩ
R_6 = 220kΩ
R_7 = 100kΩ
R_8 = 3kΩ
R_9 = 3kΩ
R_{10} = 100kΩ
R_{11} = 10MΩ

Q_1 = 2N5401
Q_2 = 2N5550
Q_3 = 2N5550
Q_4 = 2N5401
Q_5 = 2N5401

D_1 = 1N4004
D_2 = 1N4004
D_3 = 1N4004
D_4 = 1N4004
D_5 = 1N914
D_6 = 1N914
D_7 = 1N4004
D_8 = Zener Diode

C_1 = 68μF
C_2 = 390 pF
Z_1 = 120V, 1-watt Zener Diode
Z_2 = 3 to 5V, 1/2-watt Zener Diode