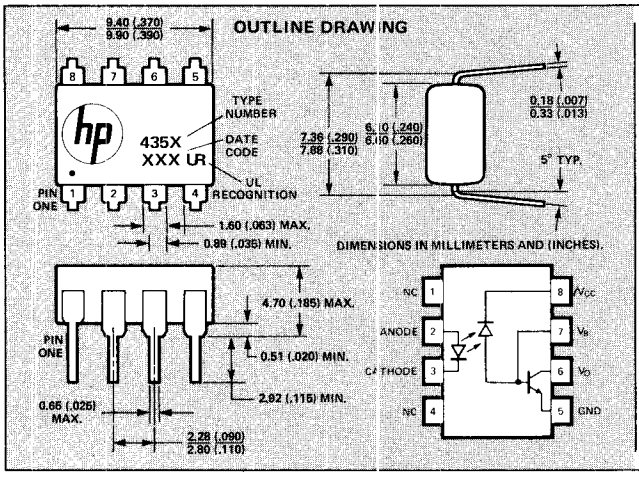
HEWLETT hp PACKARD

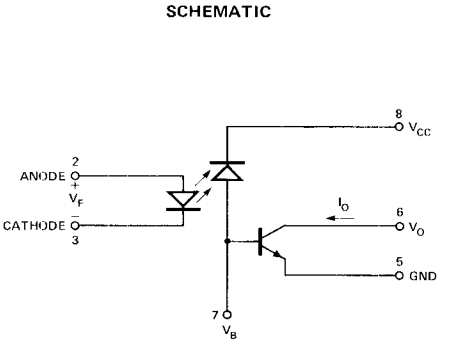
COMPONENTS

HIGH SPEED OPTICALLY COUPLED ISOLATORS

5082-4350
5082-4351
5082-4352

TECHNICAL DATA APRIL 1976





Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **3000Vdc INSULATION VOLTAGE**
- **2 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUT**

Description

The 5082-4350 series isolators use a light emitting diode and an integrated photon detector to provide 3000V dc electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collector improve the speed up to a hundred times that of a conventional phototransistor isolator by reducing the base-collector capacitance.

The 5082-4350 is suitable for use in TTL/CMOS, TTL/LTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -4350 is 7% minimum at I_F = 16 mA.

The 5082-4351 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the -4351 is 15% minimum at I_F = 16 mA.

The 5082-4352 is suitable for use in applications where matched or known CTR is desired. CTR is 15 to 22% at I_F = 16 mA.

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) allows use of low cost twisted pair cable instead of coax.
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** – Pins 2-7 of the -4350 series conform to pins 1-6 of 6 pin phototransistor isolators. Pin 8 can be tied to any available bias voltage of 1.5V to 15V for high speed operation.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.

Absolute Maximum Ratings

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to 100°C
Lead Solder Temperature . . . . . 260°C for 10Sec
(1/16" below seating plane)
Average Input Current – I_F . . . . . 25mA[1]
Peak Input Current – I_F . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F 1.0A
(≤1μsec pulse width, 300pps)
Reverse Input Voltage – V_R (Pin 3-2) 5V
Input Power Dissipation . . . . . 45mW[3]
Average Output Current – I_O (Pin 6) 8mA
Peak Output Current 16mA
Emitter-Base Reverse Voltage (Pin 5-7) 5V
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 6-5)
. . . . . -0.5V to 15V
Base Current – I_B (Pin 7) 5mA
Output Power Dissipation . . . . . 100mW[4]

See notes, following page.

Electrical Specifications (T_A = 25°C)

Parameter	Sym.	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	4350	7	18		%	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V	2	5
		4351	15	22		%			
		4352	15		22	%			
Logic Low Output Voltage	V_{OL}	4350		0.1	0.4	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V		
		4351, 4352		0.1	0.4	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}			3	500	nA	I_F = 0mA, V_O = V_{CC} = 5.5V	6	
Logic High Output Current	I_{OH}				100	μA	I_F = 0mA, V_O = V_{CC} = 15V		
Logic Low Supply Current	I_{CCL}			16		μA	I_F = 16mA, V_O = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}			0.02	1	μA	I_F = 0mA, V_O = Open, V_{CC} = 15V		
Input Forward Voltage	V_F			1.5	1.7	V	I_F = 16mA	3	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 16mA		
Input Reverse Voltage	V_R		5			V	I_R = 10μA		
Input Capacitance	C_O			40		pF	f = 1MHz, V_F = 0		
Input – Output Insulation Leakage Current	I_{I-O}				1.0	μA	45% Relative Humidity, t=5 sec. V_{I-O} = 3000 Vdc		6
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500V dc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		6
Transistor DC Current Gain	h_{FE}			150		–	V_O = 5V, I_O = 3mA		

Switching Specifications (T_A = 25°C)

V_{CC} = 5V, I_F = 16mA UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	4350		0.5	1.5	μs	R_L = 4.1kΩ	5,9	8,9
		4351, 4352		0.2	0.8	μs	R_L = 1.9kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}	4350		0.4	1.5	μs	R_L = 4.1kΩ	5,9	8,9
		4351, 4352		0.3	0.8	μs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	4350		>1000		V/μs	I_F = 0mA, V_{CM} = 10V_{P-P}, R_L = 4.1kΩ	10	7,8,9
		4351, 4352		>1000		V/μs	I_F = 0mA, V_{CM} = 10V_{P-P}, R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	4350		<-1000		V/μs	V_{CM} = 10V_{P-P}, R_L = 4.1kΩ	10	7,8,9
		4351, 4352		<-1000		V/μs	V_{CM} = 10V_{P-P}, R_L = 1.9kΩ		
Bandwidth	BW			2		MHz	R_L = 100Ω	8	10

NOTES:
1. Derate linearly above 70° C free-air temperature at a rate of 0.8mA/° C.
2. Derate linearly above 70° C free-air temperature at a rate of 1.6mA/° C.
3. Derate linearly above 70° C free-air temperature at a rate of 0.9mW/° C.
4. Derate linearly above 70° C free-air temperature at a rate of 2.0mW/° C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
8. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and a 5.6kΩ pull-up resistor.
9. The 4.1kΩ load represents 1 LTTL unit load of 0.18mA and a 5.6kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.

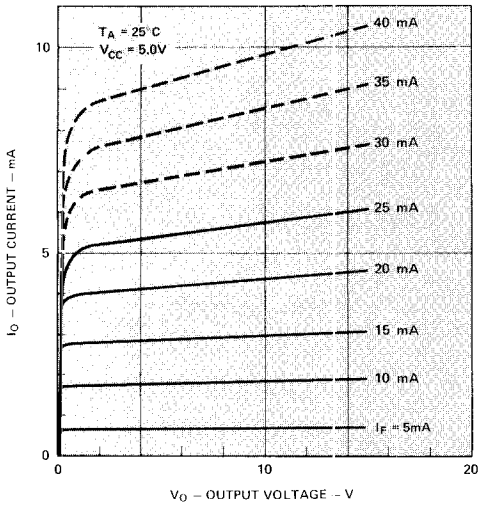


Figure 1. DC and Pulsed Transfer Characteristics.

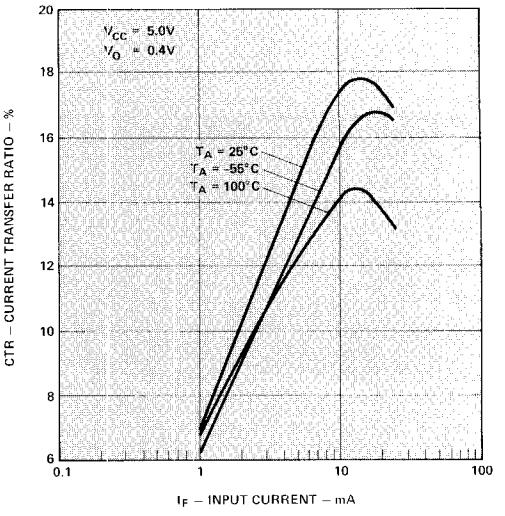


Figure 2. Current Transfer Ratio vs. Input Current.

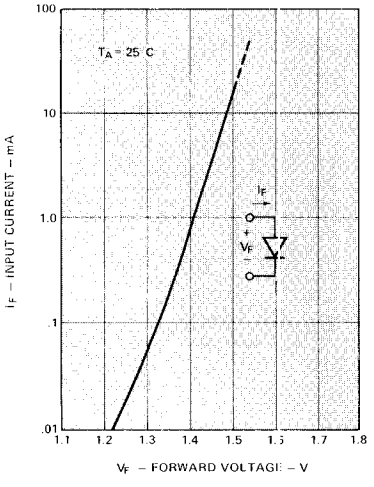


Figure 3. Input Current vs. Forward Voltage.

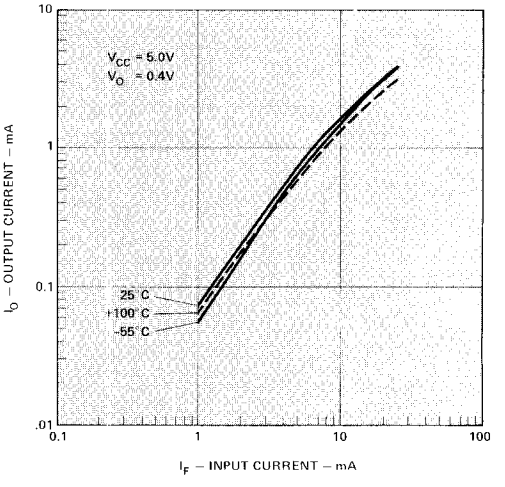


Figure 4. Output Current vs. Input Current.

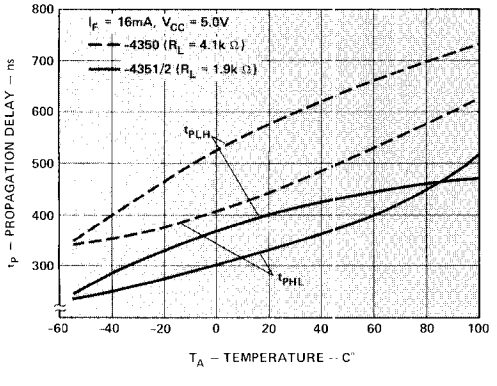


Figure 5. Propagation Delay vs. Temperature.

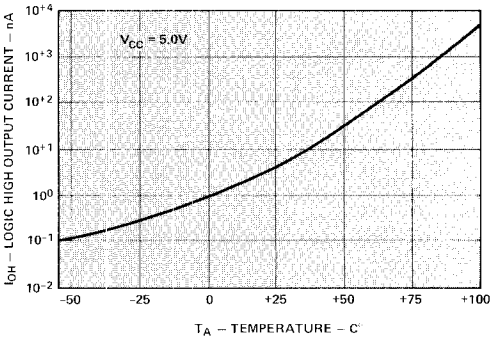


Figure 6. Logic High Output Current vs. Temperature.

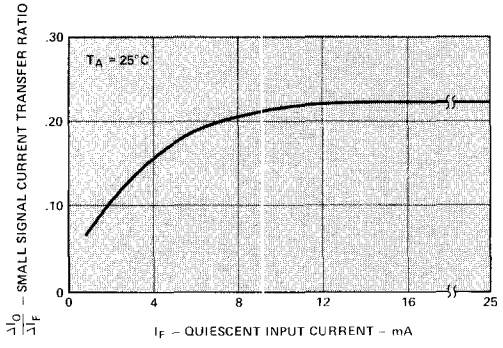
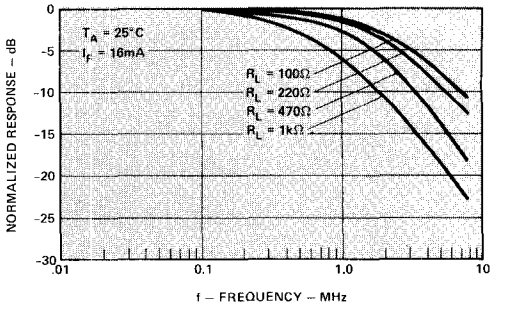


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



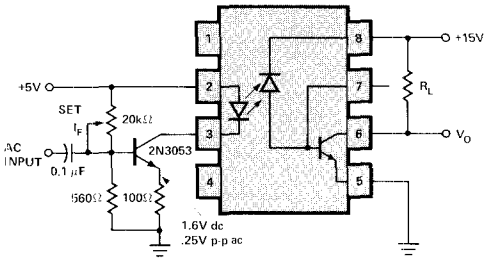
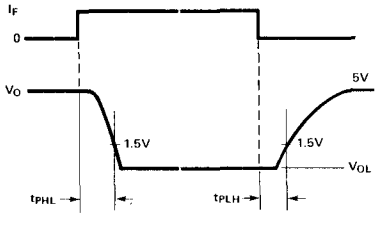


Figure 8. Frequency Response.



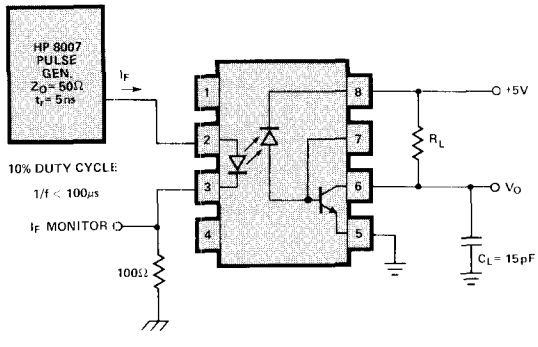
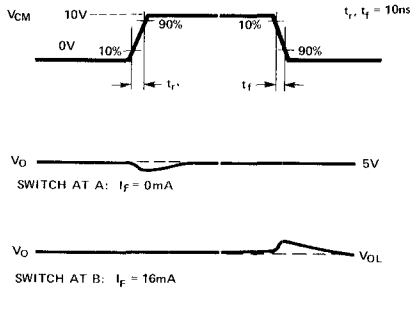


Figure 9. Switching Test Circuit.



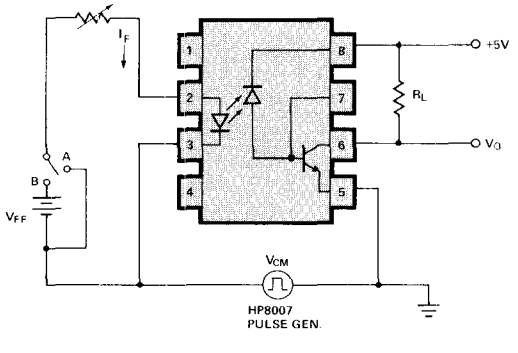


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.