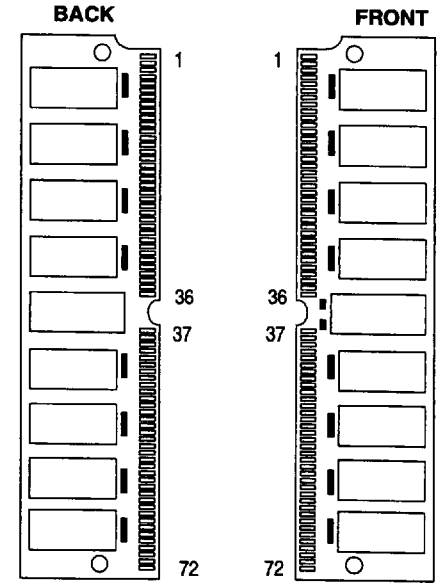
DRAM Single-In-Line Memory Module (SIMM)

16 and 32 Megabyte

4, 8M x 36
5 V, EDO, Unbuffered

- JEDEC–Standard 72–Lead Single–In–Line Memory Module (SIMM)
- Single 5 V Power Supply, TTL–Compatible Inputs and Outputs
- Extended Data Out (EDO)
- $\overline{RAS}$–Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
- 16MB/32MB: 2048 Cycle Refresh: 32 ms

4M x 36 (16MB), 8M x 36 (32MB)
72–LEAD LOW HEIGHT SIMM
CASE 866–02



BACK NOT POPULATED ON 4M x 36 (16MB)

PART NUMBERS (See Page 19 for Definitions)

Organization	60
4M x 36	MB3640J00TCSN60 MB3640J00TCSG60 MB3640J00MCSN60 MB3640J00MCSG60
8M x 36	MB3680J00TCSN60 MB3680J00TCSG60 MB3680J00MCSN60 MB3680J00MCSG60

KEY TIMING PARAMETERS

Speed	t_{RC} (ns)	t_{RAC} (ns)	t_{CAC} (ns)	t_{AA} (ns)	t_{EPC} (ns)
60	110	60	17	30	25

ADDITIONAL PARAMETERS

Configuration	Speed	Active Power Dissipation (mW) (Max)	Standby Power Dissipation	
			TTL	CMOS
16MB	60	5,885	99	49.5
32MB	60	5,984	198	99

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	$\overline{RAS3}$*	45	$\overline{RAS1}$*	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

*NC on the 16 MB.

PIN NAMES

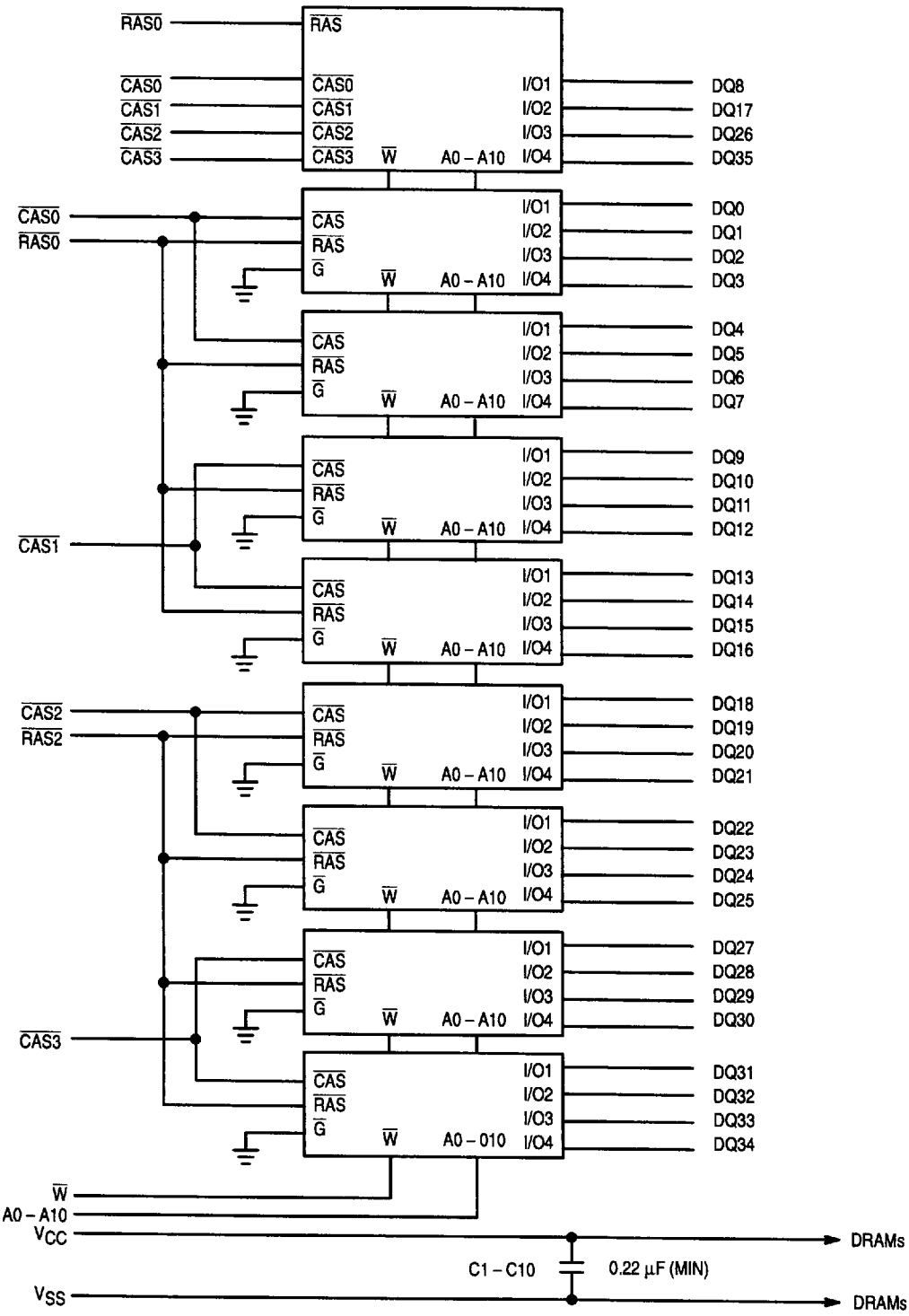
A0 – A10 ..... Address Inputs
DQ0 – DQ35 ..... Data Input/Output
$\overline{CAS0}$ – $\overline{CAS3}$ Column Address Strobe
PD1 – PD4 ..... Presence Detect
$\overline{RAS0}$ – $\overline{RAS3}$ ... Row Address Strobe
$\overline{W}$ ..... Read/Write Input
V_{CC} ..... Power (+ 5 V)
V_{SS} ..... Ground
NC ..... No Connection

All power supply and ground pins must be connected for proper operation of the device.

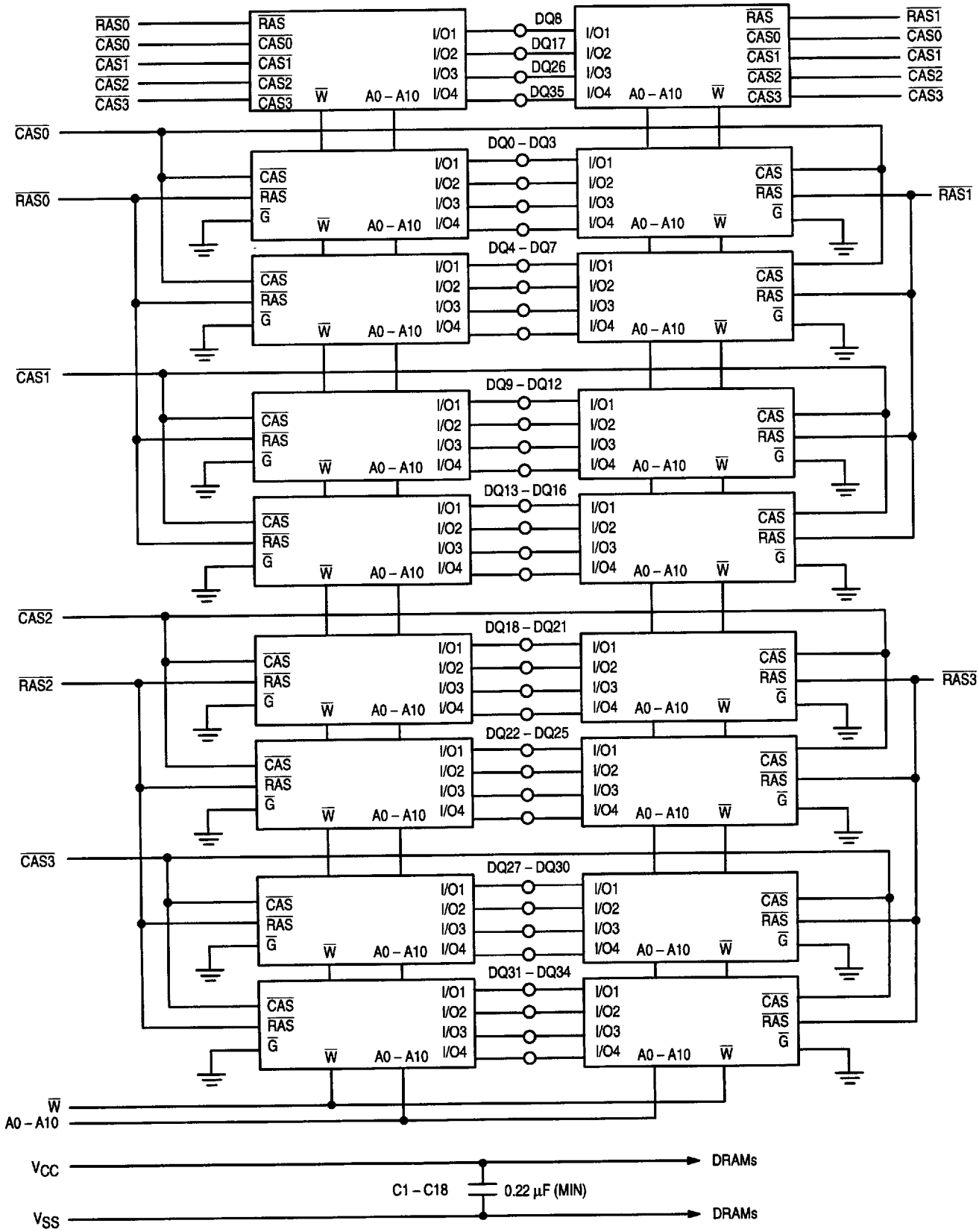
PRESENCE DETECT

Pin Names	Speed	16MB	32MB
PD1		V_{SS}	NC
PD2		NC	V_{SS}
PD3	60	NC	NC
PD4	60	NC	NC

16MB BLOCK DIAGRAM



32MB BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7	V
Voltage Relative to V_{SS} (for Any Pin Except V_{CC})	V_{in}, V_{out}	− 0.5 to V_{CC}+ 0.5	V
Data Output Current per DQ pin	I_{out}	50	mA
Power Dissipation 16MB/32MB	P_D	8.1/16.2	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	− 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	− 0.5*	—	0.8	V
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(i)}$	–170	—	+ 170	µA
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(o)}$	–20	—	+ 20	µA
Output High Voltage (I_{OH} = –5 mA)	V_{OH}	2.4	—	—	V
Output High Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	—	0.4	V

* 2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages Referenced to V_{SS})

Characteristic	Symbol	16MB		32MB		Unit	Notes
		Min	Max	Min	Max		
V_{CC} Power Supply Current (t_{RC} = t_{RC} Min) 60	I_{CC1}	—	1070	—	1088	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	18	—	36	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles (t_{RC} = t_{RC} Min) 60	I_{CC3}	—	1070	—	1088	mA	1, 2
V_{CC} Power Supply Current During EDO Cycle (t_{EPC} = t_{EPC} Min) 60	I_{CC4}	—	1005	—	1023	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	9	—	18	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (t_{RC} = t_{RC} Min) 60	I_{CC6}	—	1070	—	1088	mA	1

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Input Capacitance	Symbol	16MB Max	32MB Max	Unit
Addresses	C_{in}	55	100	pF
$\overline{WE}$	C_{in}	73	136	pF
$\overline{RAS}$	C_{in}	45	45	pF
$\overline{CAS}$	C_{in}	31	52	pF
DQ	C_{out}	17	24	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		60		Unit	Notes
	Std	Alt	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	ns	5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	ns	6, 7, 11, 12
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	17	ns	6, 8, 11
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	ns	6, 9, 12
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	ns	6
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	ns	
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	15	ns	10, 16
Transition Time (Rise and Fall)	t_T	t_T	2	50	ns	1
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	48	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	10	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	38	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	ns	12

(continued)

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed. If using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, instead of 8 $\overline{RAS}$ only refresh cyces are required.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min), t_{RWC} (min), and t_{EPC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max), t_{REZ} (max), and t_{WEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (continued)

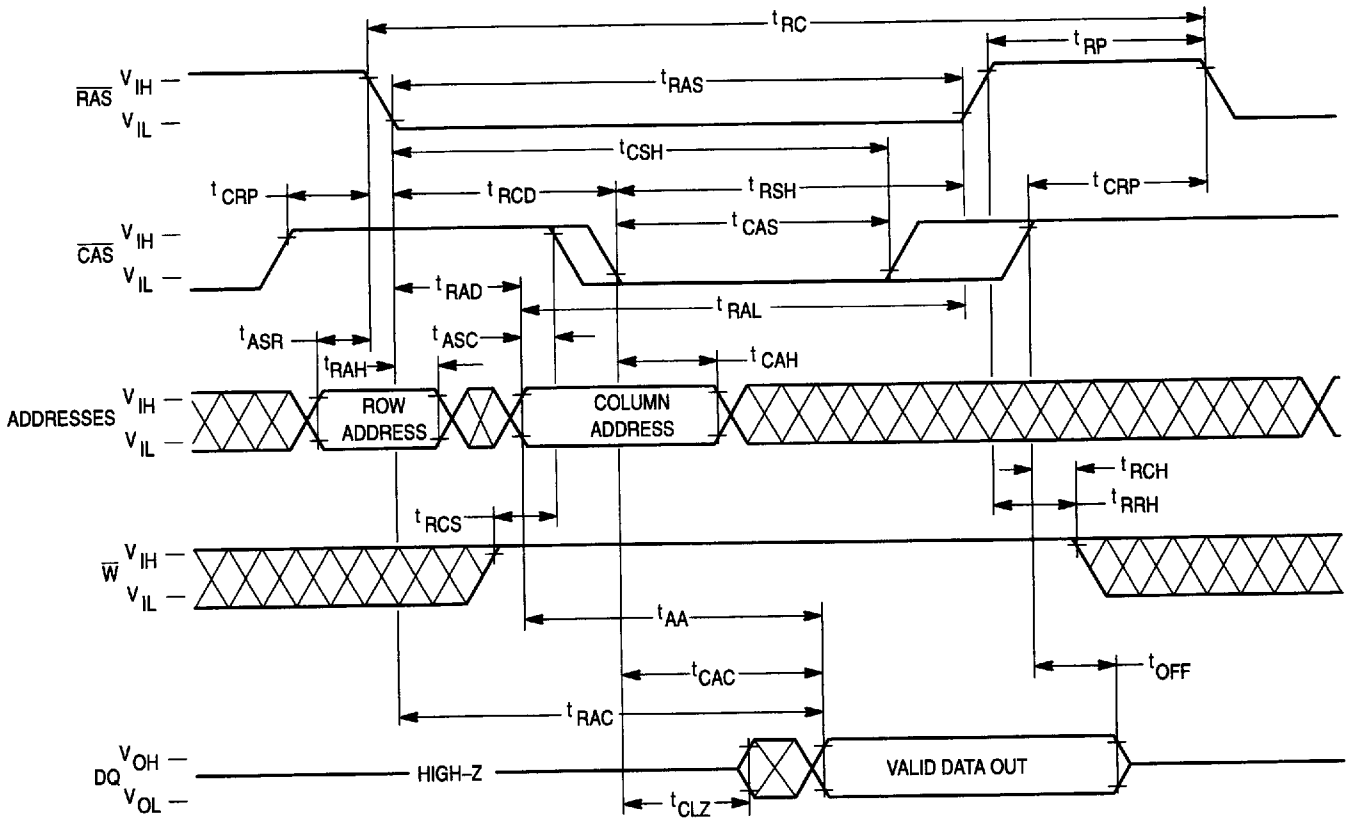
Parameter	Symbol		60		Unit	Notes
	Std	Alt	Min	Max		
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	10	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	10	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	ns	14
Refresh Period 16MB, 32MB	t_{RVRV}	t_{RFSH}	—	32	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{CELCEL}	t_{CSR}	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	20	—	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge (EDO)	t_{CEHREH}	t_{RHCP}	35	—	ns	
$\overline{RAS}$ Pulse Width (EDO)	t_{RELREH}	t_{RASP}	60	200 k	ns	
$\overline{RAS}$ to Next $\overline{CAS}$ Delay (EDO)	t_{RELCEL}	t_{RNCD}	60	—	ns	
EDO Cycle Time	t_{CELCEL}	t_{EPC}	25	—	ns	
Output Data Hold Time	t_{CELQZ}	t_{COH}	5	—	ns	
Output Buffer Turn–Off Delay from $\overline{RAS}$	t_{REHQZ}	t_{REZ}	0	15	ns	10, 16
Output Buffer Turn–Off Delay from $\overline{W}$	t_{WLQZ}	t_{WEZ}	0	15	ns	10
$\overline{W}$ to Data Delay	t_{WLDV}	t_{WED}	15	—	ns	

NOTES:

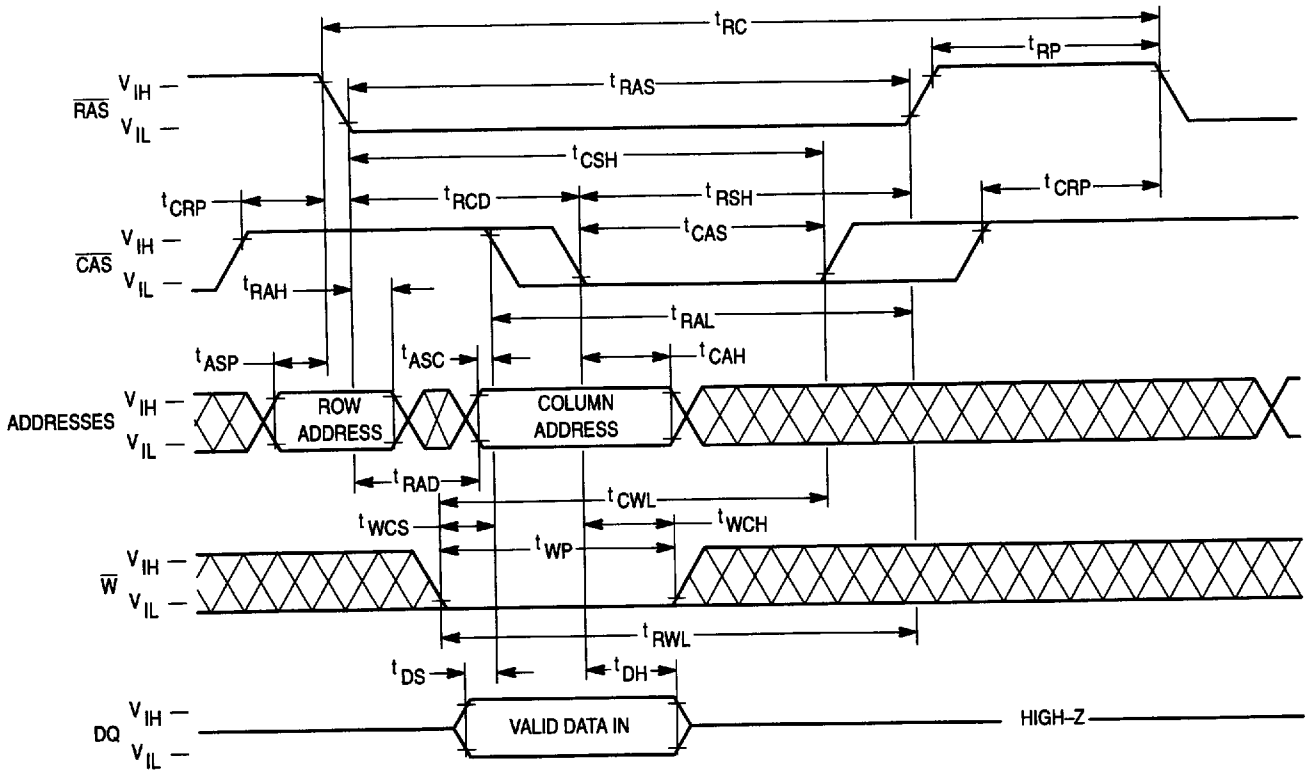
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is a write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ goes high, the open circuit condition is controlled by $\overline{CAS}$ going high (t_{OFF}). If $\overline{CAS}$ goes high before $\overline{RAS}$ goes high, the open circuit condition is controlled by $\overline{RAS}$ going high (t_{REZ}).
14. To avoid bus contention and potential damage to the module, $\overline{RAS0}$ and $\overline{RAS1}$ may not be active low simultaneously. Similarly, $\overline{RAS2}$ and $\overline{RAS3}$ may not be simultaneously active low.

TIMING DIAGRAMS

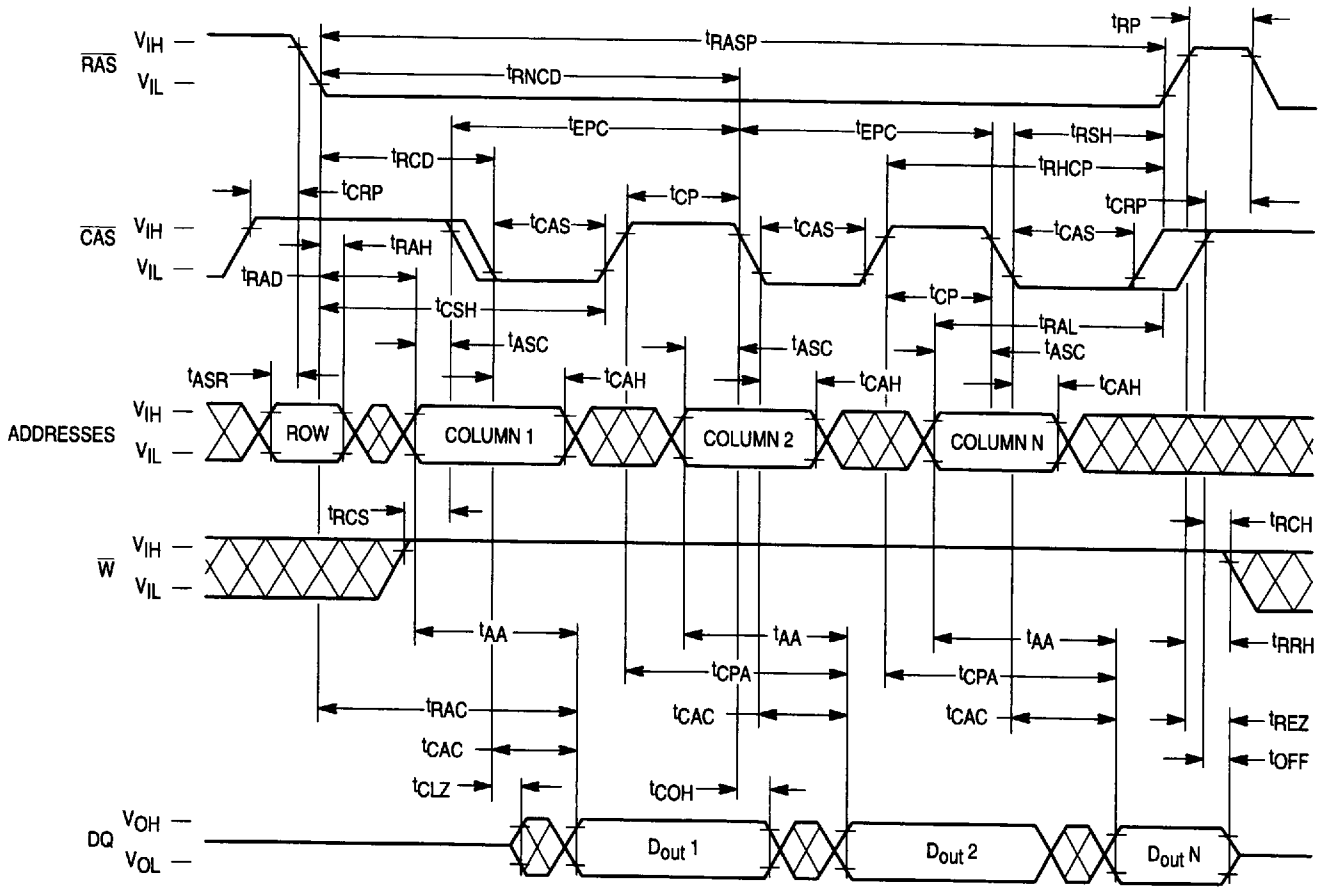
READ CYCLE



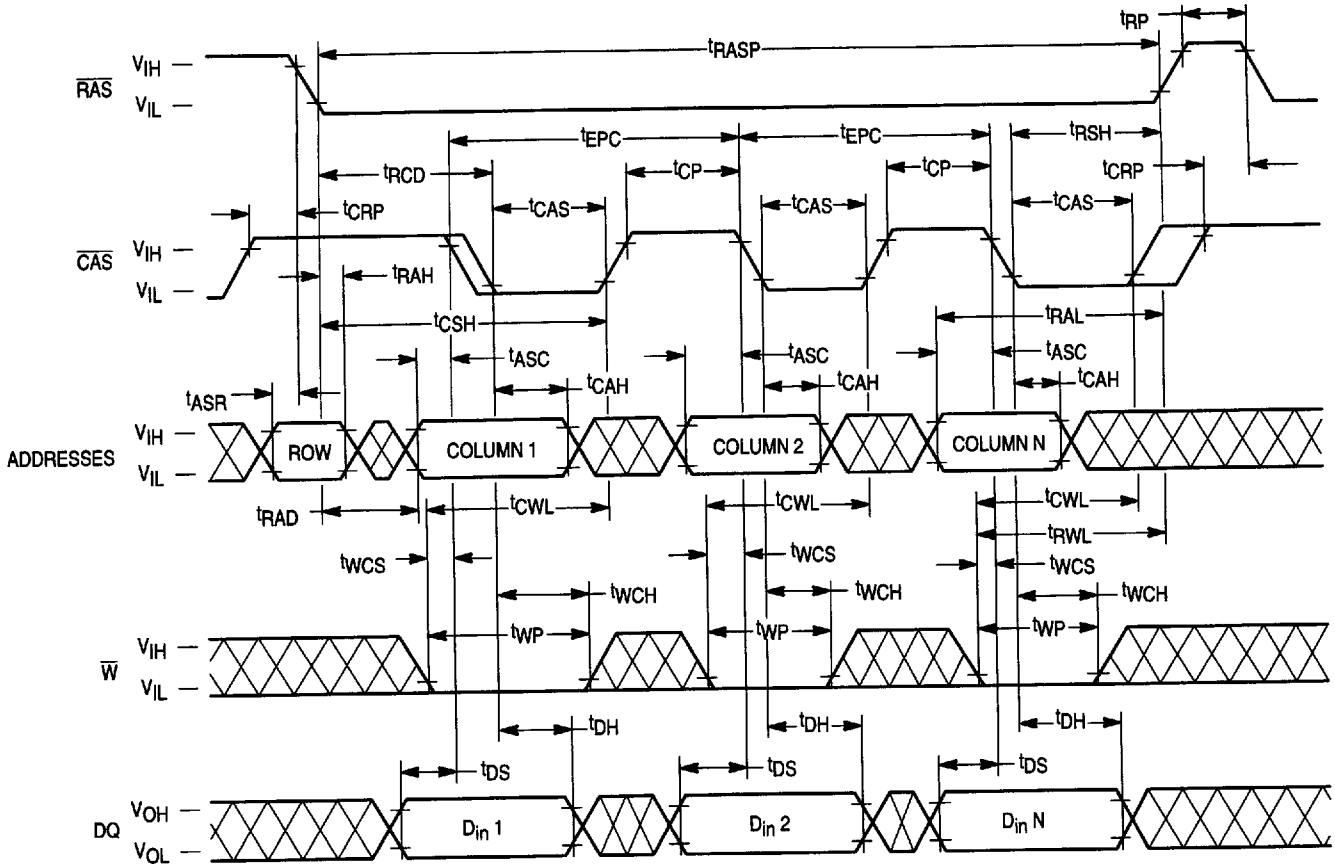
WRITE CYCLE



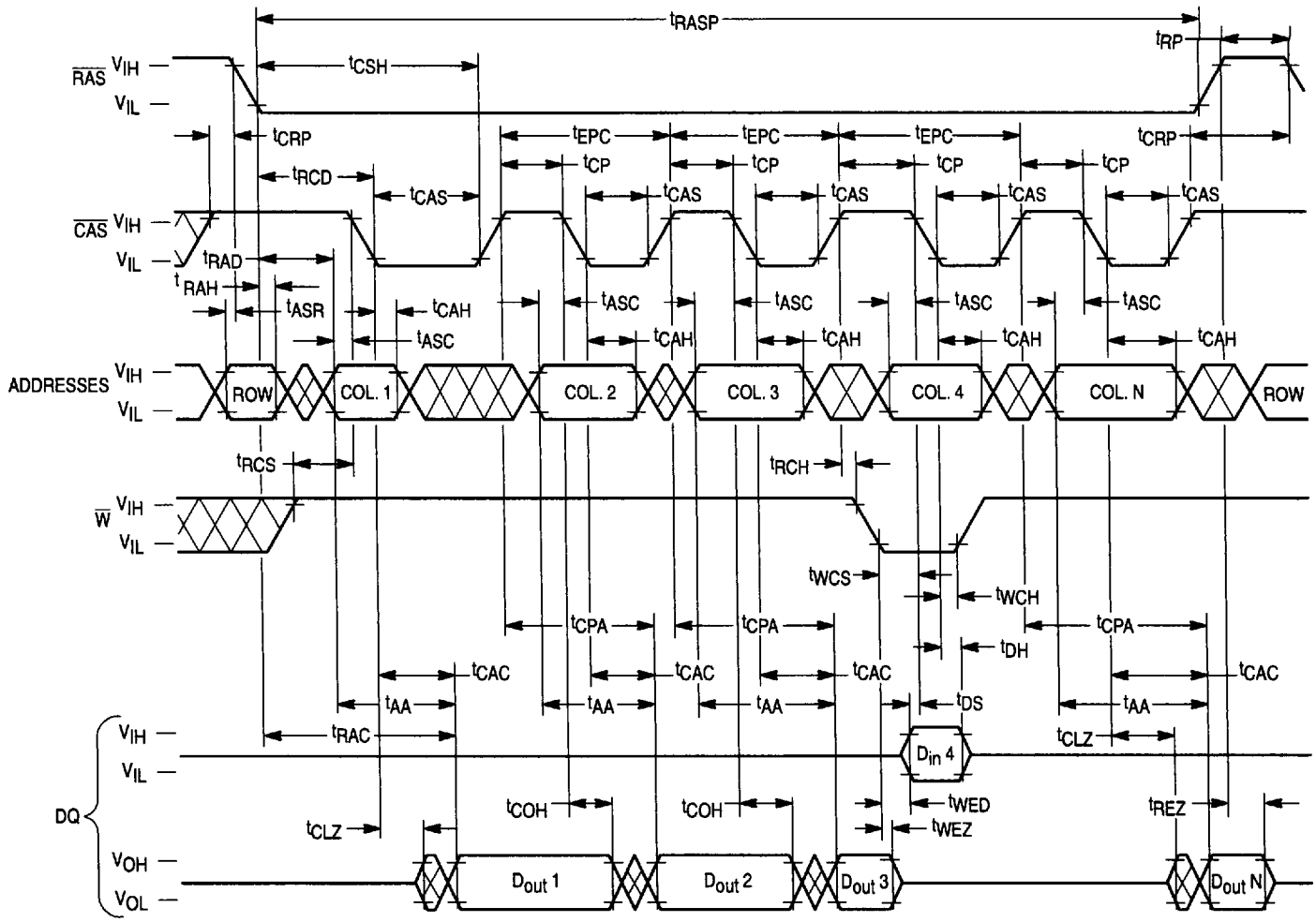
EXTENDED DATA OUT READ CYCLE



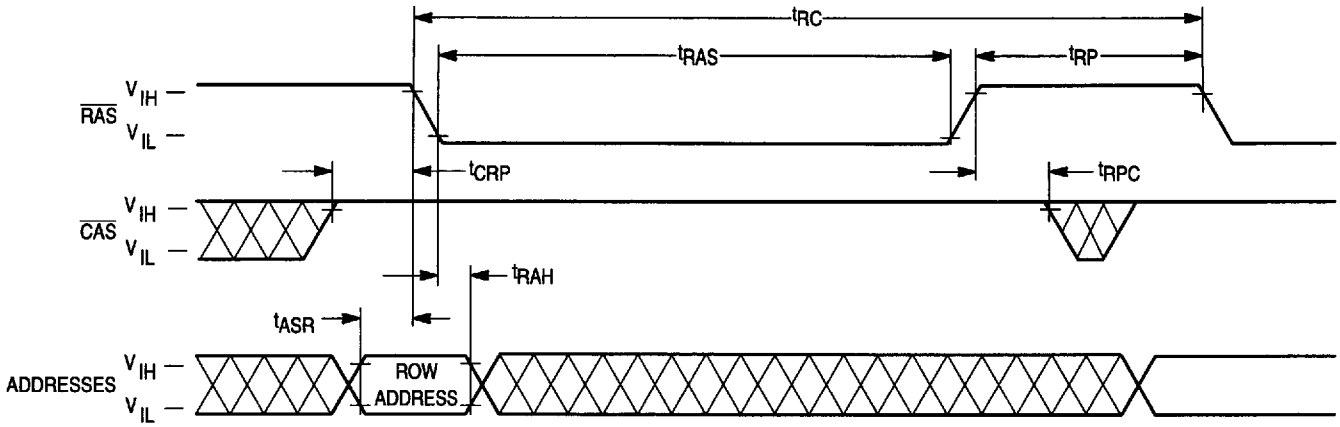
EXTENDED DATA OUT WRITE CYCLE



EXTENDED DATA OUT READ WRITE MIXED CYCLE

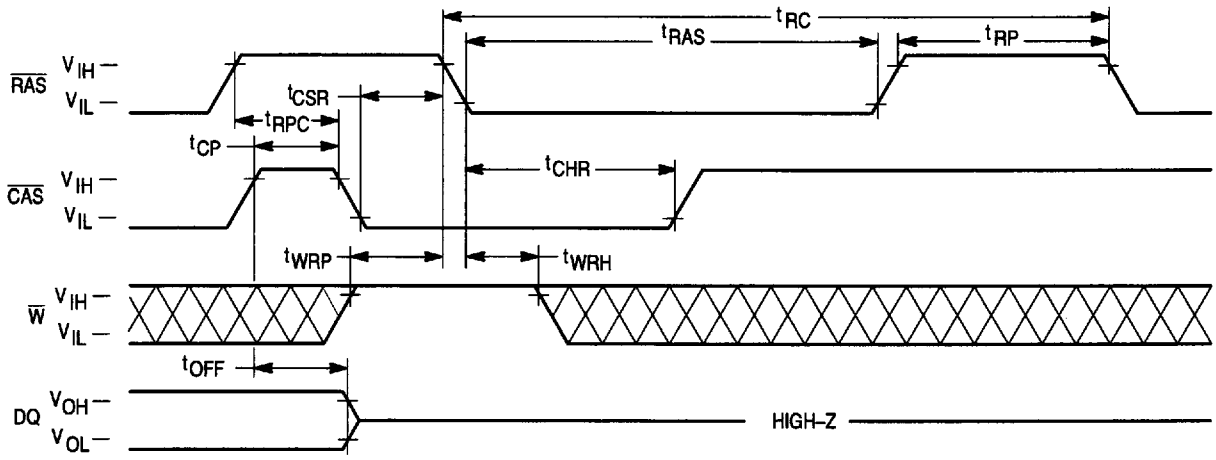


$\overline{RAS}$ ONLY REFRESH CYCLE



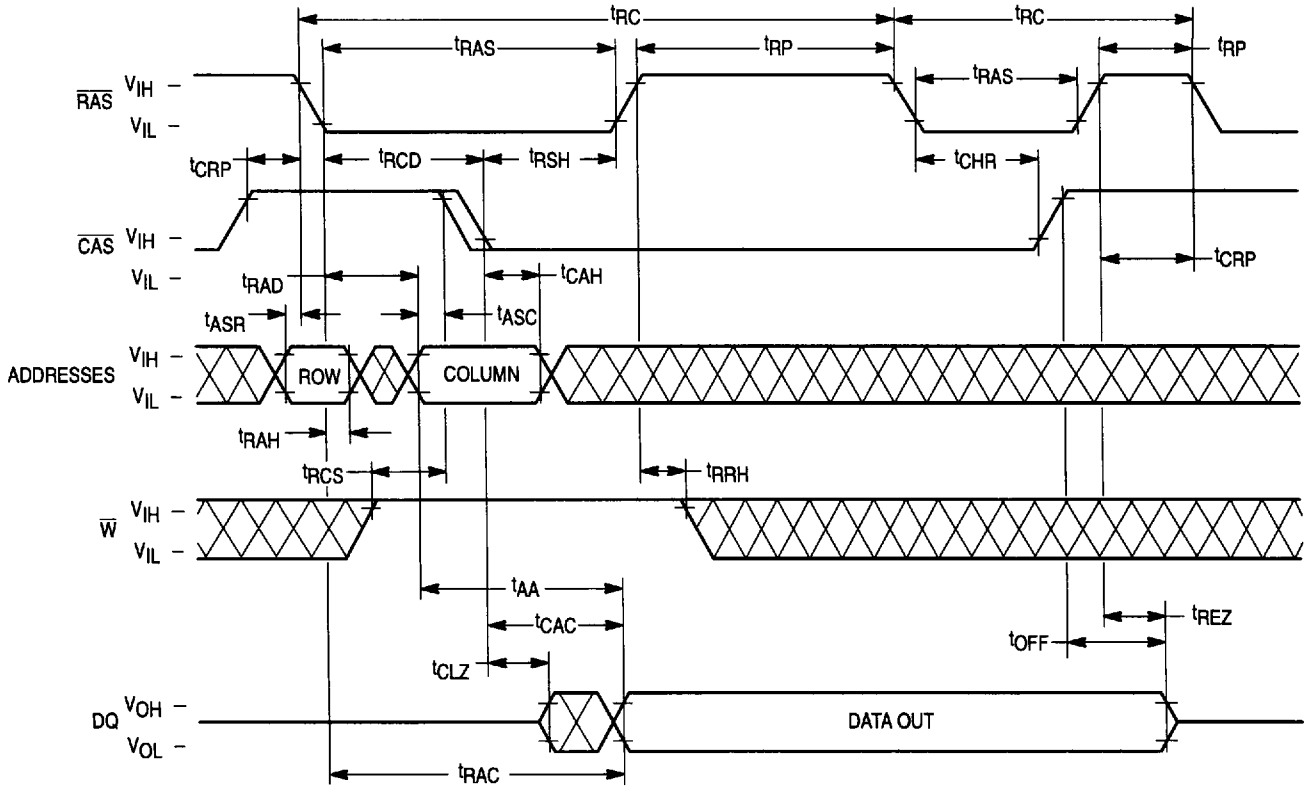
NOTE: $\overline{W}$ = H or L.
DQ = Open.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

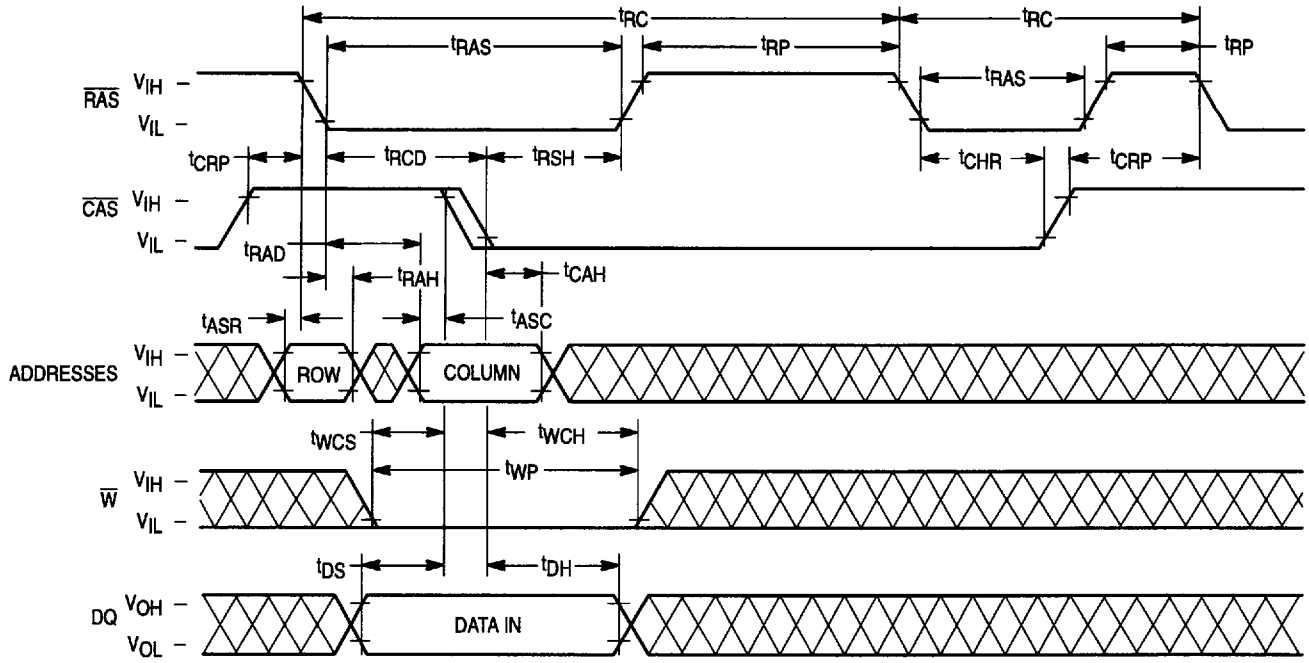


NOTE: Addresses = H or L.
16MB, 32MB: $\overline{W}$ must be as shown to avoid switching into component test mode.

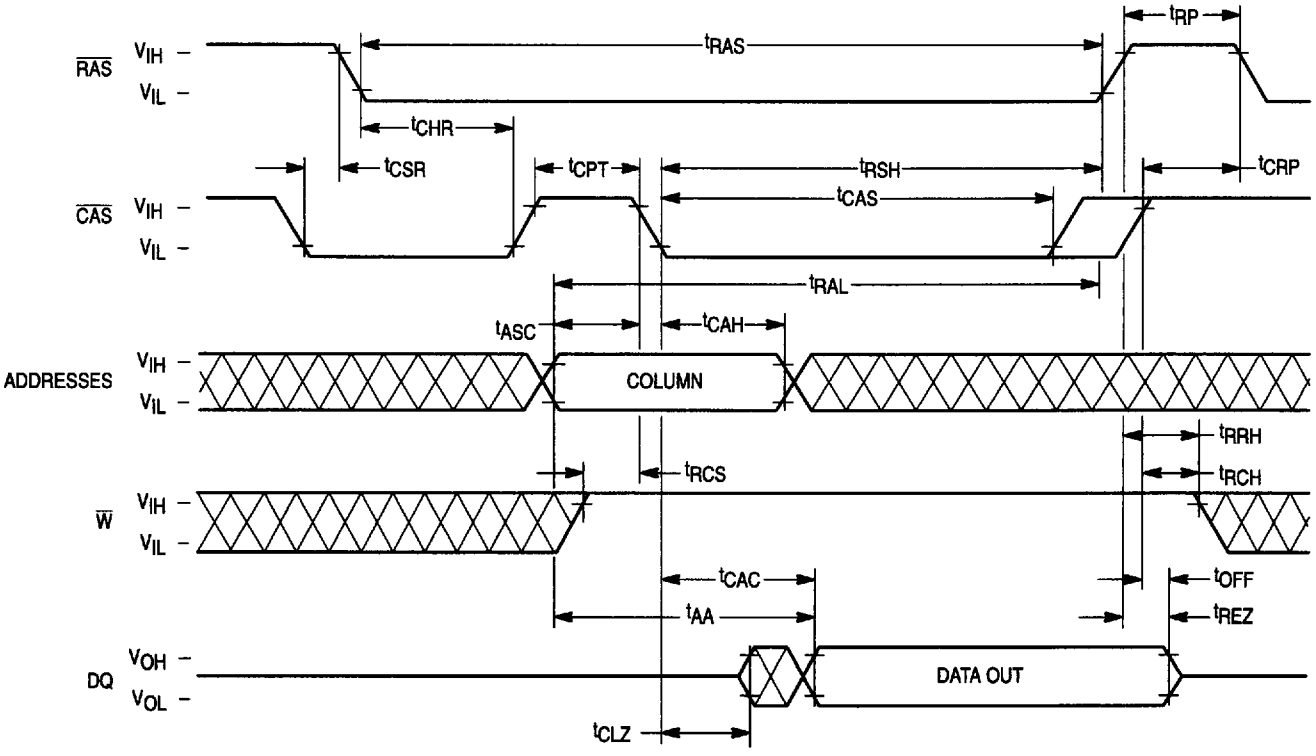
HIDDEN REFRESH CYCLE (READ)



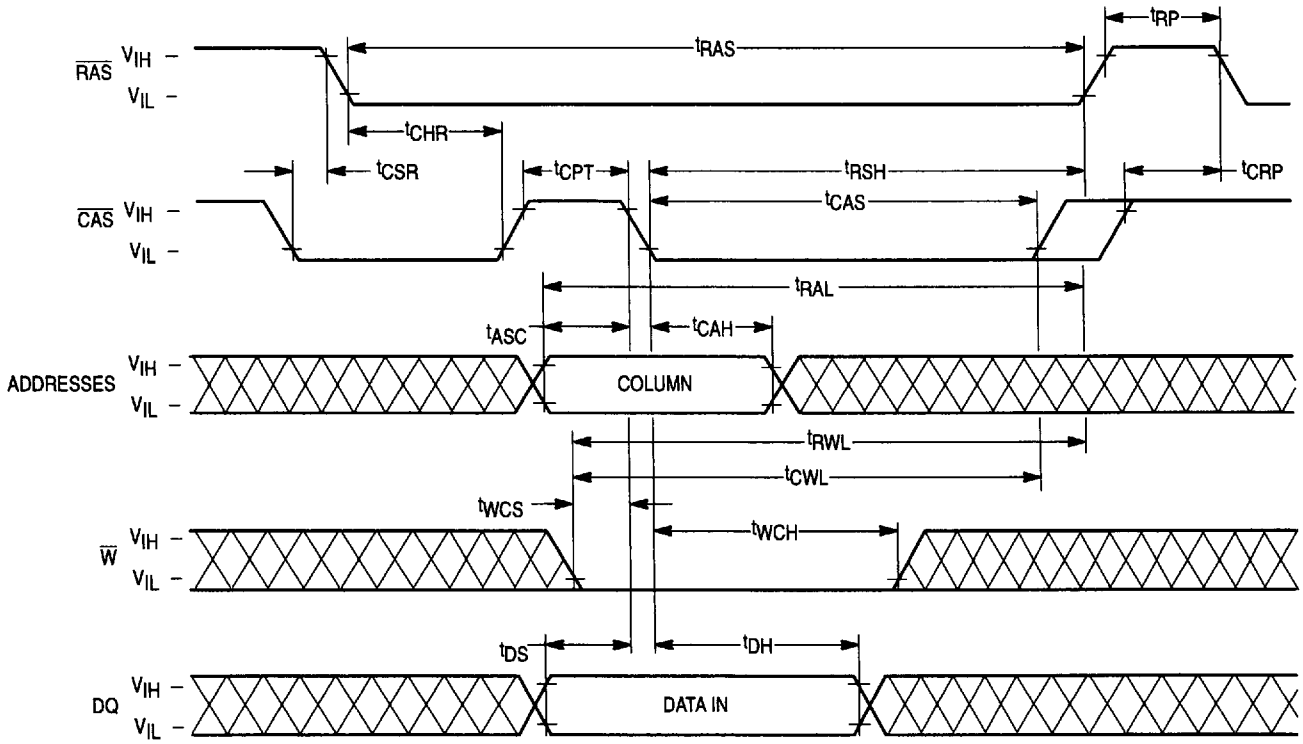
HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST READ CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 µs is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 32 ms with the device powered up for the 16MB and 32MB), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate address fields. For the 16MB and 32MB a total of 22 address bits, 11 rows and 11 columns, will decode one of the word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the module: **$\overline{RAS}$–only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or an EDO read cycle. The normal read cycle is outlined here, while the EDO mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. $\overline{CAS}$ controls read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from $\overline{RAS}$ active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the $\overline{CAS}$ clock active transition (t_{CAC}).

The $\overline{RAS}$ and $\overline{CAS}$ clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. $\overline{W}$ must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after $\overline{RAS}$ or $\overline{CAS}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{RAS}$ transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle.

WRITE CYCLE

The user can write to the DRAM with either a write or an EDO mode write cycle. The write mode is discussed here, while EDO mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Write mode is distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

A write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Data in (DQ) is referenced to $\overline{CAS}$ in a write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the write operation to complete the cycle.

EDO MODE CYCLES

EDO mode allows fast successive data operations at all column locations on a selected row of the module. Read access time in EDO mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. EDO mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$ between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

An EDO mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first EDO mode cycle (t_{EPC}). Either a read or write operation can be performed in an EDO mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive EDO mode cycles and performed in any order. The maximum number of consecutive EDO mode cycles is limited by t_{RASP}. EDO mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits require refresh every t_{RFSH}.

This is accomplished by cycling through the row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 µs. Burst refresh, a refresh of all rows consecutively, must be performed every t_{RFSH}.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decodes. Three other methods of refresh, **$\overline{RAS}$–only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$–Only Refresh

$\overline{RAS}$–only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains

high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle, while $\overline{RAS}$ cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode cycle) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after completing one cycle for every column, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 $\overline{CAS}$ before $\overline{RAS}$** initialization cycles. The test procedure is as follows:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read cycle.** Repeat this operation for every column.
3. Select a column address, and write 1 into the cell by performing **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, write cycle**. Repeat this operation for every column.
4. Read 1s (normal read mode), which were written at step three.
5. Repeat steps one through four using complement data.

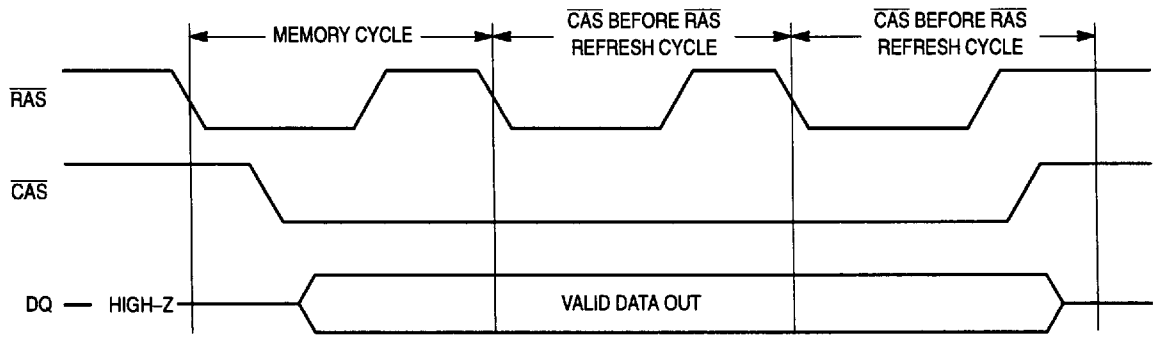
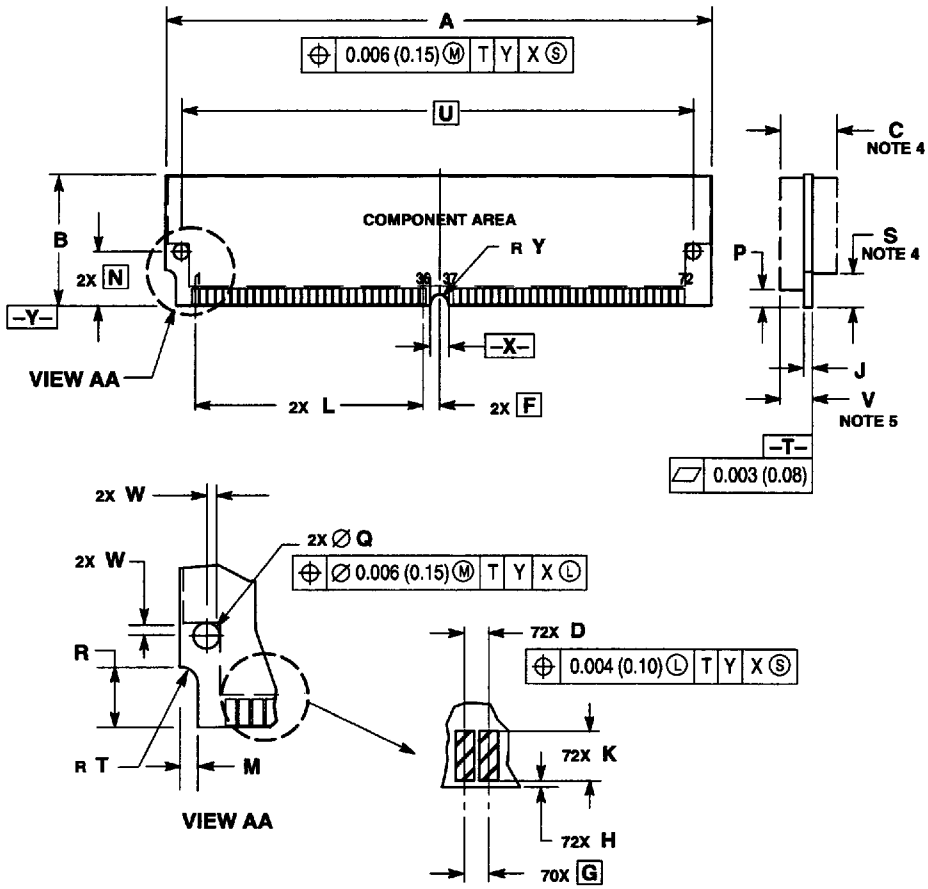


Figure 1. Hidden Refresh Cycle

PACKAGE DIMENSIONS

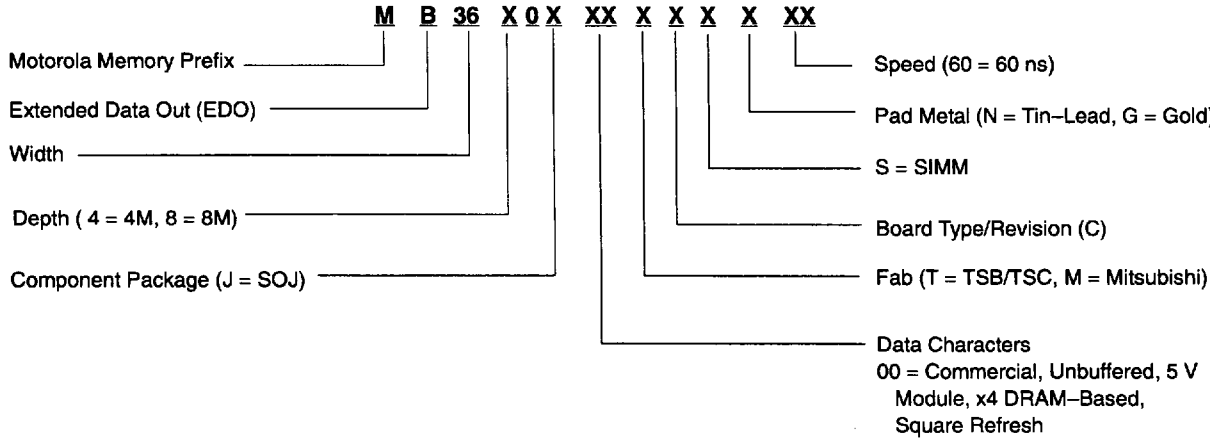
72–LEAD SIMM
CASE 866–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION:INCH
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. DIMENSIONS C AND S DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE-SIDED MODULE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.245	4.255	107.82	108.08
B	0.995	1.005	25.27	25.53
C	—	0.360	—	9.14
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.047	0.053	1.19	1.35
K	0.100	—	2.54	—
L	1.750 REF		44.45 REF	
M	0.075	0.085	1.91	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	3.984 BSC		101.19 BSC	
V	—	0.208	—	5.28
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MB3640J00TCSN60
MB3640J00TCSG60
MB3640J00MCSN60
MB3640J00MCSG60

MB3680J00TCSN60
MB3680J00TCSG60
MB3680J00MCSN60
MB3680J00MCSG60