CMS409, CMS410 8 MEGABYTE DRAM MEMORY CARDS

SMNS409A–JULY 1991–REVISED JANUARY 1993

T-81-27-15

- **Credit Card Size (85.6 mm × 54 mm × 3.4 mm)**
- **Single 5-V Power Supply (±5% Tolerance)**
- **Enhanced Page Mode Operation**
- **CMS409 – 4M × 18/1$\overline{RAS}$/2$\overline{CAS}$**
  CMS410 – 4M × 16/1$\overline{RAS}$/2$\overline{CAS}$
- **Operating Temperature 0°C to 55°C**
- **Standard 60-Pin Two-Piece Connector**
- **CMOS Buffered Inputs on All Inputs Except $\overline{RAS}$ and DQ**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Performance Ranges:**

	ACCESS TIME t_{RAC}	ACCESS TIME t_{CAC}	READ OR WRITE CYCLE t_{RC}
CMS4xx-7	70 ns	25 ns	130 ns
CMS4xx-8	80 ns	27 ns	150 ns

description

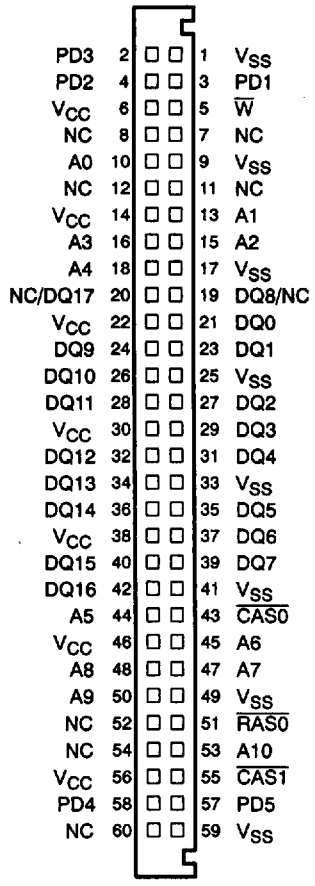
The CMS409/10 series are dynamic random-access memory cards designed to be used as internal system memory or as external add-on memory.

These cards have CMOS buffers added to the $\overline{CAS}$, $\overline{W}$, and address inputs to minimize loading caused by the module. $\overline{RAS}$ and data in/out remain compatible with Series 74 TTL.

The cards can operate in enhanced page mode. All address lines and data are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The common I/O features of the CMS409/10 dictate the use of early write cycles.

60-PIN MEMORY CARD (CONNECTOR VIEW)



PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS0}$, $\overline{CAS1}$	Column-Address Strobe
DQ0–DQ17	Data Inputs/Outputs
PD1–PD5	Presence Detect
$\overline{RAS0}$	Row-Address Strobe
V_{CC}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable
NC	No Internal Connection

operation

The CMS409/10 cards are divided into separate banks of memory as shown in the functional block diagrams. Each bank is selectable using $\overline{CASx}$ as shown in the table below.

Table 1. Memory Bank Definition

DATA BLOCK	$\overline{RAS}$	$\overline{CASx}$
DQ0–DQ7, DQ8†	$\overline{RAS0}$	$\overline{CAS0}$
DQ9–DQ16, DQ17†	$\overline{RAS0}$	$\overline{CAS1}$

† DQ8 and DQ17 are not available on CMS410.

power up

To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after full V_{CC} level is achieved. The eight initialization cycles need to include at least one refresh ($\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$) cycle.

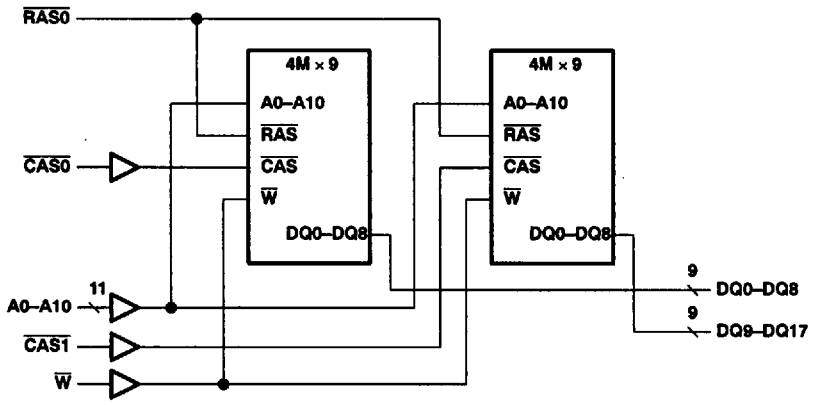
specifications

Refresh period is extended to 16 ms. During this period, each of the 1024 rows selected by A0–A9 must be strobed with $\overline{RAS}$ to retain data.

memory card components

- Meets JEDEC standard
- UL approved materials
- Plugs into molex connector part number 53213-6011 or equivalent

CMS409 functional block diagram



CMS410 functional block diagram

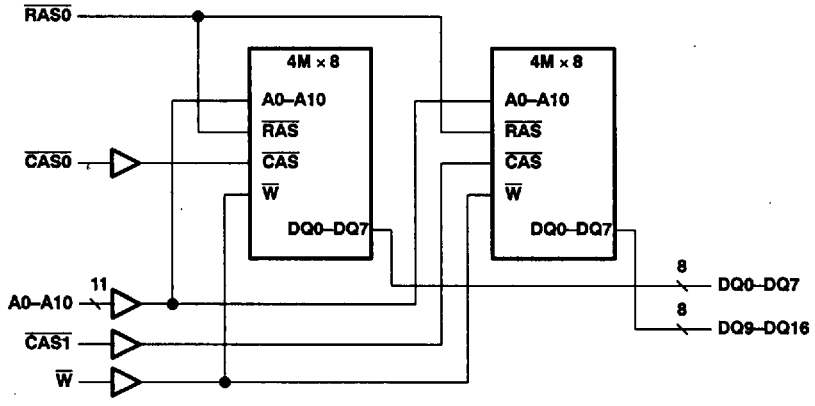


Table 2. Pin Definition

DEVICE	DQ8/NC (19)	DQ17/NC (20)
CMS409	DQ8	DQ17
CMS410	NC	NC

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Voltage range on V_{CC} ..... −0.5 V to 6 V
Short circuit output current ..... 50 mA
Power dissipation (CMS409) ..... 20 W
Power dissipation (CMS410) ..... 18 W
Operating free-air temperature ..... 0°C to 55°C
Storage temperature ..... −40 °C to 85 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{CAS}$, $\overline{W}$, address lines	0.7 V_{CC}			
		$\overline{RAS}$ and DQ lines	2.4		6.5	
V_{IL}	Low-level input voltage (See Note 2)	$\overline{CAS}$, $\overline{W}$, address lines			0.3 V_{CC}	
		$\overline{RAS}$ and DQ lines	−1		0.8	
T_A	Operating free-air temperature		0		55	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS409			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CASx}$, and $\overline{W}$	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RASx}$ (leakage)	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±180	µA
I_O	Output current (leakage)	V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{CASx}$ high			±20	µA

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS409-7		CMS409-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle (see Note 3).		1670		1490	mA
I_{CC2}	Standby current	V_{CC} = 5.25 V, After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, All other signals stable (see Note 3).		37		37	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3).		1670		1490	mA
I_{CC4}	Average page current	V_{CC} = 5.25 V, t_{PC} = minimum, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3).		1490		1310	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS409		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		126	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS410			UNIT
			MIN	NOM	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA			2.4	V
V_{OL}	Low-level output voltage	I_{IL} = 4.2 mA	0.4			V
I_I	Input current for addresses, $\overline{CAS}$x, and $\overline{W}$	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±10	µA
I_I	Input current $\overline{RAS}$x (leakage)	V_{CC} = 5 V, V_I = 0 to 5.25 V, All other pins = 0 V to V_{CC}			±160	µA
I_O	Output current (leakage)	V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{CAS}$x high			±20	µA

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	CMS410-7		CMS410-8		UNIT
			MIN	MAX	MIN	MAX	
I_{CC1}	Read or write cycle current	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle (see Note 3).		1490		1330	mA
I_{CC2}	Standby current	V_{CC} = 5.25 V After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high. All other signals stable, (see Note 3).		33		33	mA
I_{CC3}	Average refresh current ($\overline{RAS}$ only or CBR)	V_{CC} = 5.25 V, Minimum cycle, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ active, $\overline{CAS}$ high (see Note 3).		1490		1330	mA
I_{CC4}	Average page current	V_{CC} = 5.25 V, t_{PC} = minimum, Maximum of 2 address transitions per memory cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling (see Note 3).		1330		1170	mA

NOTE 3: $V_{IH} = V_{CC} - 0.2$ V and V_{IL} = 0 V for all operating currents.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		CMS410		UNIT
		MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		15	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ inputs		112	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ inputs		15	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		15	pF
$C_{i(DQ)}$	Input/output capacitance of DQ pins		14	pF

A low-power, battery-backup refresh mode is available. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of125 µs, while holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all other input levels need to be kept stable at CMOS input levels.

All values remain the same as the standard memory card except those listed in the following table:

PARAMETER		TEST CONDITIONS	CMS409L	CMS410L
I_{CC2}	Standby current	$\overline{RAS}$ and $\overline{CAS}$ high, $V_{IH} = V_{CC}-0.2$, V, $V_{IL} = 0$ V All other signals stable at V_{IH} or V_{IL}	7 mA	6 mA
I_{CC10}	Battery backup current	t_{RC} = 125 µs, t_{RAS} < 1 µs, $V_{IH} = V_{CC}-0.2$ V, V_{IL} = 0 V All other signals stable at V_{IH} or V_{IL}	10 mA	9 mA
t_{REF}	Refresh	1024 cycle	128 ms	128 ms

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		CMS4xx-7		CMS4xx-8		UNIT
		MIN	MAX	MIN	MAX	
t_{CAC}	Access time from $\overline{CAS}$ low		25		27	ns
t_{CAA}	Access time from column-address		42		47	ns
t_{RAC}	Access time from $\overline{RAS}$ low		70		80	ns
t_{CAP}	Access time form column precharge		47		52	ns
t_{CLZ}	$\overline{CAS}$ low to output in low Z	0		0		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 4)	0	25	0	27	ns

NOTE 4: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		CMS4xx-7		CMS4xx-8		
		MIN	MAX	MIN	MAX	
t_{RC}	Read cycle time	130		150		ns
t_{WC}	Write cycle time	130		150		ns
t_{PC}	Page mode read or write cycle time (see Note 5)	52		57		ns
t_{CP}	Pulse duration, $\overline{CAS}$ high	10		10		ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low	25	10 000	27	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high	50		60		ns
t_{RAS}	Pulse duration, $\overline{RAS}$ low	70	10 000	80	10 000	ns
t_{RASP}	Page mode, pulse duration, $\overline{RAS}$ low	70	100 000	80	100 000	ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	0		0		ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	7		7		ns
t_{DS}	Data setup time before $\overline{CAS}$ low	0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		ns
t_{WCS}	$\overline{W}$-low setup before $\overline{CAS}$ low	0		0		ns
t_{CWL}	$\overline{W}$-low setup before $\overline{CAS}$ high	18		20		ns
t_{RWL}	$\overline{W}$-low setup before $\overline{RAS}$ high	25		27		ns
t_{WSR}	$\overline{W}$-high setup ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	17		17		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{AR}	Column address hold time after $\overline{RAS}$ low (see note 6)	55		60		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	15		15		ns
t_{DHR}	Data hold time after $\overline{RAS}$ low	55		60		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 7)	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 7)	0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{WCR}	Write hold time after $\overline{RAS}$ low (see Note 6)	55		60		ns
t_{WHR}	$\overline{W}$-high hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	70		80		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	7		7		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	25		27		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 8)	20	47	22	53	ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 8)	15	28	15	33	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	42		47		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	35		40		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 9)	15		20		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 9)	17		17		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 9)	0		0		ns
t_{REF}	Refresh time interval		16		16	ns
t_T	Transition time (see Note 10)	3	50	3	50	ns

NOTES: 5. To assure t_{PC} min, t_{ASC} should be greater than or equal to 5 ns..
6. The minimum value is measured when t_{RCD} is set to t_{RCD}(min) as a reference.
7. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
8. Maximum values specified to assure access times.
9. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.
10. All cycle times assume t_T = 5 ns.

TI memory card nomenclature