EPSON

SPC8104F

Low Voltage VGA LCD Controller

■ DESCRIPTION

The SPC8104 is a low power, mixed voltage video controller based on VGA architecture and optimized for driving a 640×480 LCD panel display. VGA standard mode functionality is supported using standard IBM VGA parameters. A proprietary 64×6bit gray scale lookup table is provided to allow remapping of the 16 possible gray shades displayed on an LCD panel.

The target markets for this device are small, cost sensitive mixed 3.3V/1.5-2.8V sub-notebook computers, or other specialized consumer products where low cost, low power consumption, low component count, and the ability to run most VGA software on a 640×480 LCD panel display are the major design considerations. This chip is intended to operate mainly in planar graphics modes (e.g. mode 12H) and will display 16 levels of gray.

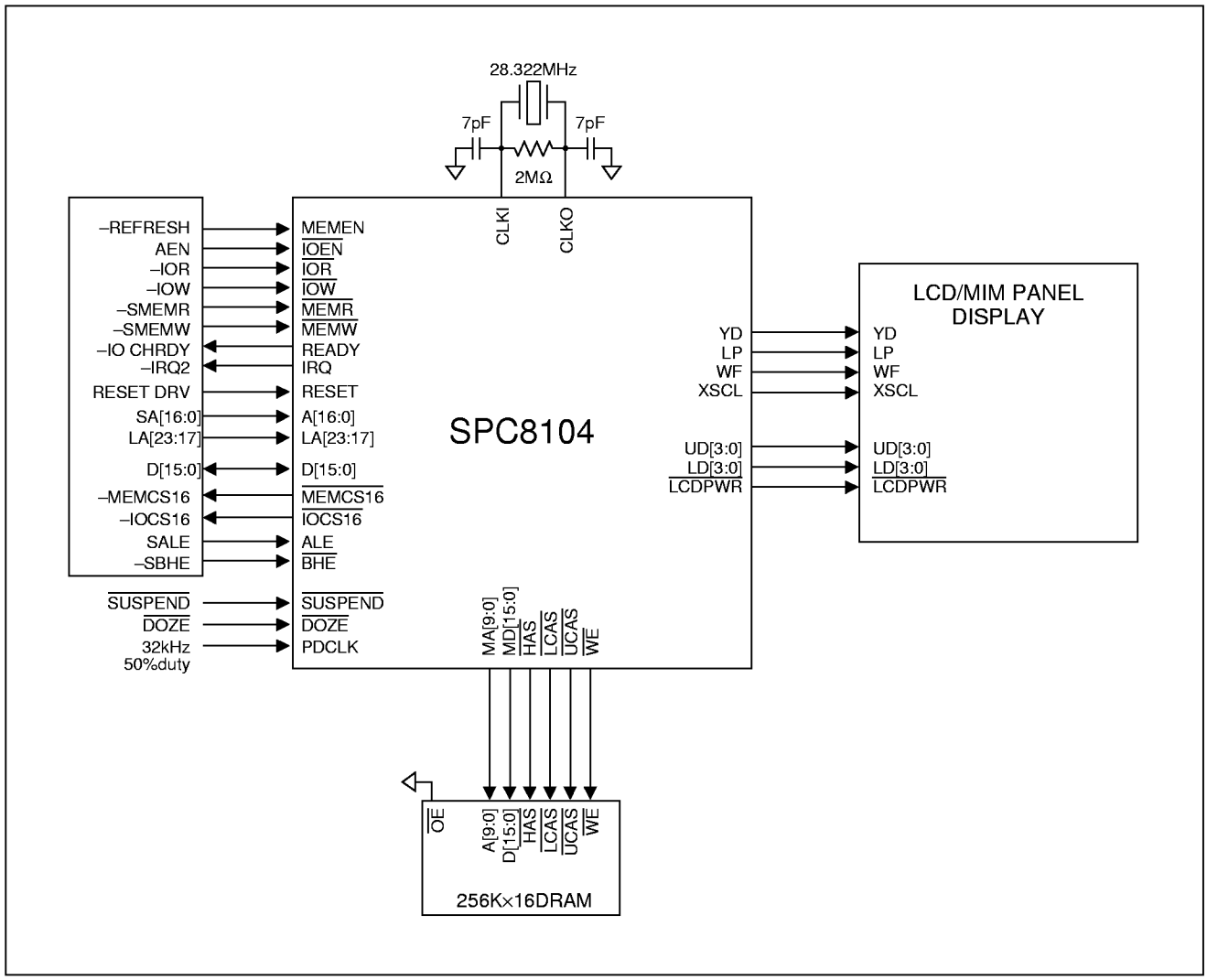
■ FEATURES

- ow-power CMOS technology
- Hardware VGA compatible except mode 13h
- 16bit ISA CPU data bus interface bus
- One 256K×16 self-refresh DRAM
- Video BIOS, software driver and utility support
- Single two-terminal crystal support
- Three hardware or software power-save modes
- 3.3 V I/O operation (1.5 to 2.8 V core)
- Monochrome LCD panel interface, for sizes 320× 200 to 640×480
- On-chip 64×4 gray-scale look-up table
- 16 gray shades by frame rate modulation
- Package: QFP15-100pin (plastic)

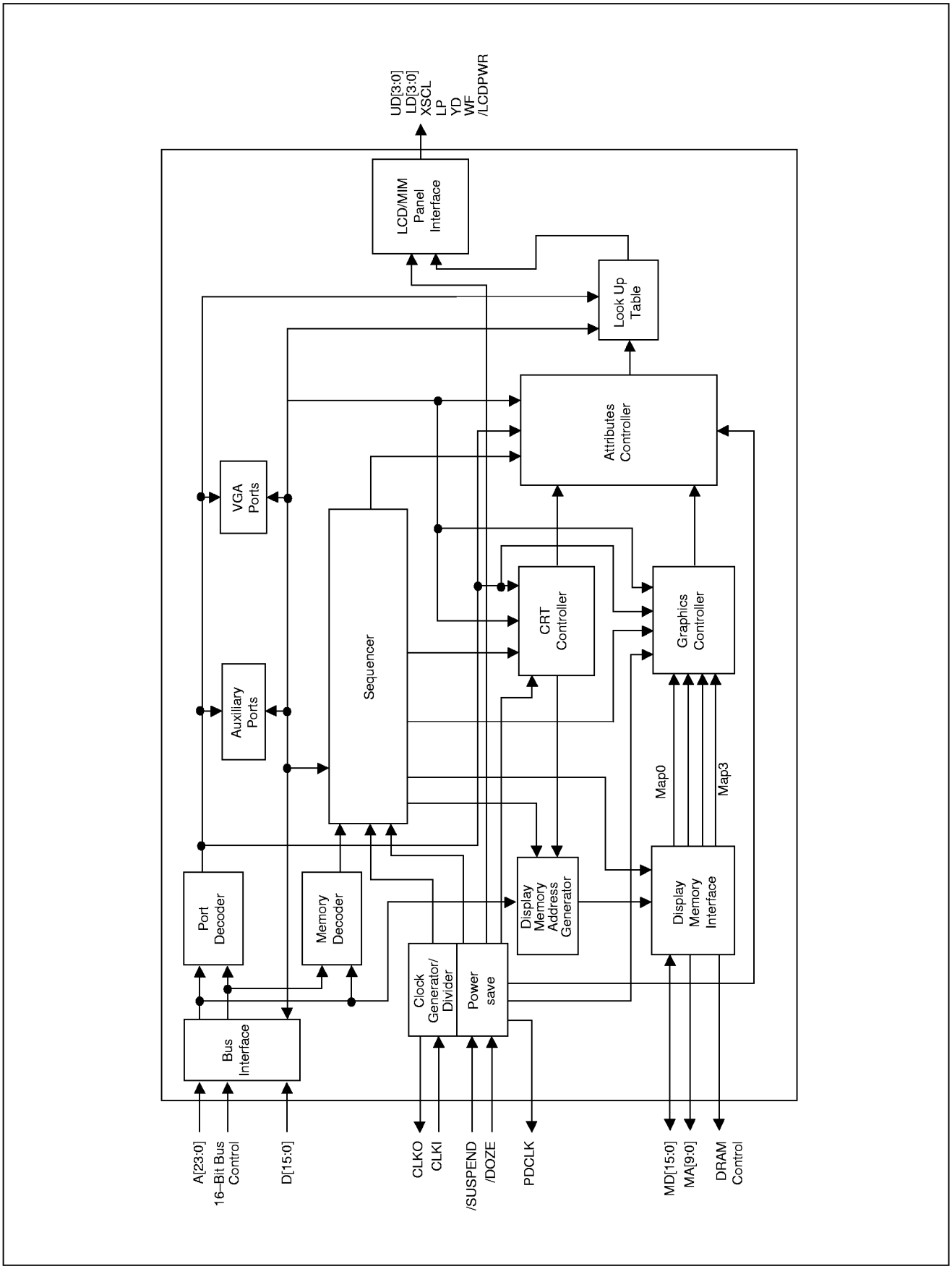
■ SUPPORTED LCD PANELS

8-bit Interface				4-bit Interface	
Dual Panel		Single Panel		Single Panel	
Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical
640	400 480	640	400 480	320 480 640	200 240 320 400 480

■ TYPICAL SYSTEM BLOCK DIAGRAM

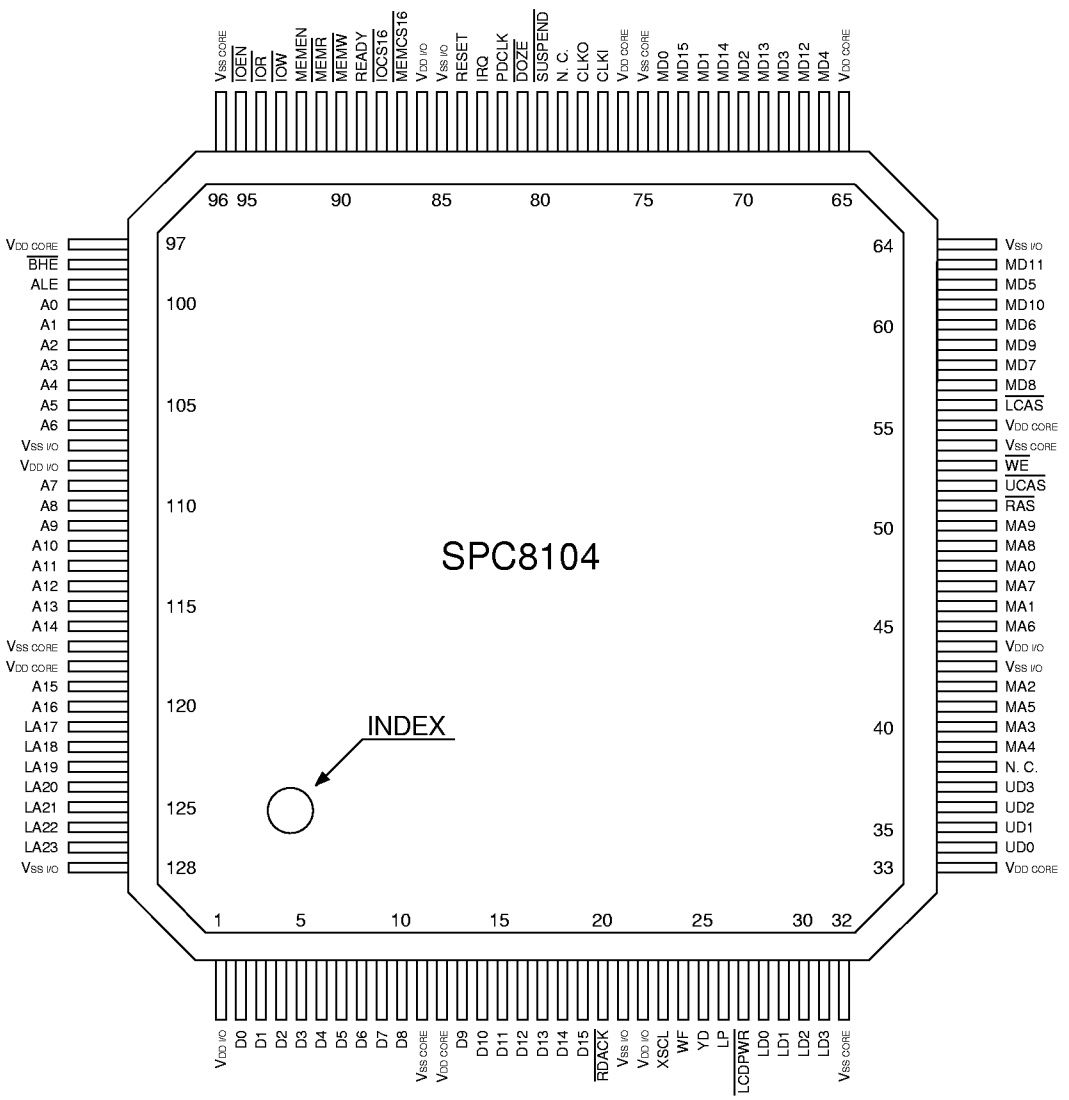


■ INTERNAL BLOCK DIAGRAM



■ PIN CONFIGURATION

QFP15-100pin



N. C.: No Connection

Note: Package type: 128 pin surface mount QFP15.

■ PIN DESCRIPTION

●Key

C =CMOS level input
CS =CMOS level input with hysteresis
COx =CMOS level output, x denotes output driver type-see DC characteristics for rating.
TSx =Tri-state CMOS level driver, x denotes driver type-see DC characteristics for rating.
TSxU =Tri-state CMOS level driver with 100 kΩ pull up resistor, x denotes driver type-see DC characteristics for rating.

● CPU Interface

Pin Name	I/O	Pin No.	Drv	Function
A[0:16] LA[17:23]	I	100..106, 109..116, 119..127	C	CPU bus address inputs. For an 8-bit CPU interface configuration, LA[20:23] are ignored and LA[17:19] should be connected to the latched CPU address SA[17:19]. In Suspend Mode, the Address inputs are internally masked off.
D[0:15]	I/O	2..10, 13..19	C /CO2	16 bit ISA-Bus data bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times. In Suspend Mode, these iputs are internally masked off.
ALE	I	99	C	ISA Bus Address Latch Enable. ALE is ignored for an 8-bit CPU interface configuration. In Suspend Mode the this input is disabled.
MEMEN	I	92	CS	ISA Bus Memory Enable. This signal should be connected to the /REFRESH signal on the ISA bus. When this signal is low(e. g. during a system memory refresh cycle), memory address decoding is disabled.
/IOR	I	94	C	ISA Bus I/O Read Strobe. In Suspend Mode the this input is disabled.
/IOW	I	93	C	ISA Bus I/O Write Strobe. In Suspend Mode the this input is disabled.
/MEMR	I	91	C	ISA Bus Memory Read Strobe. In Suspend Mode the This input is disabled.
/MEMW	I	90	C	ISA Bus Memory Write Strobe. In Suspend Mode the this input is disabled.
/IOEN	I	95	CS	ISA Bus I/O Enable. This input should be connected to the ISA bus AEN signal. When this signal is high, I/O address decoding is disabled. In Suspend Mode the this input is disabled.
READY	O	89	TS2	ISA Bus READY signal. This output is driven low to force the CPU to insert wait states during memory cycles. READY is released to high-Z after a transfer is complete.
RESET	I	84	CS	The active high Reset signal from the CPU clears all internal registers and forces all signals to their inactive state. During Suspend Mode the RESET input is ignored.
IRQ	O	83	TS2	ISA Bus Vertical Interrupt. When enabled, a Vertical Retrace interrupt will cause this signal to be driven from a logic 0 state to a logic 1(rising-edge tnggered interrupt). Once set, this interrupt must be cleared by a bit in the CRTC registers. A control bit in the Auxiliary Registers allows this output to be optionally disabled (tri-stated).
/MEMCS16	O	87	TS3	ISA Bus Memory Chip Select 16. Address inputs LA[23:17] are decoded to drive this output low when a valid memory address (AXXXXH, BXXXXH) appears on the 3 bus.

/IOCS16	O	88	TS3	ISA Bus I/O chip Select 16. Address inputs A[15:0] and/IOEN are decoded to drive this output low when a valid SPC8104 I/O register address appears on the bus. Note that I/O addresses 3C6H-3C9H doe not result in/IOCS 16 being driven low(i. e. internal LUT register reads and writes are 8 bit cycle).
/BHE	I	98	C	ISA Bus Byte High Enable. In Suspend Mode the this input is disabled.
/RDACK	O	20	C	Read Acknowledge. Thes pin goes low during valid IO or memory reads to the chip.

● Video Memory Interface

Pin Name	I/O	Pin No.	Drv	Function
MA[0:9]	O	48, 46, 42, 40, 39, 41, 45, 47, 49, 50	CO2	Multiplexed row/column address bits for video display memory.
MD[0:15]	I/O	74, 72, 70, 68, 66, 62, 60, 58, 57, 59, 61, 63, 67, 69, 71, 73	C/ TSU2	Data bits for video display memory. The output drivers of there pins are placed into a high-impedance state when RESET is high, or when the Sequencer is in a reset state. On the falling edge of RESET, the values on MD[3:0] are latched into a read-only Auxiliary Register and are available to be read as configuration inputs. Also, the values on MD[4:8]are used to configure other various hardware options-see sammary of Coufiguration Options for details. Note that there are internal pullup resistors on the inputs of these Pins.
/RAS	O	51	CO3	DRAM Row Address Strobe.
/LCAS (/LWE)	O	56	CO3	DRAM Column Address Strobe for low byte(/LCAS), or Write Enable Strobe for low byte(/LWE), as determined by logic value on MD[6]during RESET(see pin mapping table).
/UCAS (/CAS)	O	52	CO3	DRAM Column Address Strobe for high byte(/UCAS), or single Column Address Strobe(/CAS), as determined by logic value on MD[6]during RESET(see pin mapping table).
/WE (/UWE)	O	53	CO3	DRAM Write Enable Strobe(/WE), or Write Enable Strobe for high byte(/UWE), as determined by logic value on MD[6] during RESET(see pin mapping table).

● Video Memory Interface Options

Note: the logic values at pin MD [6] during RESET is used to determine memory configuration (1-256K×16 with "2 CAS with 1 WE"or "1 CAS with 2 WE" type DRAMs. The pinout diagram is labelled with the pin names for the default configuration of single 256K×16DRAM with 2 CAS and 1 WE signals. The MD[6] pin has an internal pullup resistor, so no external resistor is required for this default case. Refer to the following table for details.

MA[6]	#DRAM/size	CAS/WE Configuration
0	1/256K×16	1CAS, 2WE
1	1/256K×16	2CAS, 1WE

● PIn mapping for various DRAM configurations

Non-italicized pin names are the default configuration and correspond to the names on the pinout diagram.

Pin. No.	MA[6]=1	MA[6]=0
52	/UCAS	/CAS
53	/WE	/UWE
56	/LCAS	/LWE

● Address Mapping for 256K¥16DRAMs

Two addressing configurations of 256K×16 DRAMs are supported by the SPC8104:
1024×256×16 10 row address bits×8 column address bits
512×512×16 9 row address bits×9 column address bits
The SPC8104 is designed to accomodate both types of 256K×16 DRAMs directly without any special configuration options required. The full addressing space is available for either memory configuration. The only difference is that in the installation of the 10×8 type of DRAM, an extra row/column address output pin of the SPC8104(MA[9]) must be connected to the DRAM. For the 9×9 DRAM, only 9 row / column address pins exist, so MA[9] from the SPC8104 is left unconnected.
The following tables summarize the mapping of the SPC8104's internal memory address bits a[17:0] to the multiplexed row/column address outputs MA[9:0] for the two types of DRAM.

1) For the 10×8 type DRAMs:

	MA[9]	MA[8]	MA[7:0]
row addr	a[17]	a[16]	a[15:8]
column addr	–	a[17]	a[7:0]

2) For the 9×9 type DRAMs:

	MA[9]	MA[8]	MA[7:0]
row addr	n/c	a[16]	a[15:8]
column addr	n/c	a[17]	a[7:0]

Notes:

- The address pin mapping for both types of DRAM are actually the same.
- for the standard 256K byte VGA address space, a[17]is nornally=0, and for the upper 256K bytes, a[17]=1.
- the 10×8 type DRAM does not use the 9th column bit MA[8]-it is ignored.
- a[17]is output on the 9th column bit MA[8], so the same physical addressing scheme works for both 10×8 and 9×9 type DRAMs. In the case of the 10×8 type DRAM, this 9th column address bit is not used by the DRAM(italicized in the above table).
- the 9×9 configuration does not have a 10th row/column address bit.

● Clock Inputs

Pin Name	I/O	Pin No.	Drv	Function
CLKI	I	77	•	This pin, along with CLKO is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin is the clock input.
CLKO	O	78	•	This pin, along with CLKI is the 2-terminal crystal interface when using a 2-terminal crystal as the clock input. If an external oscillator is used as a clock source, then this pin should be left unconnected.

● LCD Panel Interface

Pin Name	I/O	Pin No.	Drv	Function
YD	O	25	TS4	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	26	TS4	Latch Pulse output. The falling edge of this signal is used to latch a row of display data in the LCD module's column driver shift registers and to turn on the row driver (Y driver) for that line.
XSCL	O	23	TS4	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers (X drivers) on each falling edge.
UD[0:3]	O	34..37	TS4	Upper panel display data for dual panel mode. For single panel mode, these bits are the most significant 4 bits of the 8 bit output data to the panel (PD[4:7]). For 4-bit single panel mode, these bits are the 4 bits of output data to the panel.
LD[0:3]	O	28..31	TS4	Lower panel display data for dual panel mode. For 8-bit single panel mode, these bits are the least significant 4 bits of the 8 bit output data to the panel(PD[0:3]). For 4-bit single panels, these bits are driven 0.
/LCDPWR	O	27	CO2	LCD power control. In normal operation this signal is driven low to enable an external LCD power supply. This signal is driven high when the chip is put into any power save mode, or if the Sequencer is in a reset state. It can be used externally to turn off the panel supply voltage and backlight. After a RESET, this signal is held high until the CRTC is programmed and running.
WF	O	24	CO2	LCD Backplane Bias Signal. The WF signal toggles once per vertical frame period.

● Power Save Mode Control

Pin Name	I/O	Pin No.	Drv	Function
/SUSPEND	I	80	CS	A low level on this pin puts the chip into the hardware Suspend mode. The/SUSPEND signal overrides any software initiated power save modes as well as the/DOZE input pin, and disables the bus interface inputs. Address and Data inputs are also masked when this signal is low. When in Suspend Mode the UD[3:0], LD[3:0], XSCL, LP, YD and WF signals are driven into a high impedance state(or optionally, a low state)and the/LCDPWR signal is driven high.
/DOZE	I	81	CS	A low level on this pin puts the chip into Doze mode. The function of the Doze mode is determined by the Doze Mode Select bits in Aux[03h]. This pin is ignored if the /SUSPEND input pin is asserted.
PDCLK	I	82	C	Power Down clock. This input may be used in to provide a low frequency clock for generating refresh in Suspend mode, as an optional alternative to using the pixel clock or MEMEN input as the refresh clock source. This clock input should be driven by either a 32kHz 50% duty cycle clock, or a 64 kHz clock source with a low period as short as possible(but>min RAS pulse width, typically 100ns) to minimize DRAM current consumption during refresh. The PDCLK input is used to directly generate the RAS and CAS pulses during Suspend.

● Power Supply

Pin Name	I/O	Pin No.	Function
VDD CORE	P	12, 33, 55, 76, 97, 118	VDD supply for core logic.
VDD I/O	P	1, 22, 44, 65, 86, 108	VDD supply for I/O pins.
Vss CORE	P	10, 32, 54, 75, 96, 117	Vss supply for core logic.
Vss I/O	P	21, 43, 64, 85, 107, 128	Vss supply for I/O pins.

● Summary of Configuration Options

Pin Name	value on this pin at falling edge of RESET is used to configure: (1/0)
MD[3:0]	values latched into read-only Aux Reg [0C]bits 7:4 for software use
MD[4]	16-bit CPU interface(1), or 8-bit CPU interface (0)
MD[5]	reserved
MD[6]	2 CAS, 1WE type DRAM (1), or 1CAS, 2 WE type DRAM (0)
MD[7]	reserved
MD[8]	use 64 kHz PDCLK clock source (1), or 32 kHz PDCLK clock source

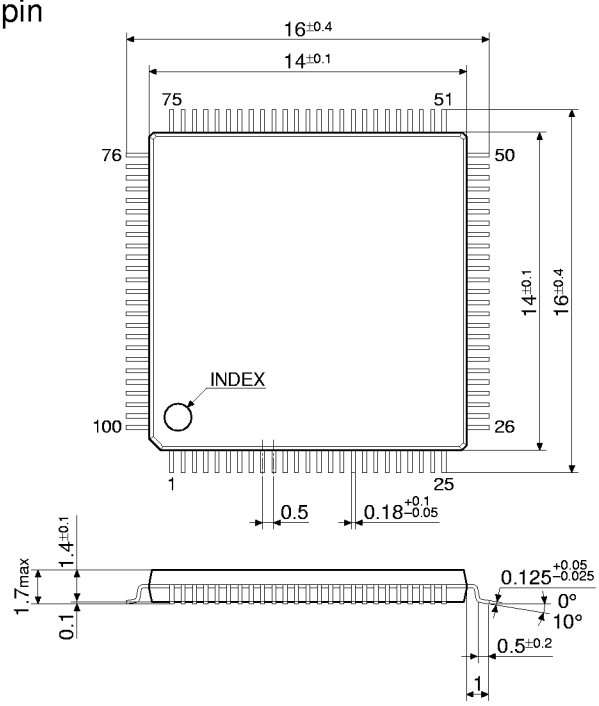
These inputs have internal pullup resistors.
These inputs have internal pullup resistors. Based on the value of the internal pull-ups, the external pull-down resistors if necessary, should be aproximately 15K ohm. This value will provide the correct voltage levels on power-up without loading the DRAM Data lines (V_{DD} = 3.3V).

● Multiple Function Pin Descriptions

Pin Name	MD Line Status	Function
/LCAS	MD [6]=1	DARM Column Address Strobe (Low Byte)
/LWE	MD [6]=0	DRAM Write Enable Strobe
/UCAS	MD [6]=1	DRAM Column Address Strobe (High Byte)
/CAS	MD [6]=0	DRAM Column Address Strobe
/WE	MD [6]=1	DRAM Write Strobe
/UWE	MD [6]=0	DRAM Write Strobe (High Byte)

■ PACKAGE DIMENSIONS

Plastic QFP15-100 pin



Unit : mm