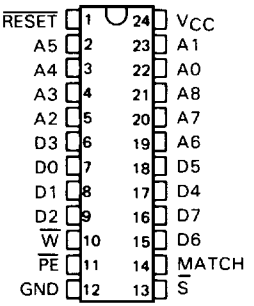
D2993, JANUARY 1987 – REVISED SEPTEMBER 1987

- **Address to MATCH Valid Time**
  TACT2150-20 . . . 20 ns max
  TACT2150-30 . . . 30 ns max
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **53 mA Typical Supply Current**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

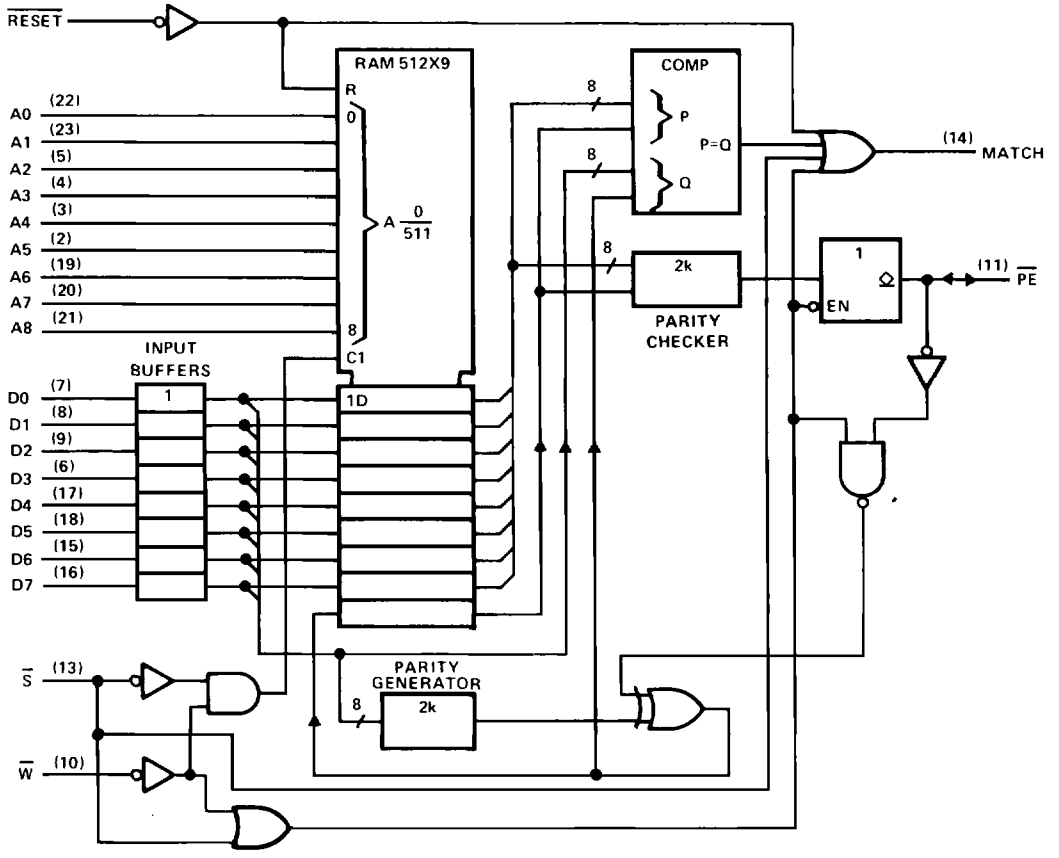
This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using Advanced CMOS technology for high-speed, low-power interface with bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The TACT2150 operates from a single 5 V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH}, $\overline{RESET}$ = V_{IH}

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PIN FUNCTIONAL DESCRIPTION

PIN NAME	PIN NO.	DESCRIPTION
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provide input data to RAM when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}.
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
GND	12	Ground
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
$\overline{PE}$	11	Parity error input/output. During write cycles, $\overline{PE}$ can force a parity error into the 9-bit location specified by A0 through A8 when $\overline{PE}$ is at V_{IL}. For compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
$\overline{RESET}$	1	$\overline{RESET}$ input. Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ is at V_{IL} and $\overline{W}$ is at V_{IH}.
$\overline{S}$	13	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ is at V_{IH}.
V_{CC}	24	5-V supply voltage
$\overline{W}$	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}. Places selected device in compare mode if $\overline{W}$ is at V_{IH}.

application

Due to the high-performance switching characteristics of the TACT2150, it is necessary that the address inputs not be allowed to float. Proper termination techniques should be employed. It is recommended that the RC time constant associated with the address inputs (63.2% of rise time on A0-A8) not exceed 60 ns.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 to 7 V
Input voltage range, any input . . . . . −1.5 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage	$\overline{PE}$			5.5	V
I_{OH}	High-level output current	MATCH			−8	mA
I_{OL}	Low-level output current	MATCH			8	mA
		$\overline{PE}$			16	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TACT2150-20			TACT2150-30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	I_{OH} = −8 mA, V_{CC} = 4.5 V	2.4			2.4			V
		I_{OH} = −20 μA, V_{CC} = 4.5 V	3.5			3.5			
$V_{OL(M)}$	MATCH low-level output voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	I_{OL} = 16 mA, V_{CC} = 4.5 V,			0.4			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V			10			10	μA
I_{OS}	Short-circuit MATCH output current	V_O = GND, V_{CC} = 5.5 V			−150			−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		53	95		53	95	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_L		2.75	6		2.75	6	mA
C_i	Input capacitance	f = 1 MHz			5			5	pF
C_o	Output capacitance	f = 1 MHz			6			6	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

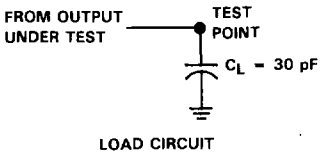
PARAMETER		TACT2150-20		TACT2150-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		20		30	ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		22		30	ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		30		35	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		10		15	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		15		20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		10		15	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		10		12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		10		12	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		15		20	ns
$t_{v(A-M)}$	MATCH valid time after change of address	3		3		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	5		5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TACT2150-20		TACT2150-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		40		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	20		25		ns
$t_{wPE(WL)}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	20		25		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	20		25		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	20		25		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	20		25		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		0		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	0		0		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		0		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		ns
t_{AVWH}	Address valid to write enable high	20		25		ns

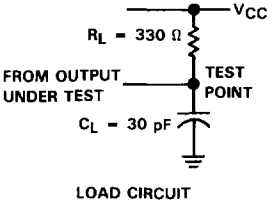
NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

PARAMETER MEASUREMENT INFORMATION



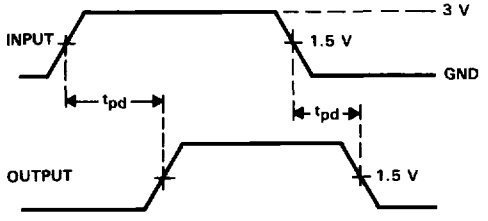
LOAD CIRCUIT

FIGURE 1. TOTEM-POLE OUTPUTS

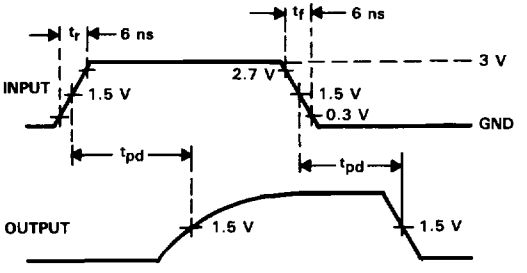


LOAD CIRCUIT

FIGURE 2. OPEN-DRAIN OUTPUTS



TOTEM-POLE OUTPUTS



OPEN-DRAIN OUTPUTS

FIGURE 3. TIMING REFERENCE LEVELS

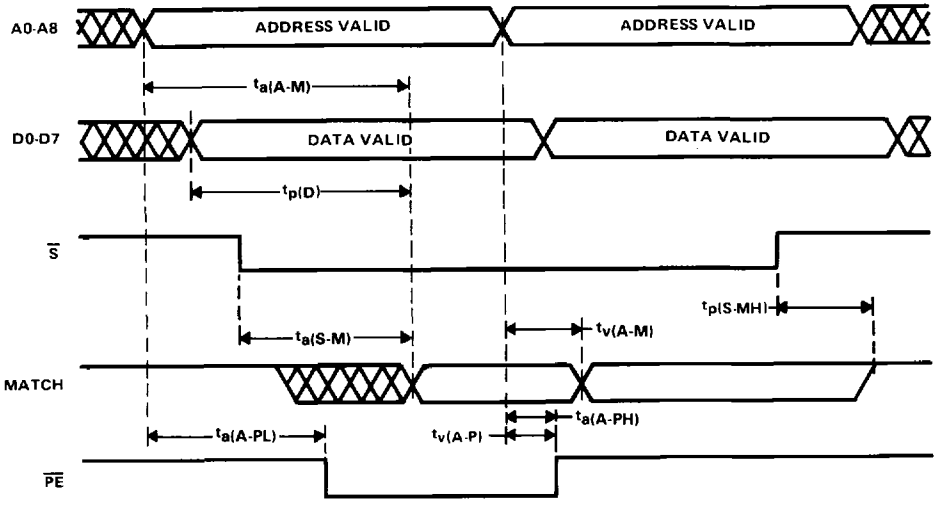


FIGURE 4. COMPARE CYCLE TIMING

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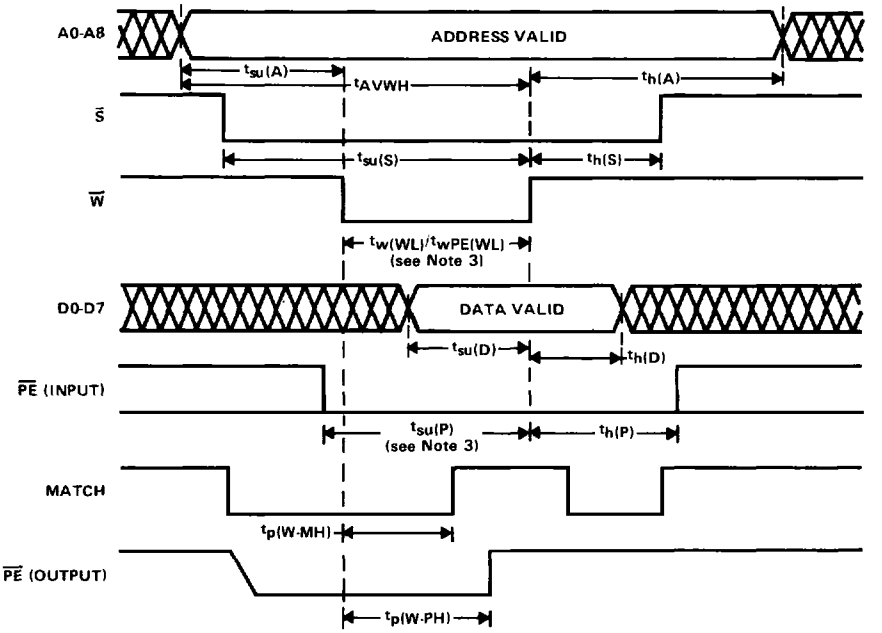
PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

FIGURE 5. WRITE CYCLE TIMING

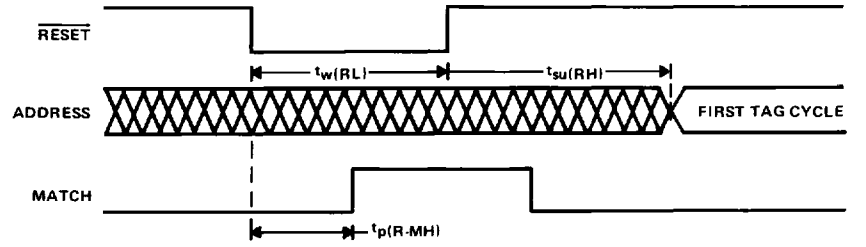


FIGURE 6. RESET CYCLE TIMING