ECL 10KH High-Speed Emitter Coupled Logic Family
MC10H166
5-Bit Magnitude Comparator

Features/Benefits

- **Propagation delay, Data-to-Output, 2.0 ns typical**
- **Power dissipation, 440 mW typical**
- **Noise margin 150 mV**
- **Voltage compensated**
- **ECL 10K-compatible**

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H166	J,N,NL	Com

Description

The MC10H166 is a member of Monolithic Memories' ECL 10KH family. This device is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard ECL 10K part with 100% improvement in propagation and no increase in power-supply current.

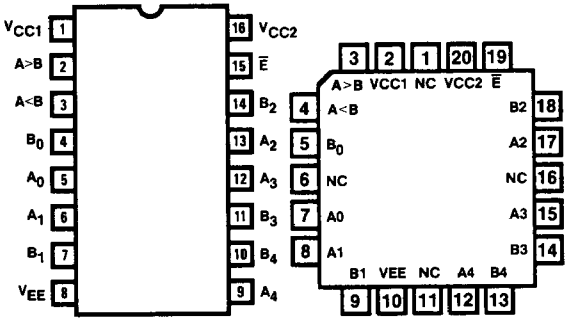
The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. The A = B function can be obtained by wire-ORing these outputs (a low level indicates A = B) or by wire-NORing the outputs (a high level indicates A = B). A high level on the enable function forces both outputs low.

Truth Table

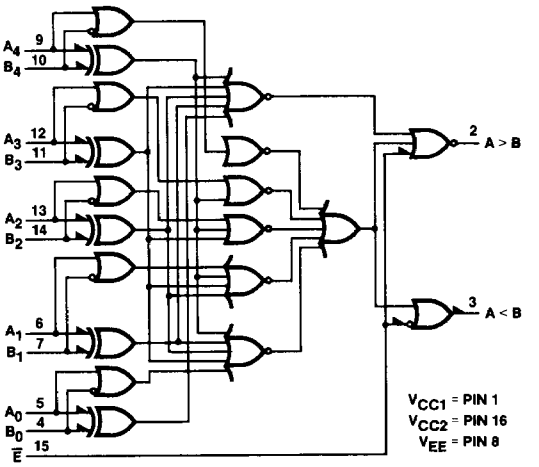
INPUTS			OUTPUTS	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

Pin Configurations

MC10H166
5-Bit Magnitude Comparator



Logic Diagram



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Monolithic Memories MMI

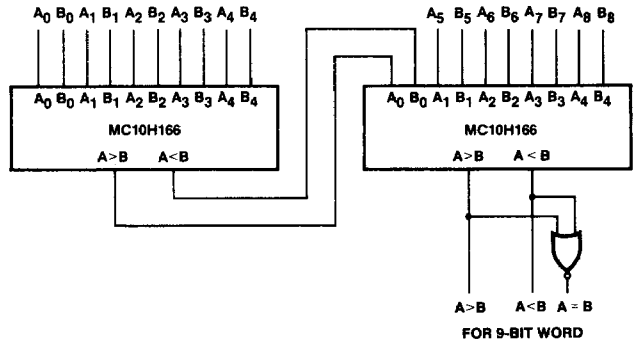

Figure 1. 9-Bit Magnitude Comparator

For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A>B and A<B outputs are fed to the A_0 and B_0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.

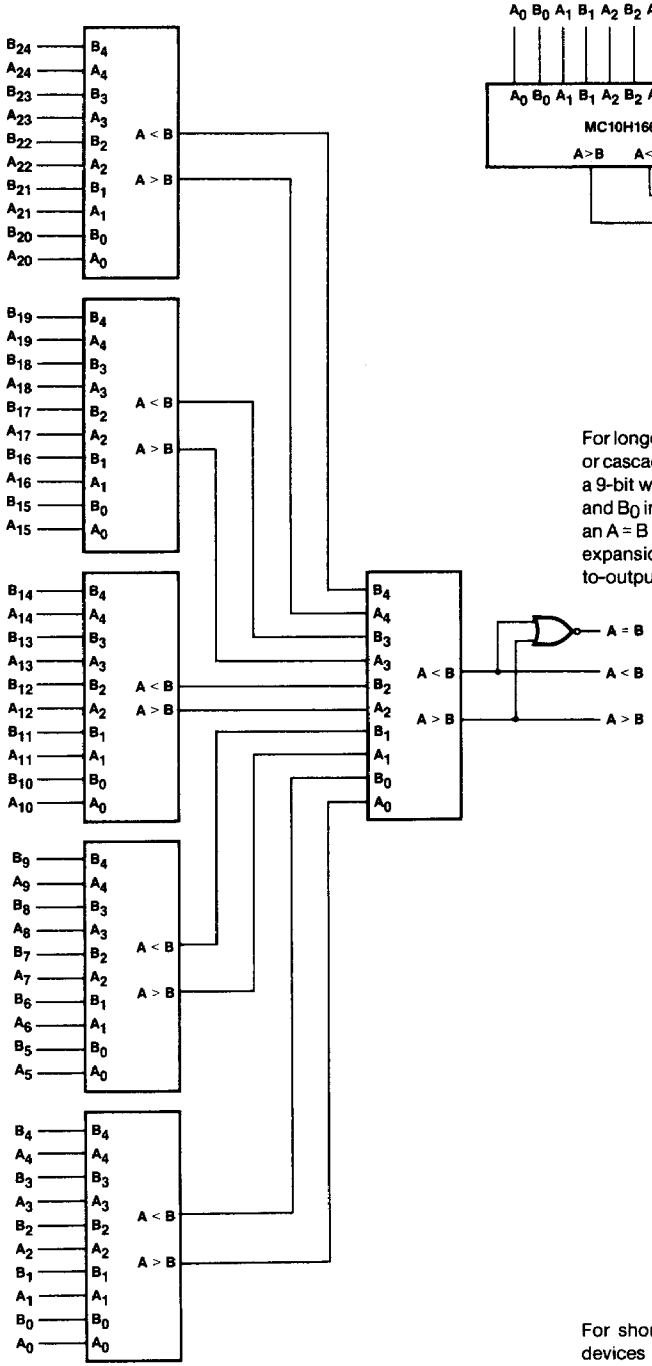

Figure 2. 25-Bit Magnitude Comparator

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

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