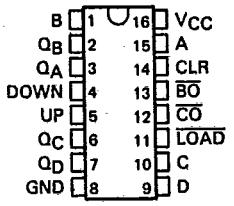
SN54HC192, SN54HC193
SN74HC192, SN74HC193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

D2684, DECEMBER 1982 – REVISED JUNE 1989

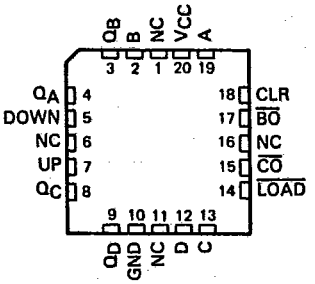
- **Look-Ahead Circuitry Enhances Cascaded Counters**
- **Fully Synchronous in Count Modes**
- **Parallel Asynchronous Load for Modulo-N Count Lengths**
- **Asynchronous Clear**
- **Package Options: Plastic and Ceramic DIPs, Plastic Small-Outline Packages, and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

SN54HC192, SN54HC193 . . . J PACKAGE
SN74HC192, SN74HC193 . . . D† OR N PACKAGE
(TOP VIEW)

T-45-23-09



SN54HC192, SN54HC193 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection
† Contact the factory for D availability.

description

The 'HC192 and 'HC193 are synchronous, reversible up/down counters. The 'HC192 is a 4-bit decade counter, and the 'HC193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero (all outputs low) and the count-down is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

The SN54HC192 and SN54HC193 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC192 and SN74HC193 are characterized for operation from −40°C to 85°C.

NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

SN54HC192, SN74HC192
SYNCHRONOUS 4-BIT UP/DOWN DECADE COUNTERS (DUAL CLOCK WITH CLEAR)

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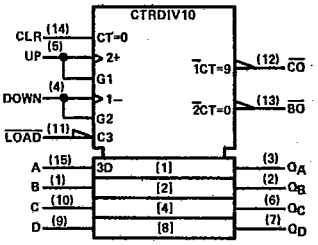
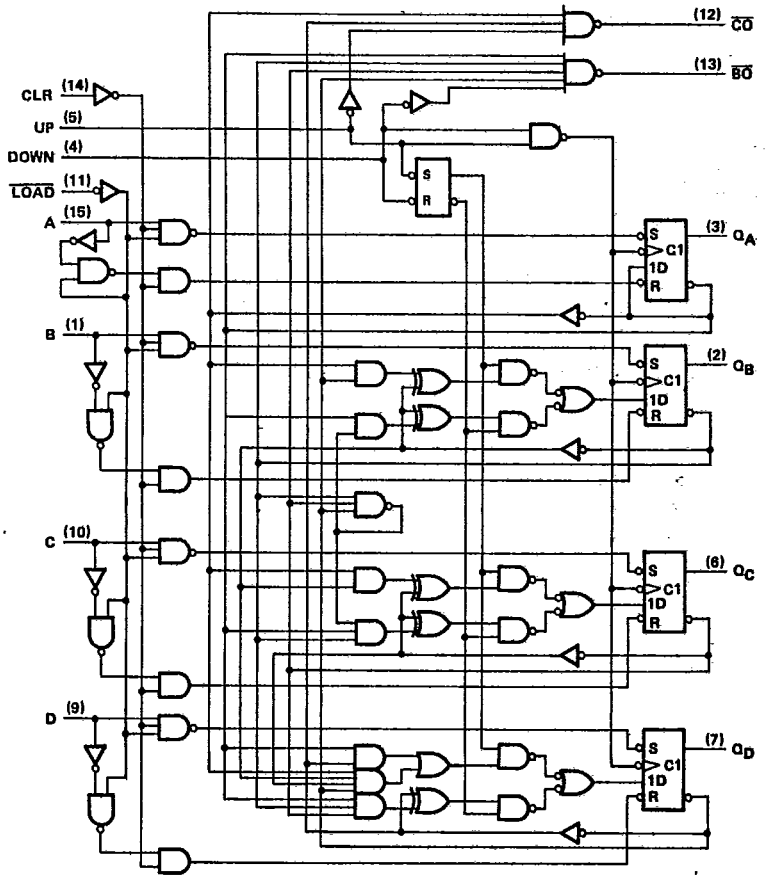
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

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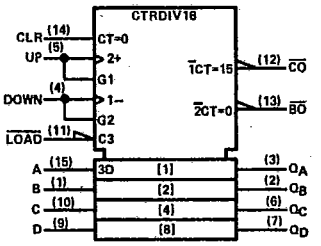
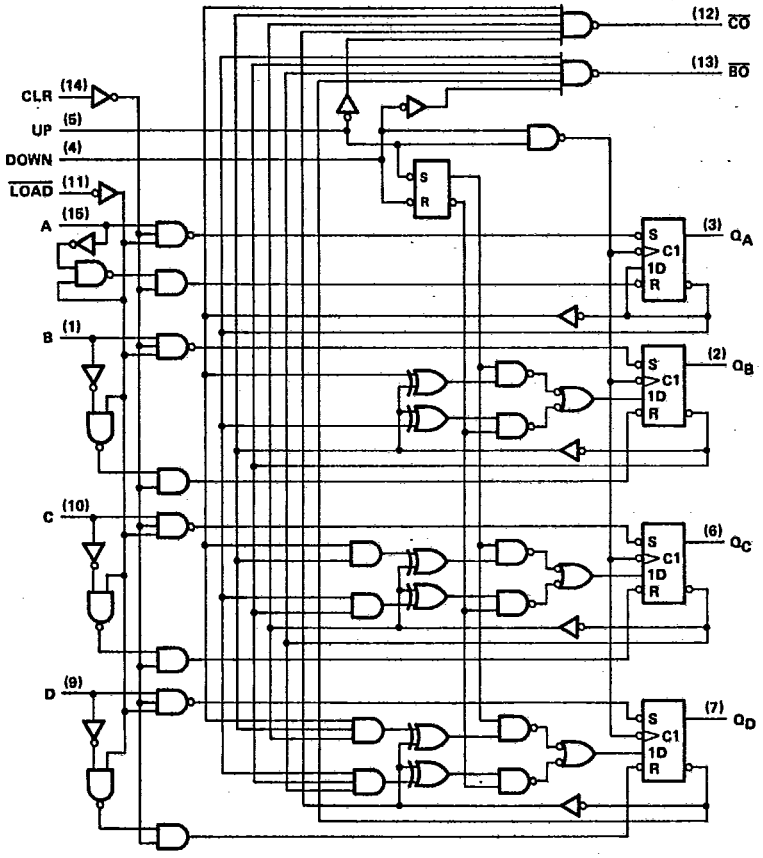
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

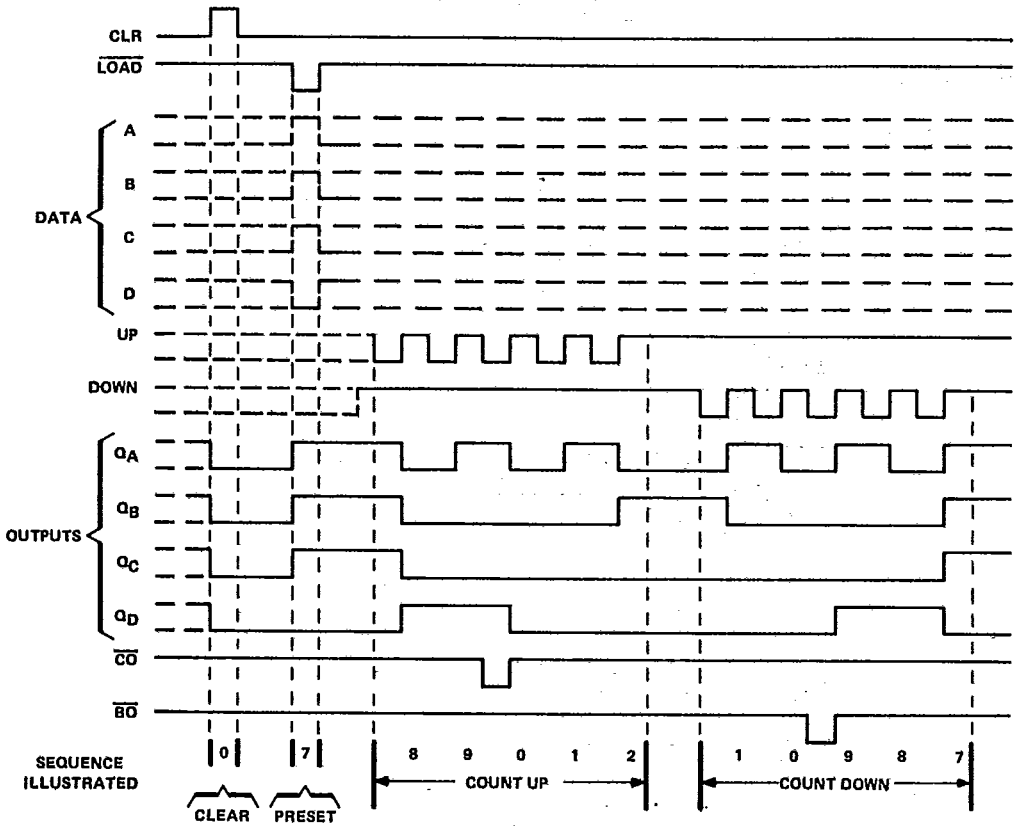


Pin numbers shown are for D, J, and N packages.

typical clear, load, and count sequence:

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to BCD seven
3. Count up to eight, nine, carry, zero, one, and two
4. Count down to one, zero, borrow, nine, eight, and seven.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

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typical clear, load, and count sequences

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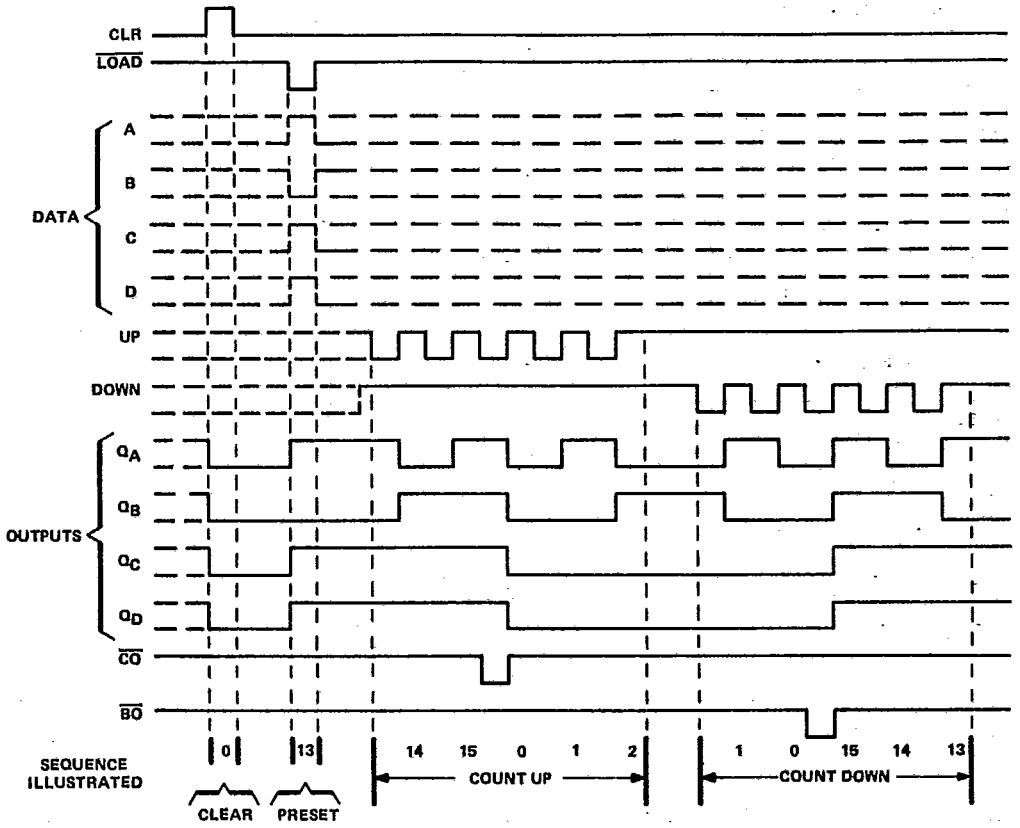
Illustrated below is the following sequence:

1. Clear outputs to zero
2. Load (preset) to binary thirteen
3. Count up to fourteen, fifteen, carry, zero, one, and two
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC} ..... −0.5 V to 7 V
Input clamp current, I_{IK}(V_I < 0 or V_I > V_{CC}) ..... ±20 mA
Output clamp current, I_{OK}(V_O < 0 or V_O > V_{CC}) ..... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) ..... ±25 mA
Continuous current through V_{CC} or GND pins ..... ±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package ..... 300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: D or N package ..... 260°C
Storage temperature range ..... −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54HC192 SN54HC193			SN74HC192 SN74HC193			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.3	0		0.3	V
		V_{CC} = 4.5 V	0		0.9	0		0.9	
		V_{CC} = 6 V	0		1.2	0		1.2	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HC192 SN54HC193		SN74HC192 SN74HC193		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	V_I = V_{IH} or V_{IL}, I_{OH} = −4 mA	4.5 V	3.98	4.30		3.7		3.84		
	V_I = V_{IH} or V_{IL}, I_{OH} = −5.2 mA	6 V	5.48	5.80		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	V_I = V_{IH} or V_{IL}, I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
	V_I = V_{IH} or V_{IL}, I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} or 0, I_O = 0	6 V			8		160		80	μA
C_i		2 to 6 V		3	10		10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC192 SN54HC193		SN74HC192 SN74HC193		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	4.2	0	2.8	0	3.3	MHz
			4.5 V	0	21	0	14	0	17	
			6 V	0	24	0	16	0	19	
t_w	Pulse duration	CLR high	2 V	120		180		150		ns
			4.5 V	24		36		30		
			6 V	21		31		26		
		$\overline{LOAD}$ low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
		UP or DOWN high or low	2 V	120		180		150		
			4.5 V	24		36		30		
			6 V	21		31		26		
t_{su}	Setup time	Data before $\overline{LOAD}$ inactive	2 V	110		165		140		ns
			4.5 V	22		33		28		
			6 V	19		28		24		
		CLR inactive before UP↑ or DOWN↑	2 V	110		165		140		
			4.5 V	22		33		28		
			6 V	19		28		24		
		$\overline{LOAD}$ inactive before UP↑ or DOWN↑	2 V	110		165		140		
			4.5 V	22		33		28		
			6 V	19		28		24		
t_h	Hold time	Data after $\overline{LOAD}$ inactive	2 V	5		5		5		ns
			4.5 V	5		5		5		
			6 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC192 SN54HC193		SN74HC192 SN74HC193		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	4.2	8		2.8		3.3		MHz
			4.5 V	21	55		14		17		
			6 V	24	60		16		19		
t_{pd}	UP	$\overline{CO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
t_{pd}	DOWN	$\overline{BO}$	2 V		75	165		250		205	ns
			4.5 V		24	33		50		41	
			6 V		20	28		43		35	
t_{pd}	UP or DOWN	Any Q	2 V		190	250		375		315	ns
			4.5 V		40	50		75		63	
			6 V		35	43		64		54	
t_{pd}	$\overline{LOAD}$	Any Q	2 V		190	260		390		325	ns
			4.5 V		40	52		78		65	
			6 V		35	44		66		55	
t_{PHL}	CLR	ANY Q	2 V		170	240		360		300	ns
			4.5 V		36	48		72		60	
			6 V		31	41		61		51	
t_t		Any	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

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