Chapter 7
Electrical Characteristics

Absolute Maximum Stress Ratings*

Table 7-1: Absolute Maximum Stress Ratings

Parameter	Symbol	Min	Max	Units
Storage temperature	T_{STG}	-55	150	°C
Supply voltage	V_{DD}	-0.5	7.0	V
Input voltage	V_{IN}	V_{SS}-0.5	V_{DD} + 0.5	V
Latch-up current	I_{LP}	± 200	-	mA**
Electrostatic discharge	ESD***	-	2K	V

** Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of this specification is not implied.*

*** -2V = Vpin > +8V*

**** SCSI pins only. Measured according to MIL-STD-883C, Method 3015.7*

Operating Conditions

Table 7-2: Operating Conditions

Parameter	Symbol	Min	Max	Units
Supply voltage	V_{DD}	4.75	5.25	V
Supply current (Static)	I_{DD}	-	1	mA
Supply current (Dynamic)	I_{DD}	-	75	mA
Operating temperature (free air)	T_A	0	70	°C
Thermal resistance (junction-ambient)	Θ_{JA}	50	65	°C/W
Power dissipation	P_{DD}	0	0.40	W

DC Characteristics

V_{DD} = 5V ± 5%, T_A = 0 to 70 °C, unless otherwise noted.

Table 7-3: SCSI Signals — SD(15-0)/*, SDP0/*, REQ/*, MSG/, I_O/, C_D/, ATN/, ACK/*, BSY/, SEL/, RST/, SDP1*

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Output low voltage	V_{OL}	V_{SS}	0.5	V	I_{OL} + 48 mA
Hysteresis	V_{HYS}	300	-	mV	-
Input leakage current	I_{IN}	-10	10	µA	-
Input leakage—SCSI RST/		-400	10	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

**TolerANT not enabled*

Table 7-4: Input Signals—BG/-HLDAI/, BOFF/, RESET/, CS/, BS(2-0)/, BCLK, SCLK, AUTO/, DIFFSENS

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Input leakage current	I_{IN}	-1.0	1.0	µA	-

Table 7-5: Input Signal—TSTIN/

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Input high leakage current	I_{IH}	-10	10	µA	$V_{IH} = V_{DD}$
Input low pull-up current	I_{IL}	-200	-50	µA	V_{IL} = 0 V

Table 7-6: Output Signals—SDIR(15-0), SDIRP0, BSYDIR, SELDIR, RSTDIR, TGS, IGS, SDIRP1

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -4 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 4 mA
Output high current	I_{OH}	-2.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	4.0	-	mA	V_{OL} = 0.4 V

Table 7-7: Output Signals—FETCH/, IRQ/, TSTOUT

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -8 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 8mA
Output high current	I_{OH}	-4.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	8.0	-	mA	V_{OL} = 0.4 V

Table 7-8: Output Signal—SLACK/-READYO/, MASTER/, MAC/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -16 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 16 mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V

Table 7-9: Tristate Output Signals—A(31-7), FC(2-0)-TM(2-0), SC(1-0), UPSO-TT0/, CBREQ/-TT1/, BR/-HOLD/

Parameter	Symbol	Min	Max	Units	Conditions
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -16 mA
Output low voltage	V_{OL}	V_{SS}	0.4	V	I_{OL} = 16mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V
Tristate leakage current	I_{OZ}	-10	10	µA	-

Table 7-10: Bidirectional Signals—A(6-0), D(31-0), DP(3-0), DS/-DLE/, AS/-TS/-ADS/, R_W/, BE0, BE1/, SIZ1-0, BHE/-BE2, SIZ1-BE3, BERR/-TEA/, HALT/-TIP/, BGACK-BB/, CBACK/-TBI/, STERM/-TA/-READYI/, GPIO (4-0)

Parameter	Symbol	Min	Max	Units	Conditions
Input high voltage	V_{IH}	2.0	V_{DD} + 0.5	V	-
Input low voltage	V_{IL}	V_{SS} - 0.5	0.8	V	-
Output high voltage	V_{OH}	2.4	V_{DD}	V	I_{OH} = -16 mA
Output low voltage	V_{OL}	V_{SS}	0.5	V	I_{OL} = 16 mA
Output high current	I_{OH}	-8.0	-	mA	$V_{OH} = V_{DD}$ - 0.5 V
Output low current	I_{OL}	16.0	-	mA	V_{OL} = 0.4 V
Input leakage current	I_{IN}	-10	10	µA	-
Tristate leakage current	I_{OZ}	-10	10	µA	-

Table 7-11: Capacitance

Parameter	Symbol	Min	Max	Units
Input capacitance of input pads	C_I	-	7	pF
Input capacitance of I/O pads	C_{IO}	-	10	pF

NCR TolerANT Technology

Table 7-12: NCR TolerANT Active Negation Technology Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.5	3.1	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.2	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	-	7.0	V	-
V_{IL}	Input low voltage	-0.5	-	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	-0.66	-0.74	-0.77	V	V_{DD} = 4.75; I_I = -20 mA
V_{TH}	Threshold, high to low	1.1	1.2	1.3	V	-
V_{TL}	Threshold, low to high	1.5	1.6	1.7	V	-
V_{TH}- V_{TL}	Hysteresis	300	350	400	mV	-
I_{OH}[1]	Output high current	2.5	15	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	150	200	mA	V_{OL} = 0.5 V
I_{OSH}[1]	Short-circuit output high current	-	-	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	-	-	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	-	0.05	10	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	-	-0.05	-10	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	-	20	-	MΩ	SCSI pins[3]

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

[1] *Active negation outputs only: Data, Parity, SREQ/, SACK/*

[2] *Single pin only; irreversible damage may occur if sustained for one second*

[3] *SCSI RESET pin has 10 kΩ pull-up resistor*

Table 7-12: NCR TolerANT Active Negation Technology Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_P	Capacitance per pin	-	8	10	pF	PQFP
t_R[1]	Rise time, 10% to 90%	9.7	15.0	18.5	ns	Figure 7-1
t_F	Fall time, 90% to 10%	5.2	8.1	14.7	ns	Figure 7-1
dV_H/dt	Slew rate, low to high	0.15	0.23	0.49	V/ns	Figure 7-1
dV_L/dt	Slew rate, high to low	0.19	0.37	0.67	V/ns	Figure 7-1
ESD	Electrostatic discharge	2	-	-	KV	MIL-STD-883C; 3015-7
	Latch-up	100	-	-	mA	-
	Filter delay	20	25	30	ns	Figure 7-2
	Extended filter delay	40	50	60	ns	Figure 7-2

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

[1] *Active negation outputs only: Data, Parity, SREQ/, SACK/*

[2] *Single pin only; irreversible damage may occur if sustained for one second*

[3] *SCSI RESET pin has 10 kΩ pull-up resistor*

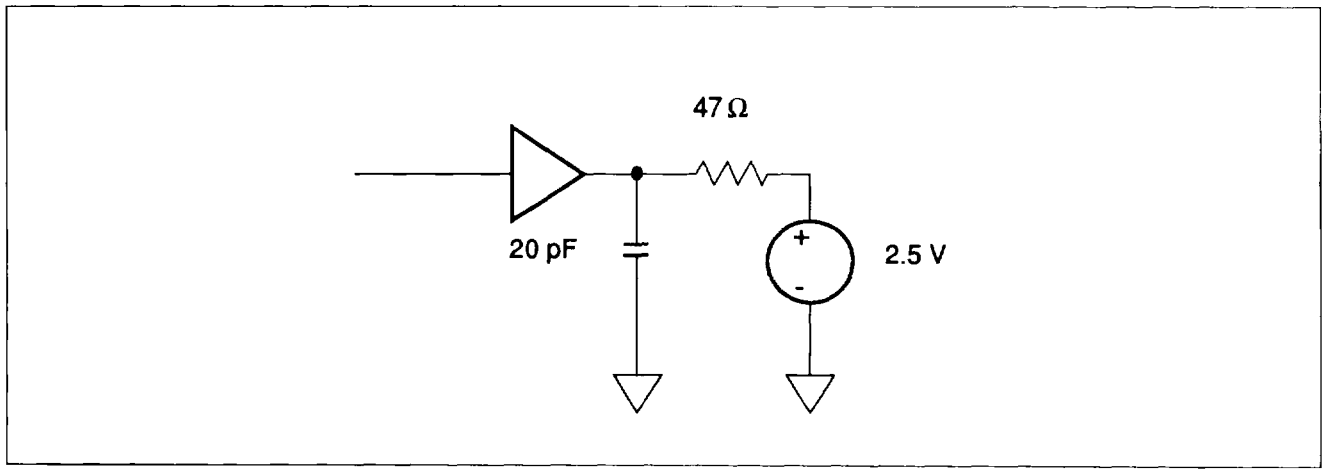


Figure 7-1: Rise and Fall Time Test Conditions

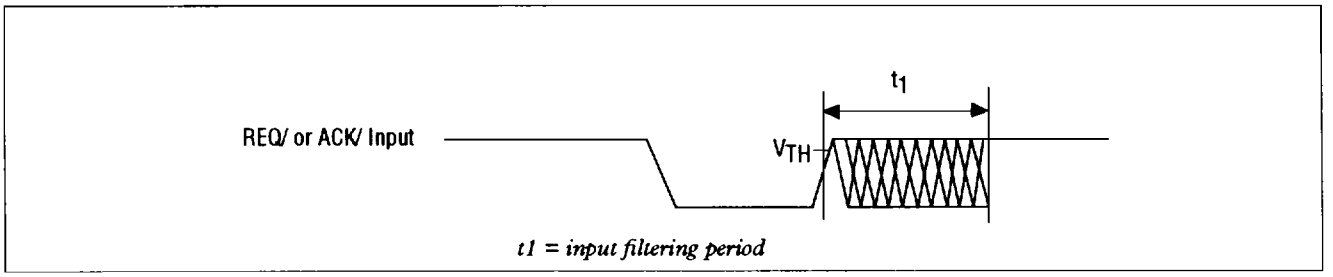


Figure 7-2: SCSI Input Filtering

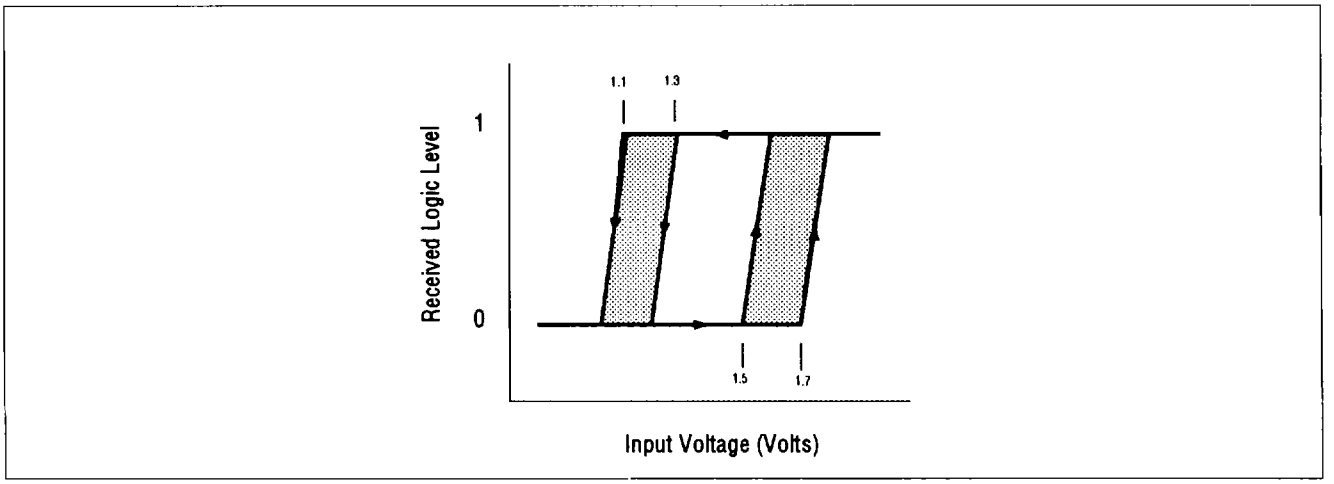


Figure 7-3: Hysteresis of SCSI Receiver

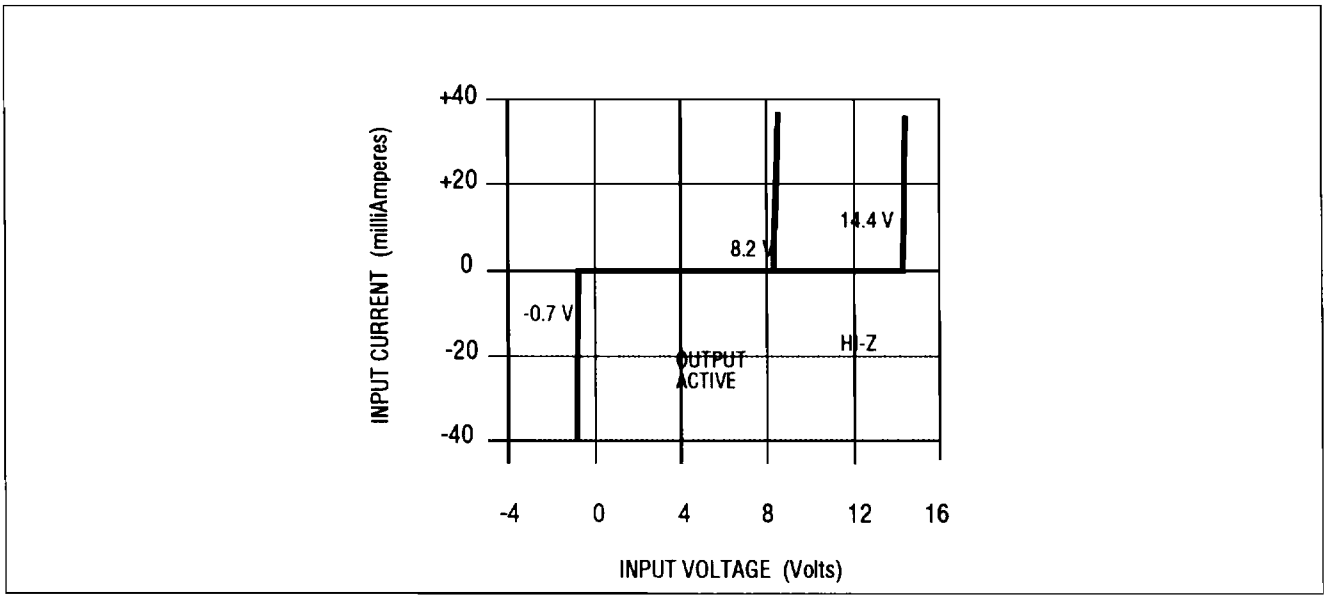
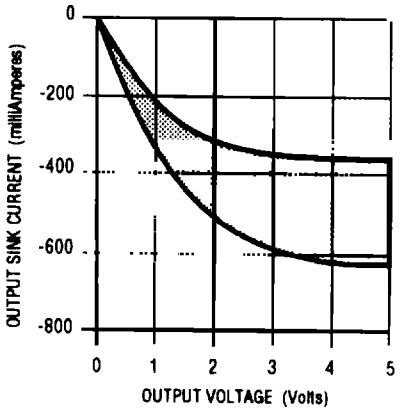
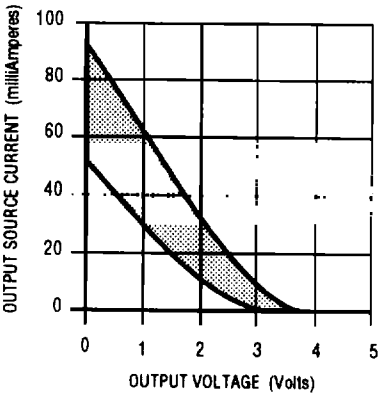


Figure 7-4: Input current as a Function of Input Voltage



Output source current as a function of output voltage (I_{OH})



Output sink current as a function of output voltage (I_{OL})

Figure 7-5: Output Current as a Function of Output Voltage

AC Characteristics

The AC characteristics in this section apply over the entire range of operating conditions (refer to Table 7-2, "Operating Conditions"). Chip timings are based on simulation at worst case voltage, temperature, and processing.

Clock Timings

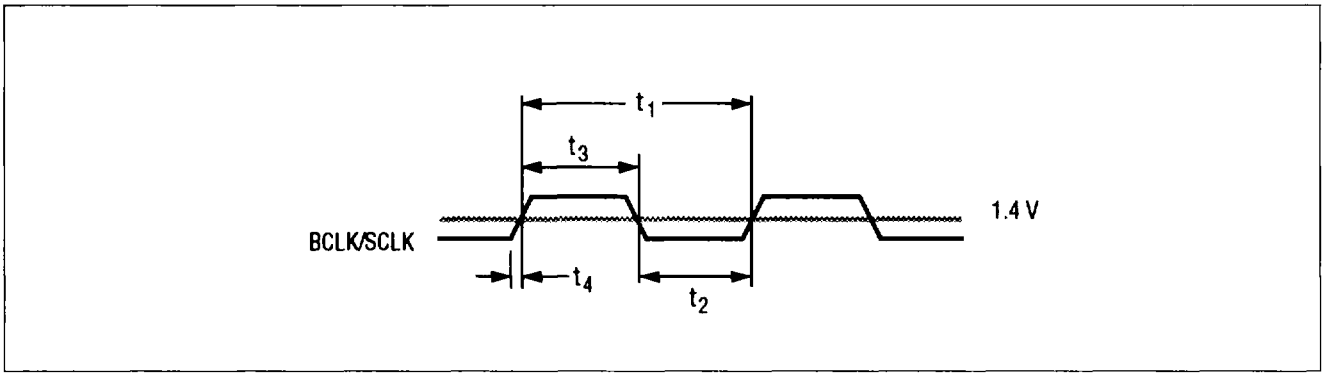


Figure 7-6: Clock Waveform

Table 7-13: Clock Timings

Parameter	Symbol	Min	Max	Units
Bus clock cycle time (BCLK)	t_1	40	DC	ns
Bus Mode 1		30	DC	ns
Bus Mode 2, 3, 4				
SCSI clock cycle time (SCLK)*		15	60	ns
BCLK low time	t_2	40% of BCLK cycle time	DC	ns
Bus Mode 1			DC	ns
Bus Modes 2, 3, 4				
SCLK low time*		40% of SCLK cycle time	33	ns
BCLK high time	t_3	40% of BCLK cycle time	-	ns
Bus Mode 1			-	ns
Bus Modes 2, 3, 4				
SCLK high time		40% of SCLK cycle time	33	ns
BCLK slew rate	t_4	1	-	V/ns
SCLK slew rate		1	-	V/ns

**This parameter must be met to insure SCSI timings are within specification*

Reset Input

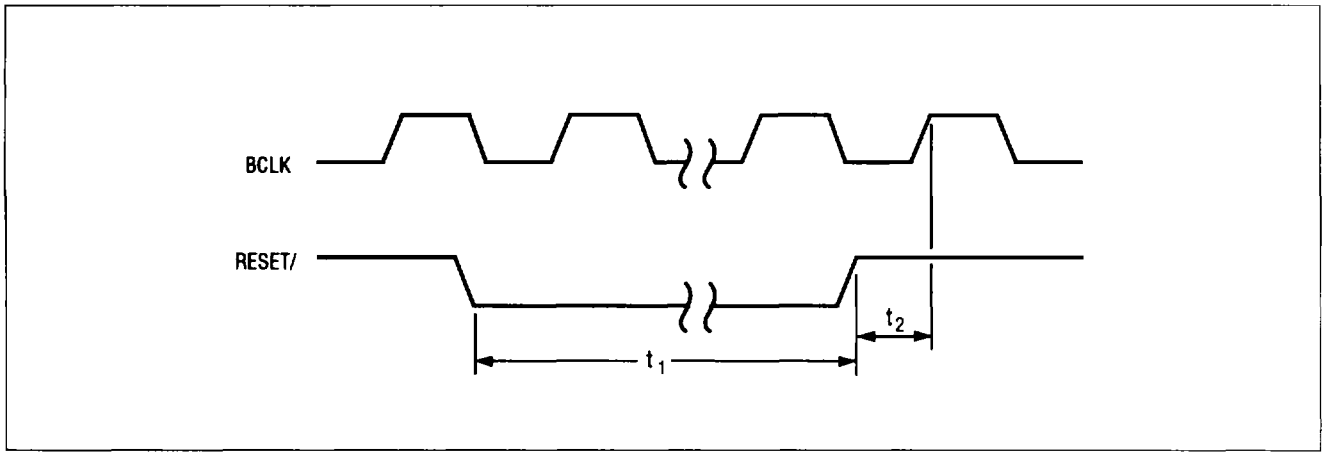


Figure 7-7: Reset Input Waveforms

Table 7-14: Reset Input Timings

Parameter	Symbol	Min	Max	Units
Reset pulse width	t_1	10	-	BCLK
Reset deasserted setup to BCLK high	t_2	10	-	ns

Interrupt Output

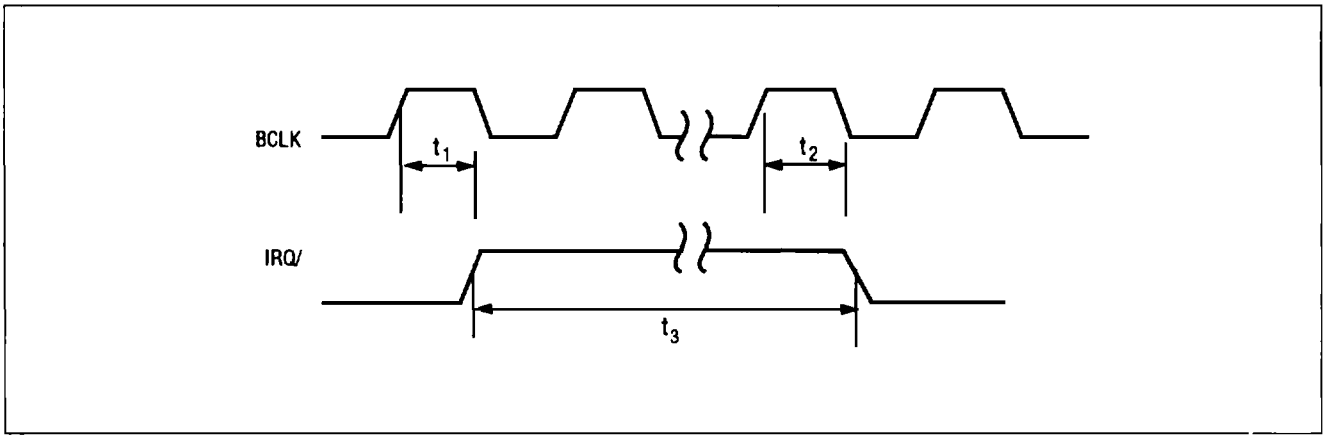


Figure 7-8: Interrupt Output Waveforms

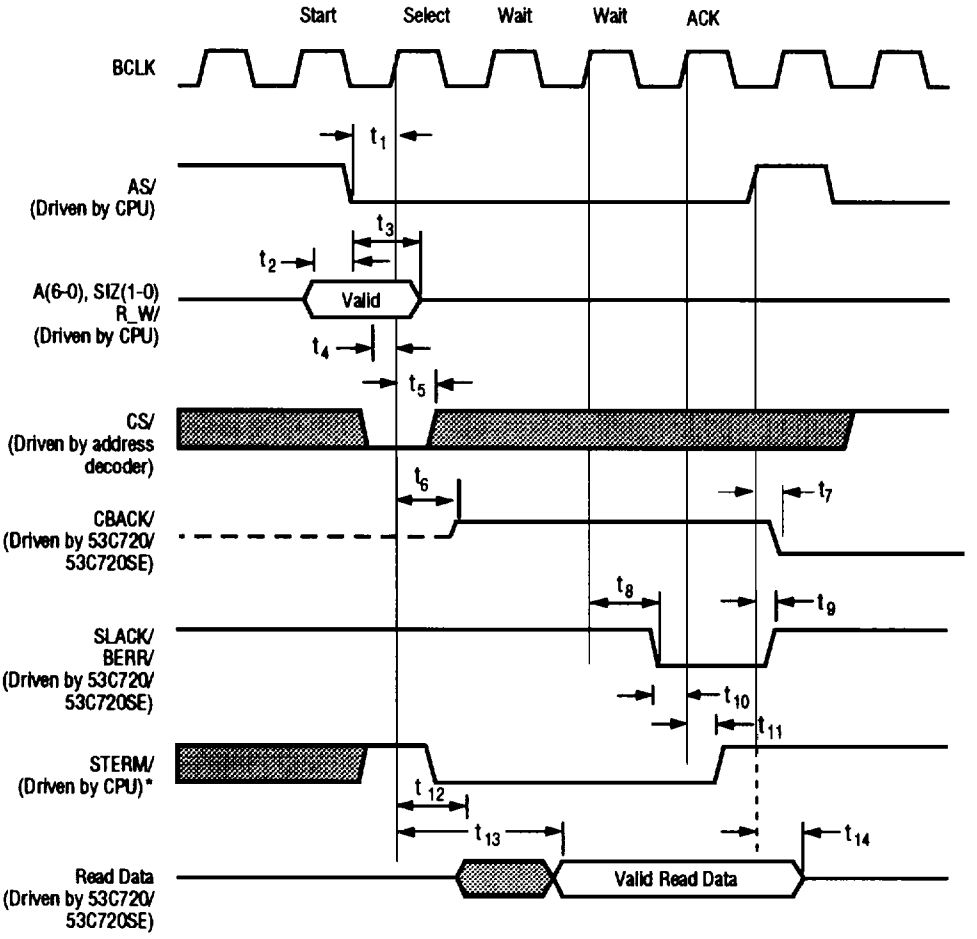
Table 7-15: Interrupt Output Timings

Parameter	Symbol	Min	Max	Units
BCLK high to IRQ/ high	t_1	-	20	ns
BCLK high to IRQ/ low	t_2	-	58	ns
IRQ/ deassertion time	t_3	3	-	BCLK

Bus Mode 1 Slave Cycle

Bus Mode 1 Slave Read Sequence

1. R_W/, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the NCR 53C720/53C720SE on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the NCR 53C720/53C720SE.
5. Two clock cycles of wait state are inserted (these wait states are required) and the data lines are asserted by the NCR 53C720/53C720SE.
6. Slave Acknowledge is asserted by the NCR 53C720/53C720SE if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the NCR 53C720/53C720SE and the data lines are tristated by the NCR 53C720/53C720SE.



**This signal may be driven the by NCR 53C720/53C720SE if the Enable ACK bit is set (DCNTL bit 5). See the explanation in Chapter 2 for use of this signal as an output.*

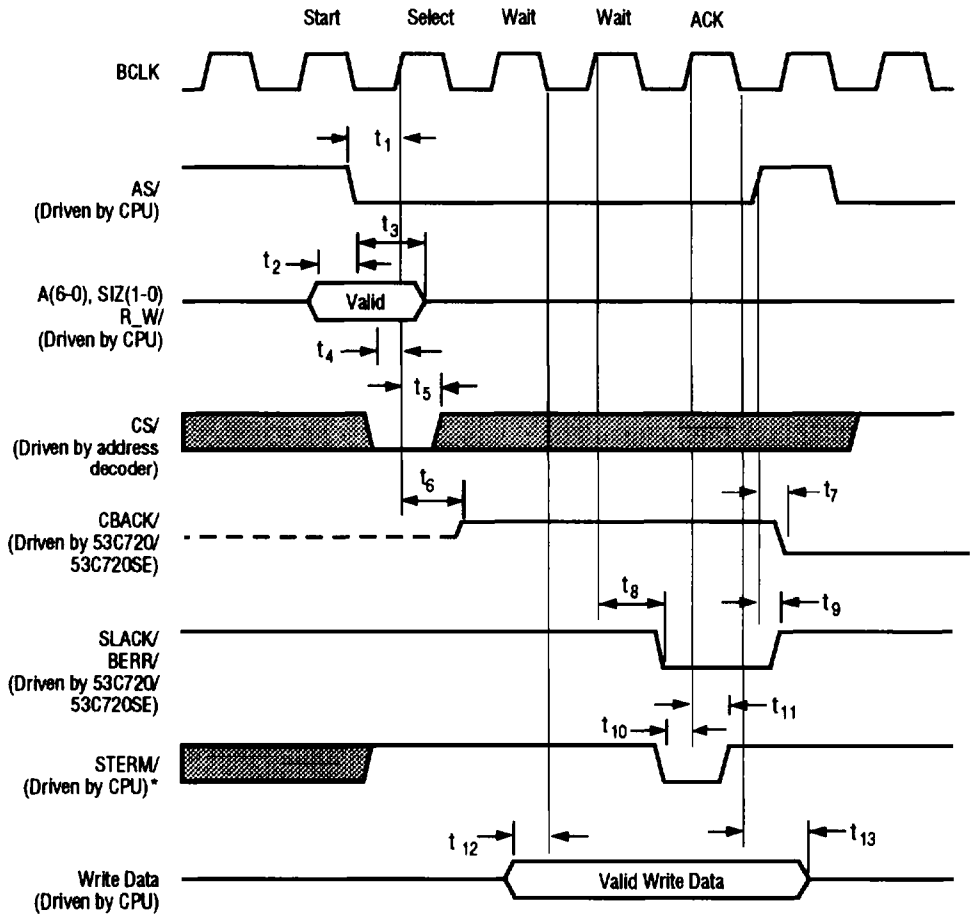
Figure 7-9: Bus Mode 1 Slave Read Waveforms

Table 7-16: Bus Mode 1 Slave Read Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R_W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	30	ns
AS/ high to CBACK/ low	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ setup to BCLK high	t_{10}	3	-	ns
STERM/ hold from BCLK high	t_{11}	7	-	ns
BCLK high to data bus driven	t_{12}	8	28	ns
BCLK high to read data valid	t_{13}	-	75	ns
AS/ high to data bus high-Z	t_{14}	7	32	ns

Bus Mode 1 Slave Write Sequence

1. R_W/, Address, and Size lines are asserted by the CPU.
2. Address Strobe is asserted by the CPU.
3. Chip Select is validated by the NCR 53C720/53C720SE on any following rising edge of BCLK.
4. Cache Burst Acknowledge is deasserted by the NCR 53C720/53C720SE
5. The data lines are asserted by the CPU.
6. Slave Acknowledge is asserted by the NCR 53C720/53C720SE if the cycle ends normally, or Bus Error is asserted if a bus error is detected.
7. STERM/ is sampled.
8. Address Strobe is deasserted by the CPU.
9. Slave Acknowledge or Bus Error is deasserted by the NCR 53C720/53C720SE.



**This signal may be driven by the NCR 53C720/53C720SE if the Enable ACK bit is set (DCNTL bit 5). See Chapter 2 for information on using this signal as an output.*

Note: data is latched on the rising edge of the ACK cycle when SLACK/ is asserted. Wait states cannot be inserted by using STERM/

Figure 7-10: Bus Mode 1 Slave Write Waveforms

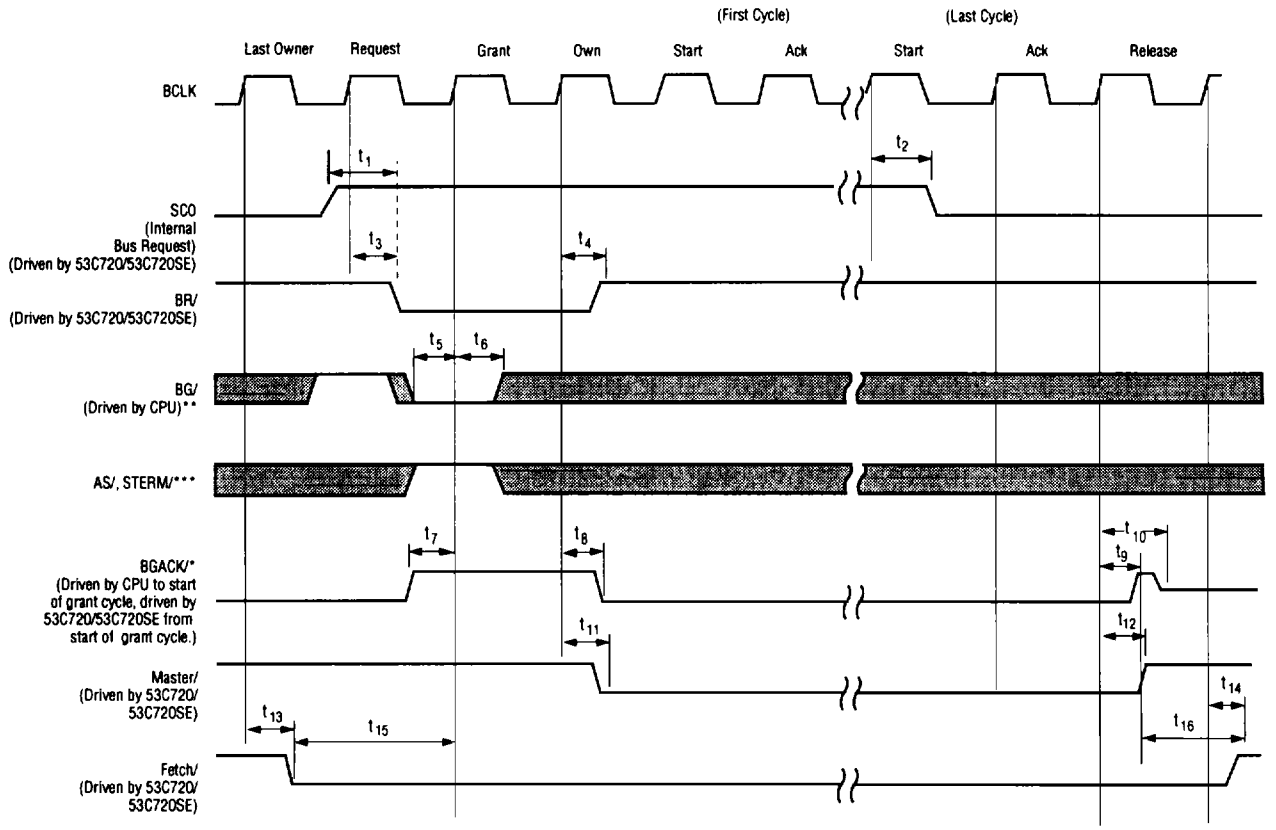
Table 7-17: Bus Mode 1 Slave Write Timings

Parameter	Symbol	Min	Max	Units
AS/ setup to CS/ clocked active	t_1	5	-	ns
A(6-0), SIZ(1-0), R_W/ setup to AS/	t_2	4	-	ns
A(6-0), SIZ(1-0), R/W/ hold from AS/	t_3	8	-	ns
CS/ setup to BCLK high after AS/	t_4	5	-	ns
CS/ hold from BCLK high after AS/	t_5	5	-	ns
BCLK high to CBACK/ high	t_6	5	30	ns
AS/ high to SLACK/ BERR/ high	t_7	3	17	ns
BCLK high to SLACK/, BERR/ low	t_8	-	22	ns
AS/ high to SLACK/, BERR/ high	t_9	-	22	ns
STERM/ (input) setup to BCLK high	t_{10}	3	-	ns
STERM/ (input) hold from BCLK high	t_{11}	7	-	ns
Write data setup to BCLK low	t_{12}	4	-	ns
Write data hold from BCLK low	t_{13}	6	-	ns

Bus Mode 1 Host Bus Arbitration

Bus Arbitration Sequence

1. The NCR 53C720/53C720SE internally determines bus mastership is required. If appropriate, FETCH/ is asserted.
2. Bus Request is asserted.
3. The NCR 53C720/53C720SE waits for Bus Grant and checks that Bus Grand Acknowledge is deasserted. Then the NCR 53C720/53C720SE asserts Bus Grant Acknowledge and Master, and deasserts Bus Request.



**If the Fast Arbitration bit is set (DCNTL bit 1), the NCR 53C720/53C720SE will drive the BGACK/ signal as soon as it receives a Bus Grant. One clock cycle of arbitration will be saved.*

****AS/ and STERM/ must be deasserted at this point for the NCR 53C720/53C720SE to take control of the bus.*

Note: the NCR 53C720/53C720SE will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access—it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may service.

Figure 7-11: Bus Mode 1 Host Bus Arbitration

Table 7-18: Bus Mode 1 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Unit
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BGACK/ setup to BCLK high (any rising edge after BR/)	t_7	5	-	ns
BCLK high to BGACK/ low	t_8	4	24	ns
BCLK high to BGACK/ high	t_9	3	19	ns
BCLK high to BGACK/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BGACK/ high to FETCH/ high**	t_{16}	1	2	BCLK

**When Snoop Mode bit 0 of CTEST3 is set to 1*

*** During a retry operation, FETCH/ will remain low until a successful completion of the op code fetch or a fatal bus error.*

Bus Mode 1 Fast Arbitration

Fast Arbitration Sequence*

1. The 53C720/53C720SE internally determines if bus mastership is required. FETCH/ is asserted during cycles in which the NCR 53C720/53C720SE is retrieving new SCRIPTS instructions.
2. Bus Request is asserted.
3. The NCR 53C720/53C720SE waits for Bus Grant. The NCR 53C720/53C720SE becomes bus master asynchronously on the leading edge of BG/. The NCR 53C720/53C720SE asynchronously asserts Bus Grant Acknowledge and Master, then deasserts Bus Request.
4. The NCR 53C720/53C720SE issues a start cycle on the next rising edge of BCLK.

** The Fast Arbitration bit must be set.*

Note: In fast arbitration mode, the NCR 53C720/53C720SE will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BGACK/

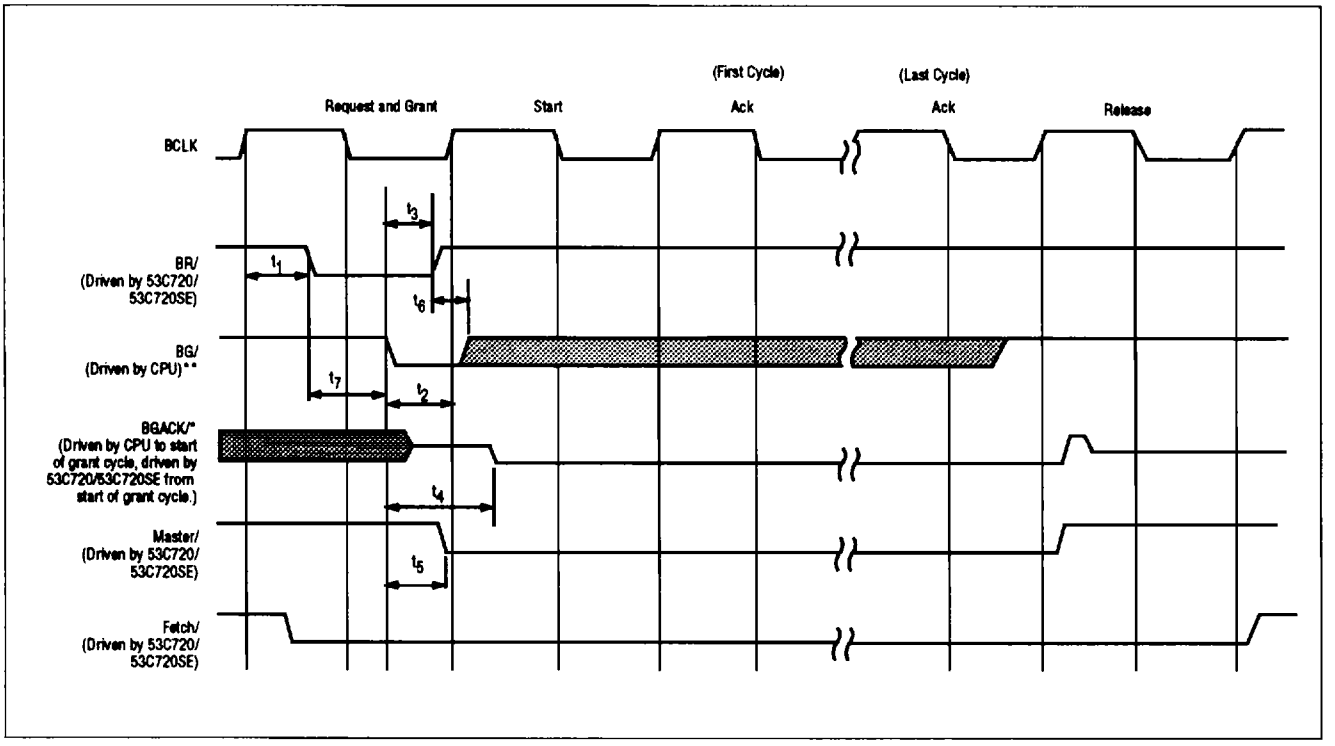


Figure 7-12: Bus Mode 1 Fast Arbitration

Table 7-19: Bus Mode 1 Fast Arbitration Timings

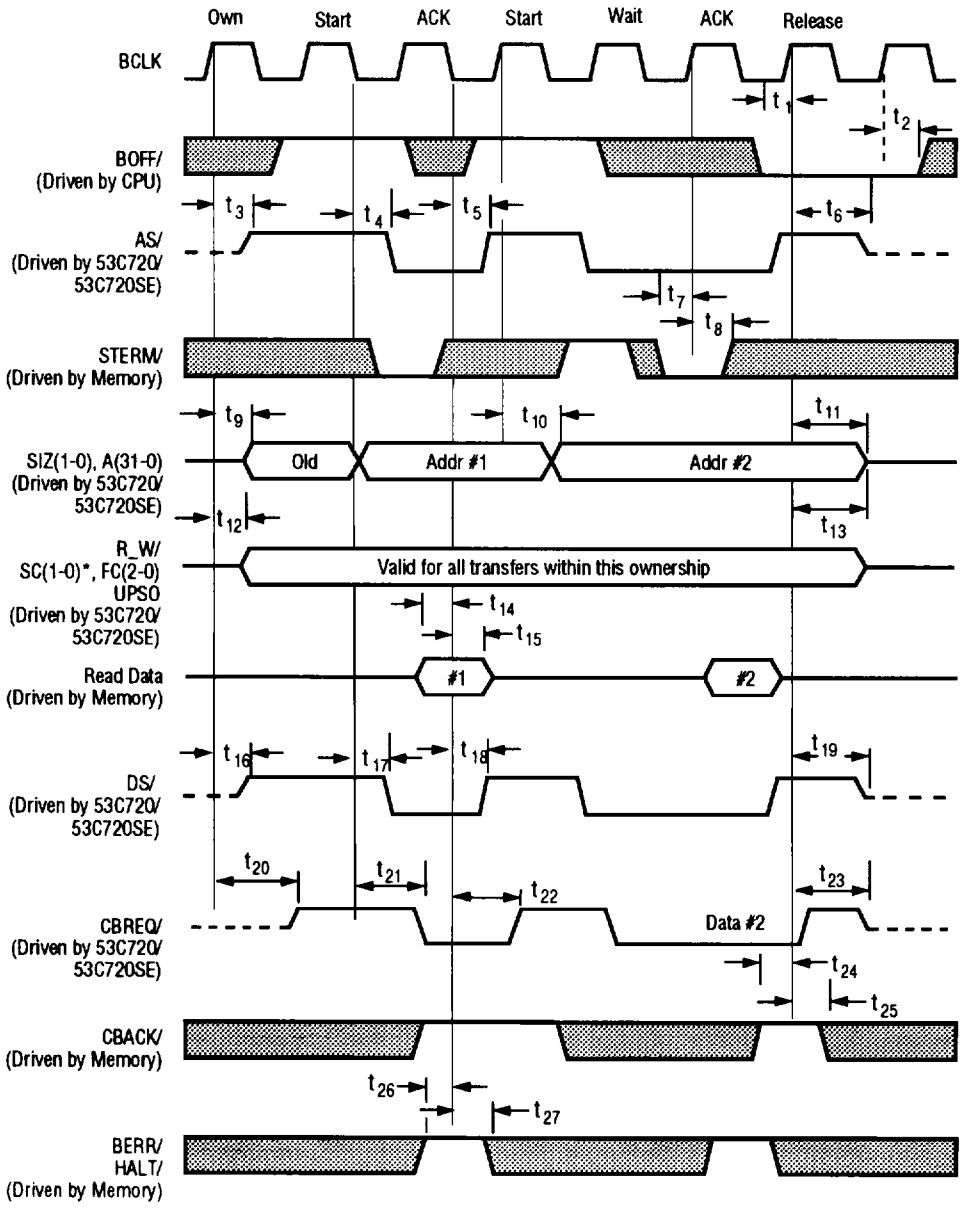
Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	12	-	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BGACK/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted*	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns

**BG/ may not be asserted prior to BR/*

Bus Mode 1 Master Cycle

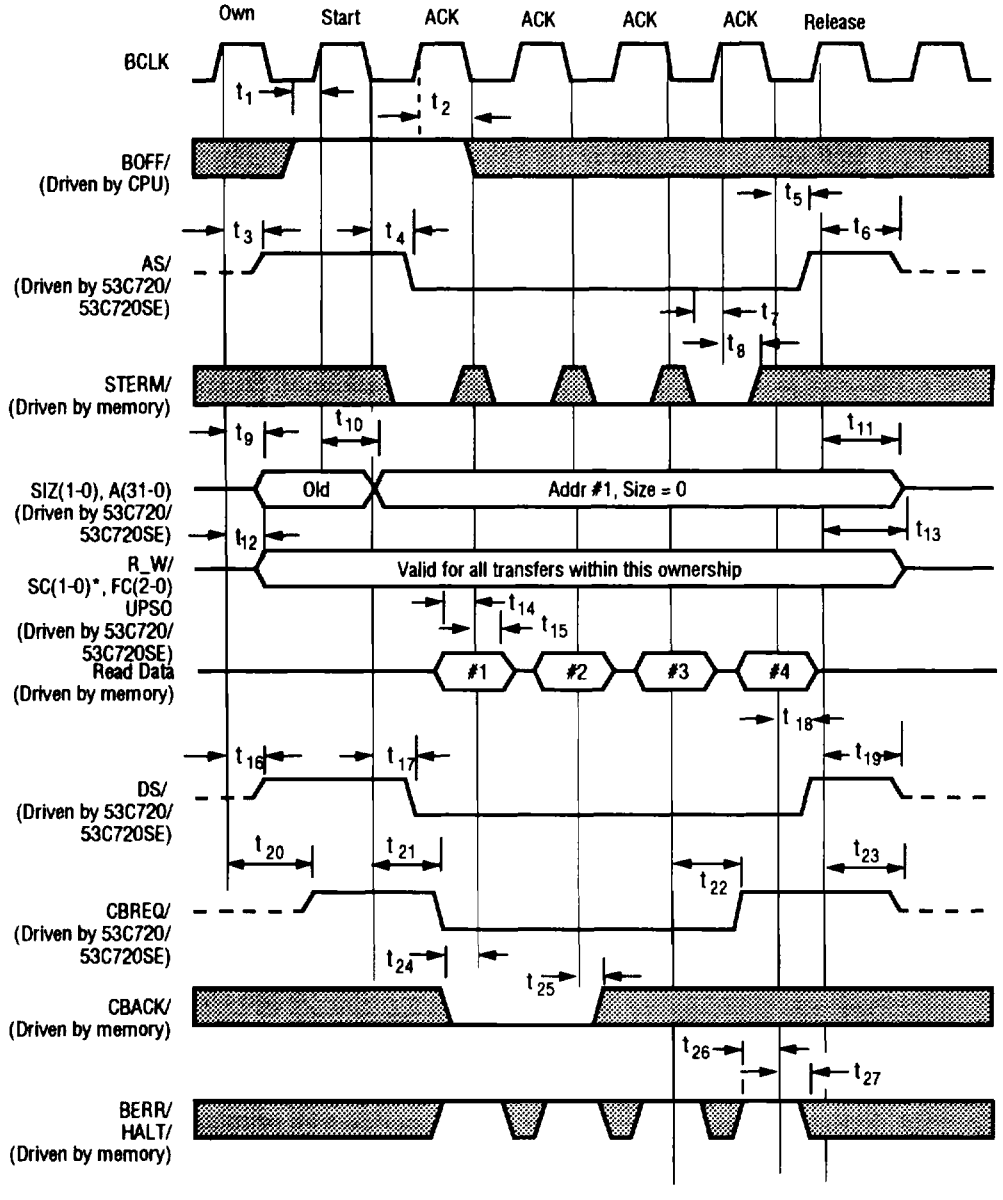
Bus Mode 1 Master Read Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the R_W/, Snoop Control, Function Control, and general purpose lines.
3. The NCR 53C720/53C720SE asserts the address and size lines.
4. The NCR 53C720/53C720SE asserts Address Strobe, Cache Burst Request (if bursting is enabled), and Data Strobe.
5. The NCR 53C720/53C720SE waits for Synchronous Termination, Valid Data, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting. Otherwise, proceed with non-cache transfers.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the NCR 53C720/53C720SE requires more cycles, then return to step 3.
6. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master and Bus Grant Acknowledge.
7. The NCR 53C720/53C720SE floats the control and address lines.



** SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0*

Figure 7-13: Bus Mode 1 Bus Master Read (Cache Line Burst Requested but not Acknowledged)



* *SC(1-0) timings apply only if Snoop Mode bit 0 of CTEST3 = 0*

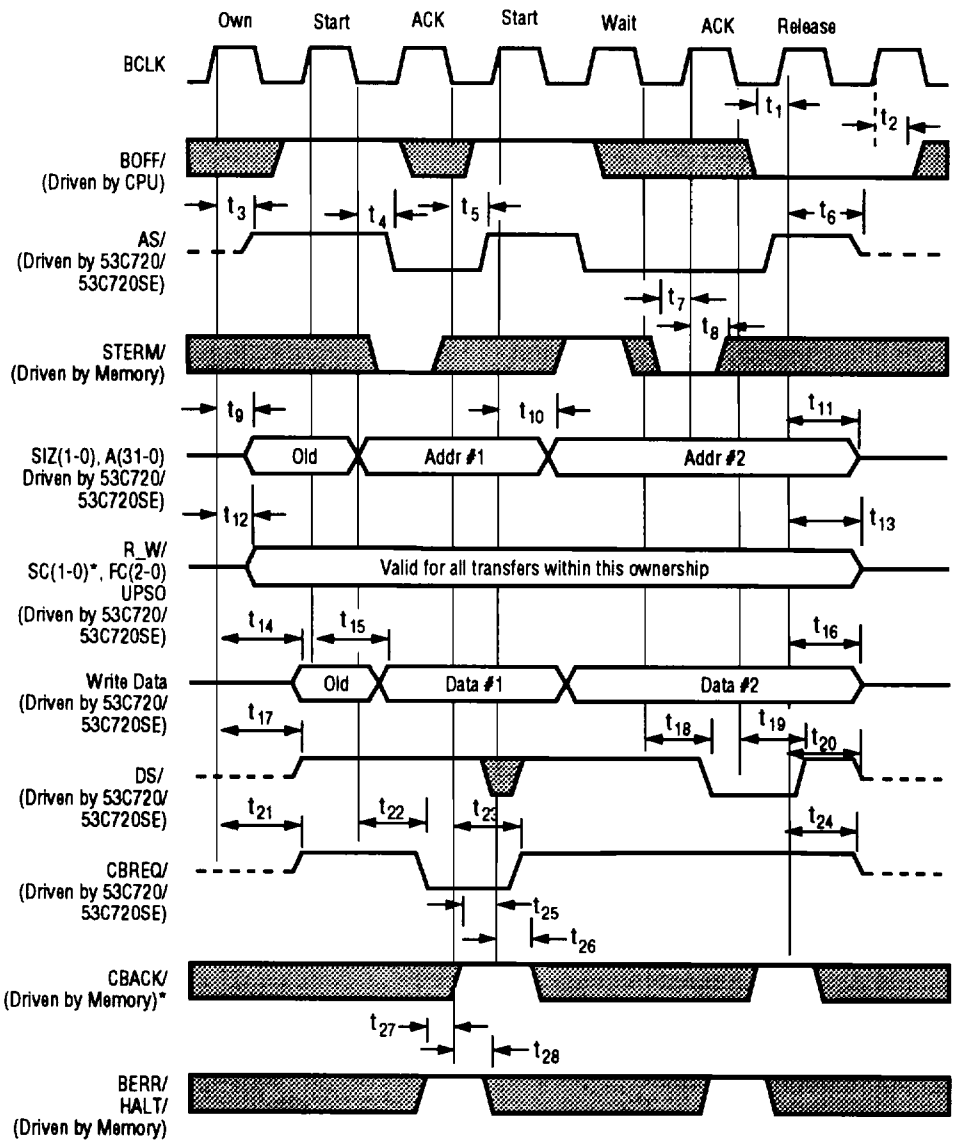
Figure 7-14: Bus Mode 1 Bus Master Read (Cache Line Burst)

Table 7-20: Bus Mode 1 Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ (1-0), A(31-0) valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
Read Data setup to BCLK low	t_{14}	4	-	ns
Read Data hold from BCLK low	t_{15}	6	-	ns
BCLK h igh to DS/ driven	t_{16}	5	28	ns
BCLK low to DS/ low	t_{17}	3	17	ns
BCLK low to DS/ high	t_{18}	3	17	ns
BCLK high to DS/ high-Z	t_{19}	7	32	ns
BCLK high to CBREQ/ driven	t_{20}	5	28	ns
BCLK high to CBREQ/ low	t_{21}	3	18	ns
BCLK low to CBREQ/ high	t_{22}	3	18	ns
BCLK high to CBREQ/ high-Z	t_{23}	7	32	ns
CBACK/ setup to BCLK low	t_{24}	8	-	ns
CBACK/ hold from BCLK low	t_{25}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{26}	6	-	ns
BERR/, HALT/ hold from BCLK low	t_{27}	4	-	ns

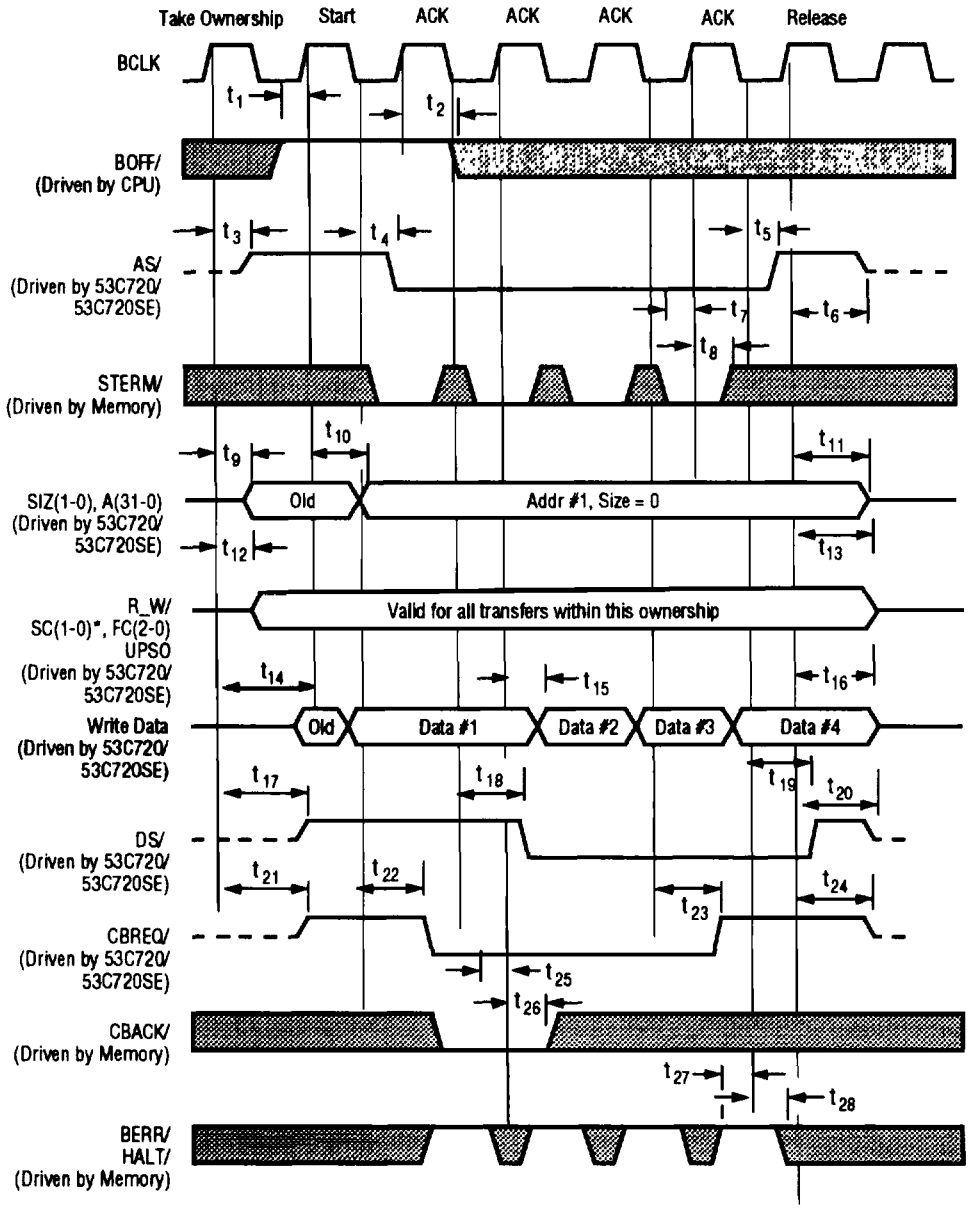
Bus Mode 1 Bus Master Write Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the R_W/, Snoop Control, Function Control, and General Purpose lines
3. The NCR 53C720/53C720SE asserts the Address, Size, and Data lines
4. The NCR 53C720/53C720SE asserts Address Strobe and Cache Burst Request.
5. The NCR 53C720/53C720SE asserts Data Strobe.
6. The NCR 53C720/53C720SE waits for Synchronous Termination, Cache Burst Acknowledge, Bus Error, and Halt.
   - If Cache Burst Acknowledge is asserted, attempt bursting.Otherwise, proceed with non-cache transfers.
   - If Bus Error and Halt are asserted, attempt a retry.
   - If Synchronous Termination is asserted without Bus Error or Halt, and the NCR 53C720/ 53C720SE requires more cycles, then return to step 3.
7. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master and Bus Grant Acknowledge
8. The NCR 53C720/53C720SE floats the Control, Address, and Data lines.



**SC(1-0 timings apply only if Snoop Mode bit o of CTEST3 = 0*

Figure 7-15: Bus Mode 1 Bus Master Write (Cache Line Burst Requested but not Acknowledged)



** SC(1-0) timings apply only if the Snoop Mode bit (CTEST3 bit 0) is clear.*

Figure 7-16: Bus Mode 1 Bus Master Write (Cache Line Burst)

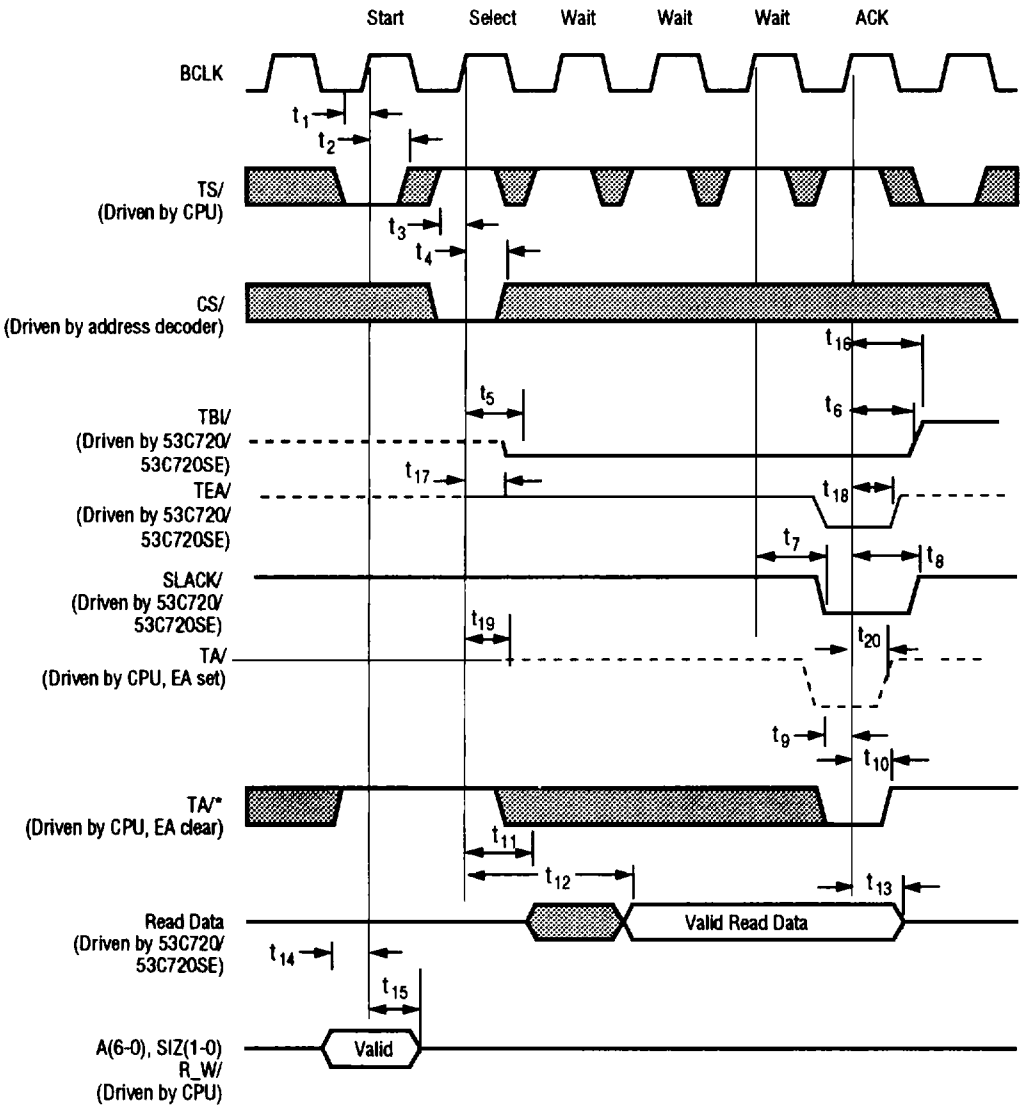
Table 7-21: Bus Mode 1 Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to AS/ driven	t_3	5	32	ns
BCLK low to AS/ low	t_4	3	15	ns
BCLK low to AS/ high	t_5	3	15	ns
BCLK high to AS/ high-Z	t_6	7	34	ns
STERM/ setup to BCLK high	t_7	3	-	ns
STERM/ hold from BCLK high	t_8	7	-	ns
BCLK high to SIZ(1-0), A(31-0) driven	t_9	5	28	ns
BCLK high to SIZ(1-0), A(31-0), valid	t_{10}	4	20	ns
BCLK high to SIZ(1-0), A(31-0) high-Z	t_{11}	7	34	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO driven and valid	t_{12}	5	28	ns
BCLK high to R_W/, SC(1-0), FC(2-0), UPSO high-Z	t_{13}	6	30	ns
BCLK high to Write Data driven	t_{14}	6	34	ns
BCLK high to Write Data valid	t_{15}	6	24	ns
BCLK high to Write Data high-Z	t_{16}	6	32	ns
BCLK high to DS/ driven	t_{17}	5	32	ns
BCLK low to DS/ low	t_{18}	3	17	ns
BCLK low to DS/ high	t_{19}	3	17	ns
BCLK high to DS/ high-Z	t_{20}	7	34	ns
BCLK high to CBREQ/ driven	t_{21}	5	30	ns
BCLK low to CBREQ/ low	t_{22}	3	18	ns
BCLK low to CBREQ/ high	t_{23}	3	18	ns
BCLK high to CBREQ/ high-Z	t_{24}	7	32	ns
CBACK/ setup to BCLK high	t_{25}	8	-	ns
CBACK/ hold from BCLK high	t_{26}	4	-	ns
BERR/, HALT/ setup to BCLK low	t_{27}	6	-	ns
BERR/, HALT hold from BCLK low	t_{28}	4	-	ns

Bus Mode 2 Slave Cycle

Bus Mode 2 Slave Read Sequence

1. R_W/, Address, Transfer Start, and the Size lines are asserted by the CPU.
2. Chip Select is validated by the NCR 53C720/53C720SE on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. Three clock cycles of wait state are inserted (these wait states are required) and the data lines are asserted.
6. Slave Acknowledge is asserted by the NCR 53C720/53C720SE, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Slave Acknowledge or Transfer Error Acknowledge is deasserted.
9. The NCR 53C720/53C720SE waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if no errors are detected.
10. The data lines are tristated by the NCR 53C720/53C720SE.



** This signal may be driven by the NCR 53C720/53C720SE if the Enable Ack bit is set (DCNTL bit 5). See the explanation in Chapter 2 of this manual for use of this signal as an output.*

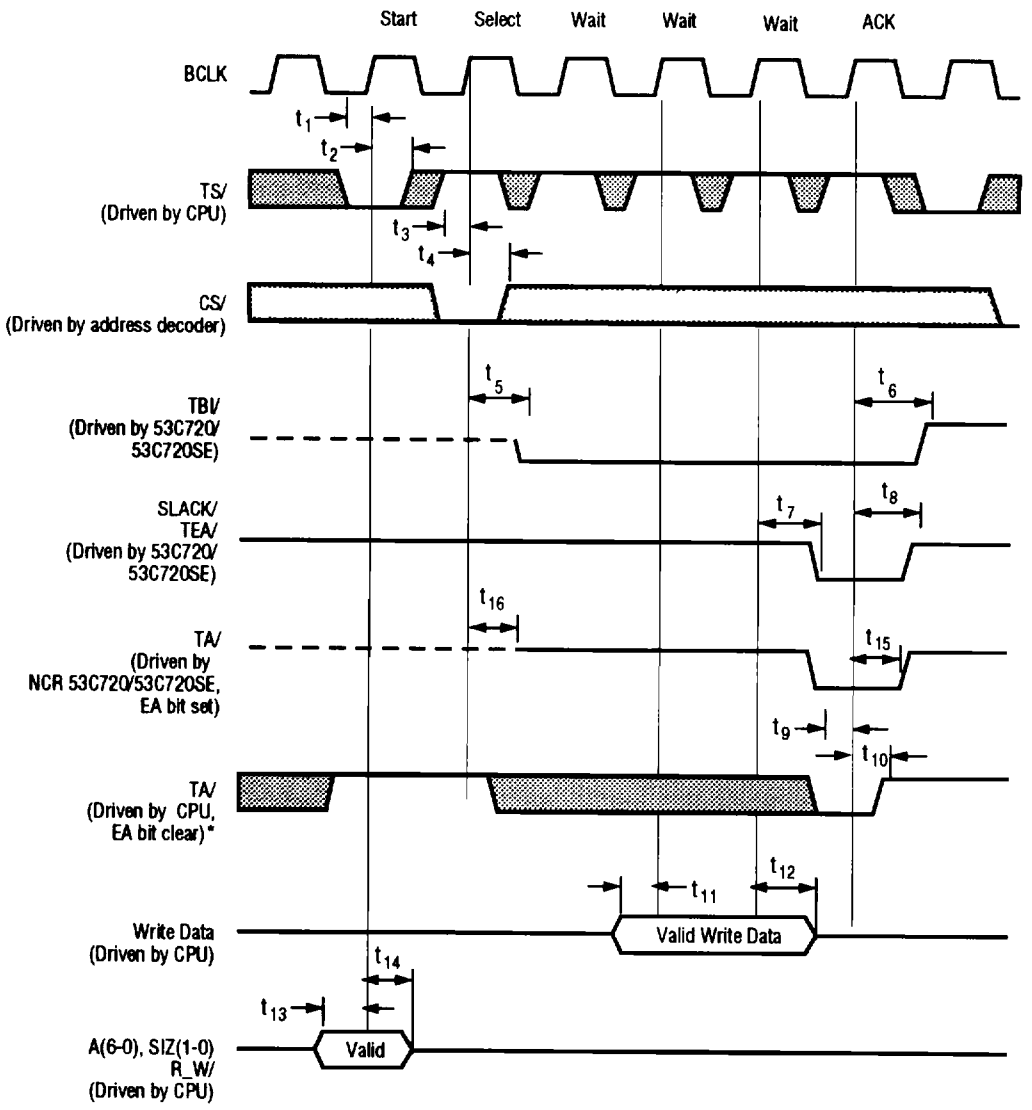
Figure 7-17: Bus Mode 2 Slave Read

Table 7-22: Bus Mode 2 Slave Read Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	34	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{14}	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{15}	12	-	ns
BCLK high to TBI/ high-Z	t_{16}	8	32	ns
BCLK high to TEA/ driven	t_{17}	8	27	ns
BCLK high to TEA/ high-Z	t_{18}	9	34	ns
BCLK high to TA/ driven	t_{19}	8	27	ns
BCLK high to TA/ high-Z	t_{20}	9	33	ns

Bus Mode 2 Slave Write Sequence

1. R_W/, Address, Transfer Start, and the Size Lines are asserted by the CPU.
2. Chip Select is validated by the NCR 53C720/53C720SE on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Transfer Start is deasserted by the CPU.
5. The data lines are asserted by the CPU.
6. Three clock cycles of wait state are inserted (these wait states are required).
7. Slave Acknowledge is asserted by the NCR 53C720/53C720SE, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. The NCR 53C720/53C720SE waits for Transfer Acknowledge to be asserted and then ends the slave cycle, if there are no errors.
10. Slave Acknowledge or Transfer Error Acknowledge is deasserted.



**This signal may be driven by the NCR 53C720/53C720SE if the Enable Ack bit (DCNTL bit 5) is set. See the explanation in Chapter 2 of this manual for use of this signal as an output.*

Figure 7-18: Bus Mode 2 Slave Write

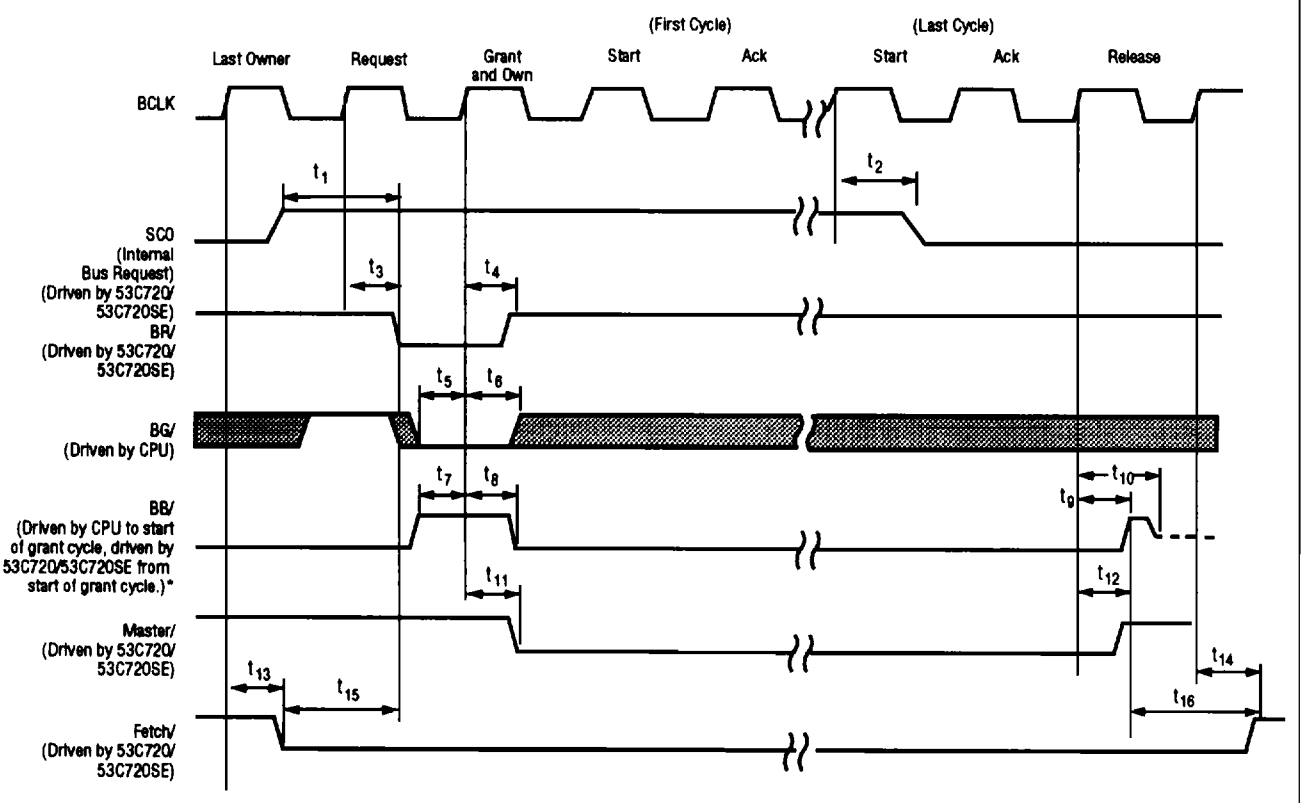
Table 7-23: Bus Mode 2 Slave Write Timings

Parameter	Symbol	Min	Max	Units
TS/ setup to BCLK high	t_1	4	-	ns
TS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after TS/	t_3	5	-	ns
CS/ hold from BCLK high after TS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to SLACK/, TEA/ low	t_7	5	20	ns
BCLK high to SLACK/, TEA/ high	t_8	4	20	ns
TA/ setup to BCLK high during or after SLACK/, TEA/	t_9	9	-	ns
TA/ hold from BCLK high during or after SLACK/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	6	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(6-0), SIZ(1-0), R_W/ setup to BCLK high	t_{13}	4	-	ns
A(6-0), SIZ(1-0), R_W/ hold from BCLK high	t_{14}	12	-	ns
BCLK high to TA/ driven	t_{15}	8	27	ns
BCLK high to TA/ high-Z	t_{16}	9	33	ns

Bus Mode 2 Host Bus Arbitration

Bus Mode 2 Bus Arbitration Sequence

1. The NCR 53C720/53C720SE internally determines bus mastership is required. FETCH/ is asserted during cycles in which the NCR 53C720/53C720SE is retrieving new SCRIPTS instructions.
2. Bus Request is asserted.
3. The NCR 53C720/53C720SE waits for BG/ and checks that BB/ is deasserted. Then the NCR 53C720/53C720SE asserts BB/ and MASTER/, and deasserts BR/.



** If the Fast Arbitration bit is set (DCNTL bit 1), the NCR 53C720/53C720SE will drive the Bus Grant Acknowledge signal as soon as it receives a bus grant. One clock cycle of arbitration will be saved.*

Note: the NCR 53C720/53C720SE will periodically assert the BR/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the BG/ signal to complete the normal bus arbitration handshake. The chip no longer wants host bus access—it deasserts the BR/, MASTER/, and all control lines after one BCLK, and does not assert TS/, the signal that indicates a valid bus cycle is starting. The chip will next generate an interrupt which the system may service.

Figure 7-19: Bus Mode 2 Host Bus Arbitration

Table 7-24: Bus Mode 2 Host Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to BR/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to BR/ low	t_3	4	20	ns
BCLK high to BR/ high	t_4	5	25	ns
BG/ setup to BCLK high (any rising edge after BR/)	t_5	4	-	ns
BG/ hold from BCLK high (any rising edge after BR/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after BR/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
FETCH/ low to BR/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

**When Snoop Mode bit of CTEST3 is set to 1.*

***During a retry operation, FETCH/ will remain low until successful completion of an op code fetch or a fatal bus error.*

Bus Mode 2 Fast Arbitration

Bus Mode 2 Fast Arbitration Sequence*

1. The NCR 53C720/53C720SE determines bus mastership is required. FETCH/ is asserted during cycles in which the NCR 53C720/53C720SE is retrieving new SCRIPTS instructions.
2. Bus request is asserted
3. The NCR 53C720/53C720SE waits for Bus Grant. The NCR 53C720/53C720SE becomes bus master asynchronously on the leading edge of BG/. Then the NCR 53C720/53C720SE asynchronously asserts Bus Busy and Master, and deasserts Bus Request.
4. The NCR 53C720/53C720SE issues a start cycle on the next rising edge of BCLK.

** Fast Arbitration bit must be set.*

Note: in fast arbitration mode, the NCR 53C720/53C720SE will take bus ownership on the assertion of BG/ regardless of the state of BR/ or BB/.

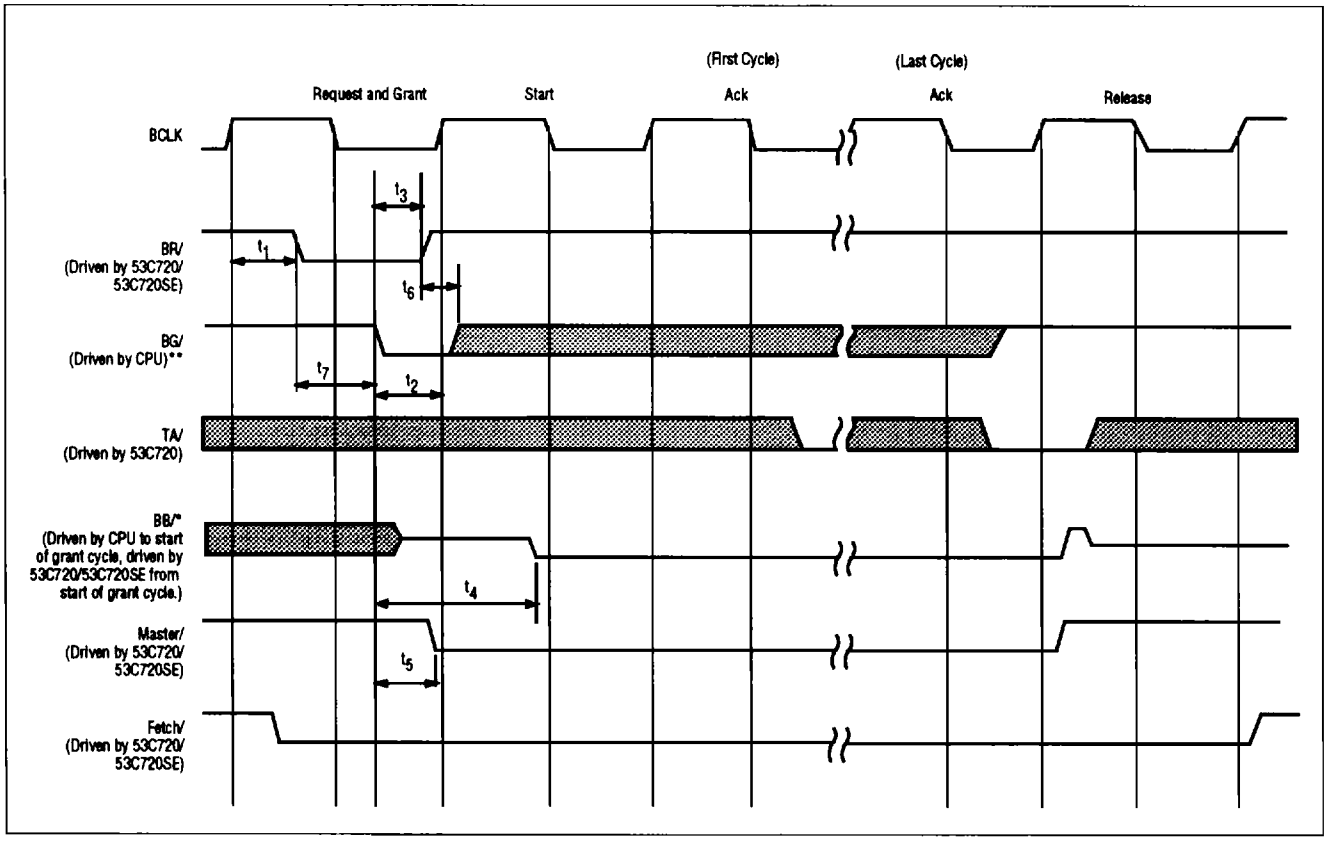


Figure 7-20: Bus Mode 2 Fast Arbitration

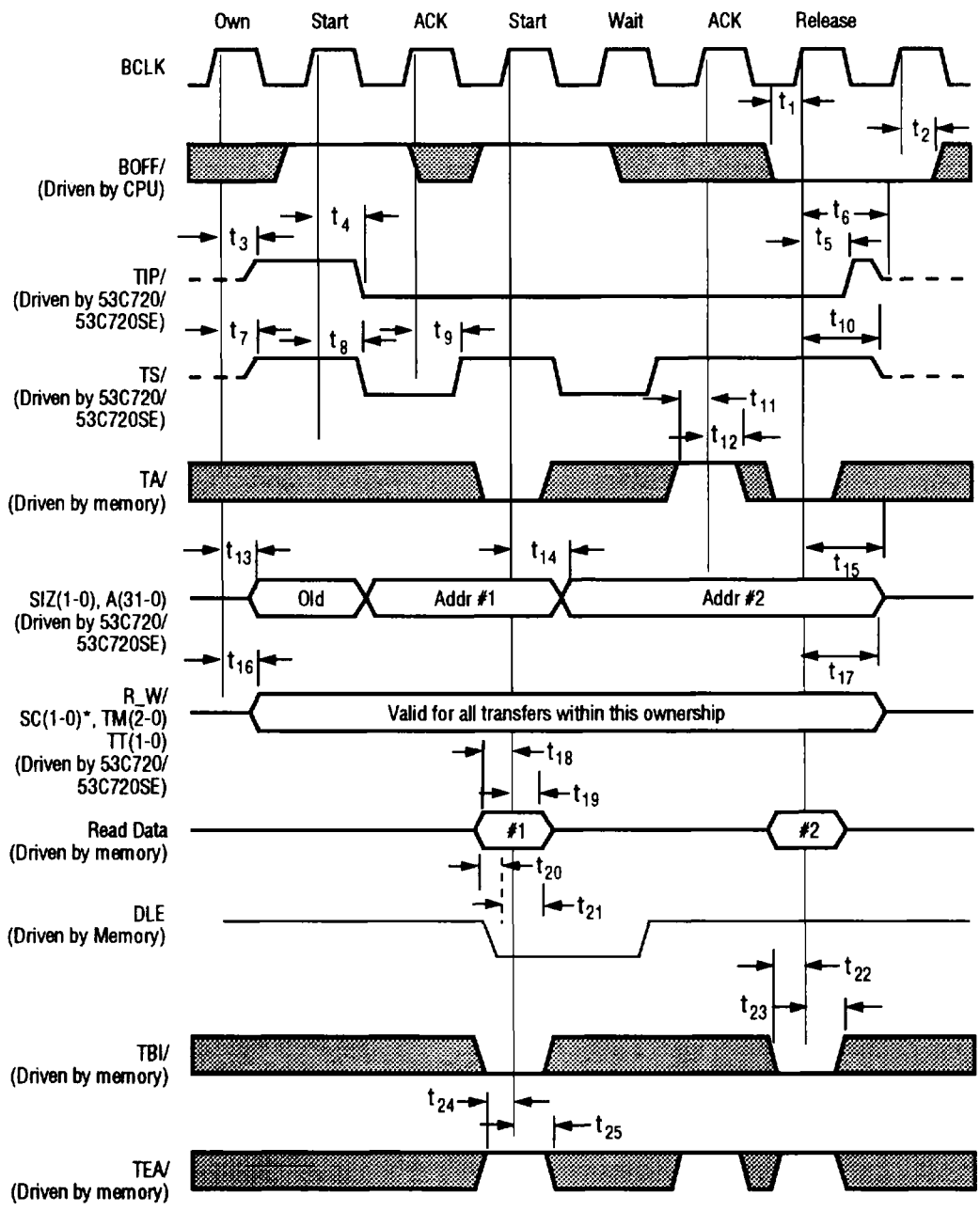
Table 7-25: Bus Mode 2 Fast Arbitration Timings

Parameter	Symbol	Min	Max	Units
BCLK high to BR/ asserted	t_1	-	20	ns
BG/ setup to BCLK high	t_2	12	-	ns
BG/ asserted to BR/ deasserted	t_3	-	22	ns
BG/ asserted to BB/ asserted	t_4	-	20	ns
BG/ asserted to MASTER/ asserted	t_5	-	16	ns
BG/ hold after BR/ deasserted	t_6	0	-	ns
BR/ asserted to BG/ asserted	t_7	0	-	ns

Bus Mode 2 Master Cycle

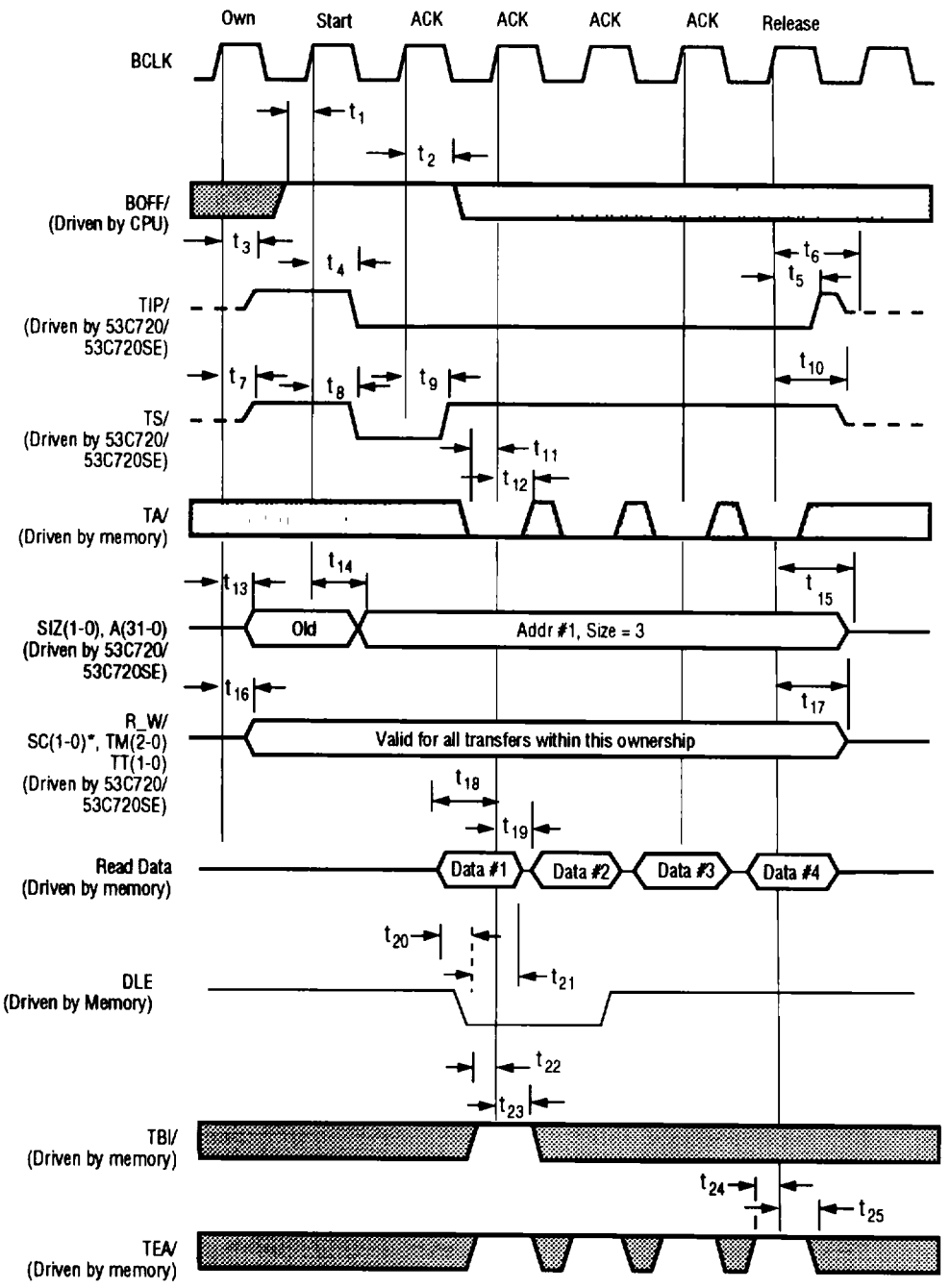
Bus Mode 2 Master Read Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the R_W/, Snoop Control, Transfer Modifier, and Transfer Type lines.
3.
   a. The NCR 53C720/53C720SE asserts Transfer in Progress.
   b. The NCR 53C720/53C720SE asserts Transfer Start, Address, and Size lines.
4. The NCR 53C720/53C720SE deasserts Transfer Start.
5. The NCR 53C720/53C720SE waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the NCR 53C720/53C720SE requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master, Bus Busy, and Transfer in Progress.
7. The NCR 53C720/53C720SE floats the Control and Address lines.



SC(1-0) timings apply only if Snoop Mode bit, bit 0 of CTEST3 = 0

Figure 7-21: Bus Mode 2 Bus Master Read (Cache Line Burst Requested but not Acknowledged)



SC(1-0) timings apply only if the Snoop Mode bit (bit 0 of CTEST0) is zero.

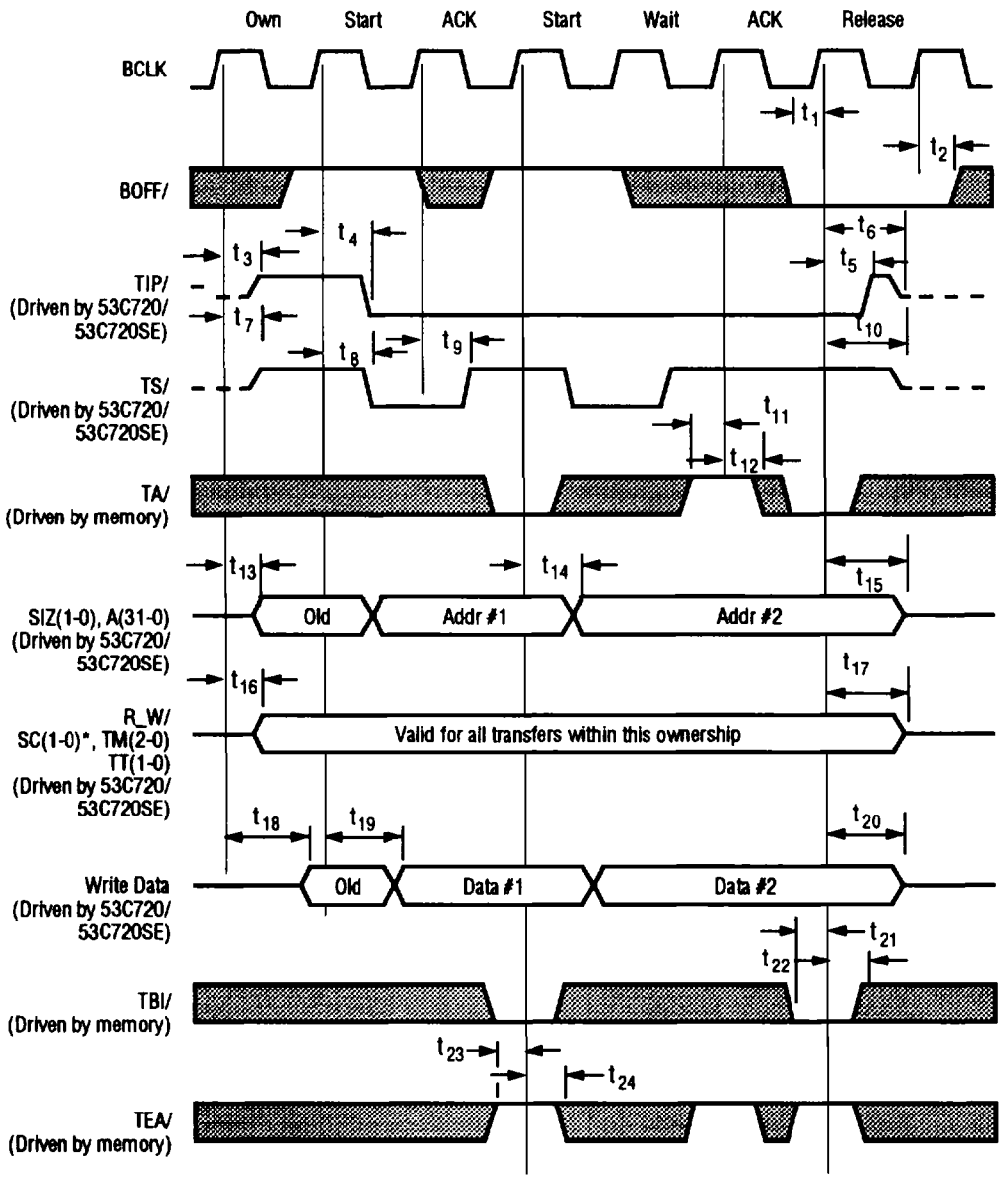
Figure 7-22: Bus Mode 2 Bus Master Read (Cache Line Burst)

Table 7-26: Bus Mode 2 Bus Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	4	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	5	20	ns
BCLK high to A(31-0), SIZ(1-0)	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read data hold from BCLK high	t_{19}	6	-	ns
Read data setup to DLE low	t_{20}	4	-	ns
Read data hold from DLE low	t_{21}	6	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns

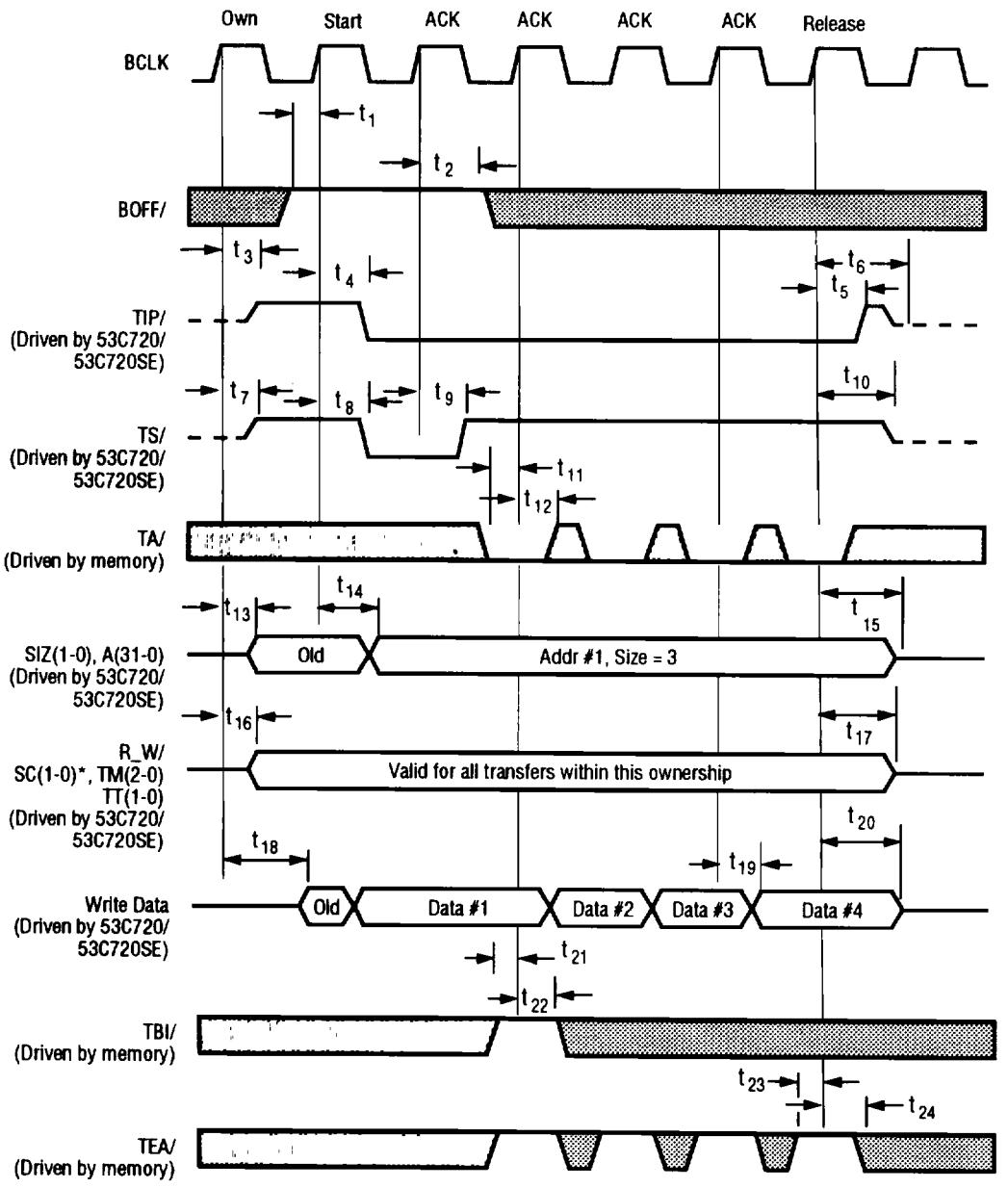
Bus Mode 2
Bus Master Write Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the R_W/, Snoop Control, Transfer Modifier, and Transfer Type Lines.
3.
   a. The NCR 53C720/53C720SE asserts Transfer in Progress
   b. The NCR 53C720/53C720SE asserts Transfer Start, Address, Size lines, and Data lines.
4. The NCR 53C720/53C720SE deasserts Transfer Start.
5. The NCR 53C720/53C720SE waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the NCR 53C720/53C720SE requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master, Busy, and Transfer in Progress.
7. The NCR 53C720/53C720SE floats the Control, Address, and Data lines.



**SC(1-0) timings apply only if the Snoop Mode bit (bit 0 of CTEST3) is zero.*

Figure 7-23: Bus Mode 2 Bus Master Write (Cache Line Burst Requested but not Acknowledged)



**SC(1-0) timings apply only if the Snoop Mode bit (CTEST3, bit 0) is zero.*

Figure 7-24: Bus Mode 2 Bus Master Write (Cache Line Burst)

Table 7-27: Bus Mode 2 Bus Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to TS/ driven	t_7	5	30	ns
BCLK high to TS/ low	t_8	3	17	ns
BCLK high to TS/ high	t_9	3	17	ns
BCLK high to TS/ high-Z	t_{10}	7	32	ns
TA/ setup to BCLK high	t_{11}	9	-	ns
TA/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-0), SIZ(1-0) driven	t_{13}	5	30	ns
BCLK high to A(31-0), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-0), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to R_W/, SC(1-0), TM(2-0), TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to write data driven	t_{18}	5	34	ns
BCLK high to write data valid	t_{19}	7	24	ns
BCLK high to Write data high-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns

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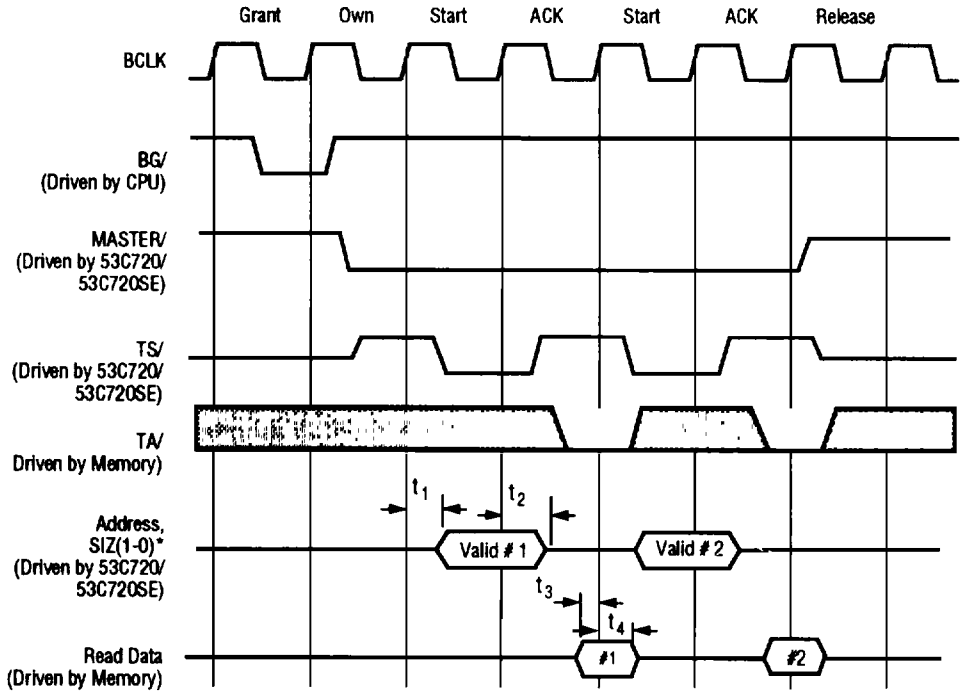
Bus Mode 2 Mux Mode Cycle

Mux Mode Read Sequence

1. The NCR 53C720/53C720SE has attained bus mastership
2. The NCR 53C720/53C720SE asserts the R_W/, Snoop Control, Function Control, and Transfer Type lines.
3.
   a. The NCR 53C720/53C720SE asserts Transfer in Progress .
   b. The NCR 53C720/53C720SE asserts the Transfer Start, Address, and Size lines.
4. The NCR 53C720/53C720SE deasserts Transfer Start and floats the address lines.
5. The NCR 53C720/53C720SE waits for transfer acknowledge, Valid Data driven on the data pins, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted and Transfer Error Acknowledge is not asserted and the NCR 53C720/53C720SE requires more cycles, then return to step 3b.
6. The NCR 53C720/53C720SE deasserts the control lines.
7. Upon acknowledgment of the last bus cycle, the NCR 53C720/53C720SE deasserts Master and Bus Grant Acknowledge.

Note: this mode of operation expects D(31-0) to be physically tied to A(31-0), respectively.



* *For cache line bursting, the value of the SIZ(1-0) bits must be 03h*

Figure 7-25: Mux Mode Read Cycle (Cache Line Burst Requested but not Acknowledged)

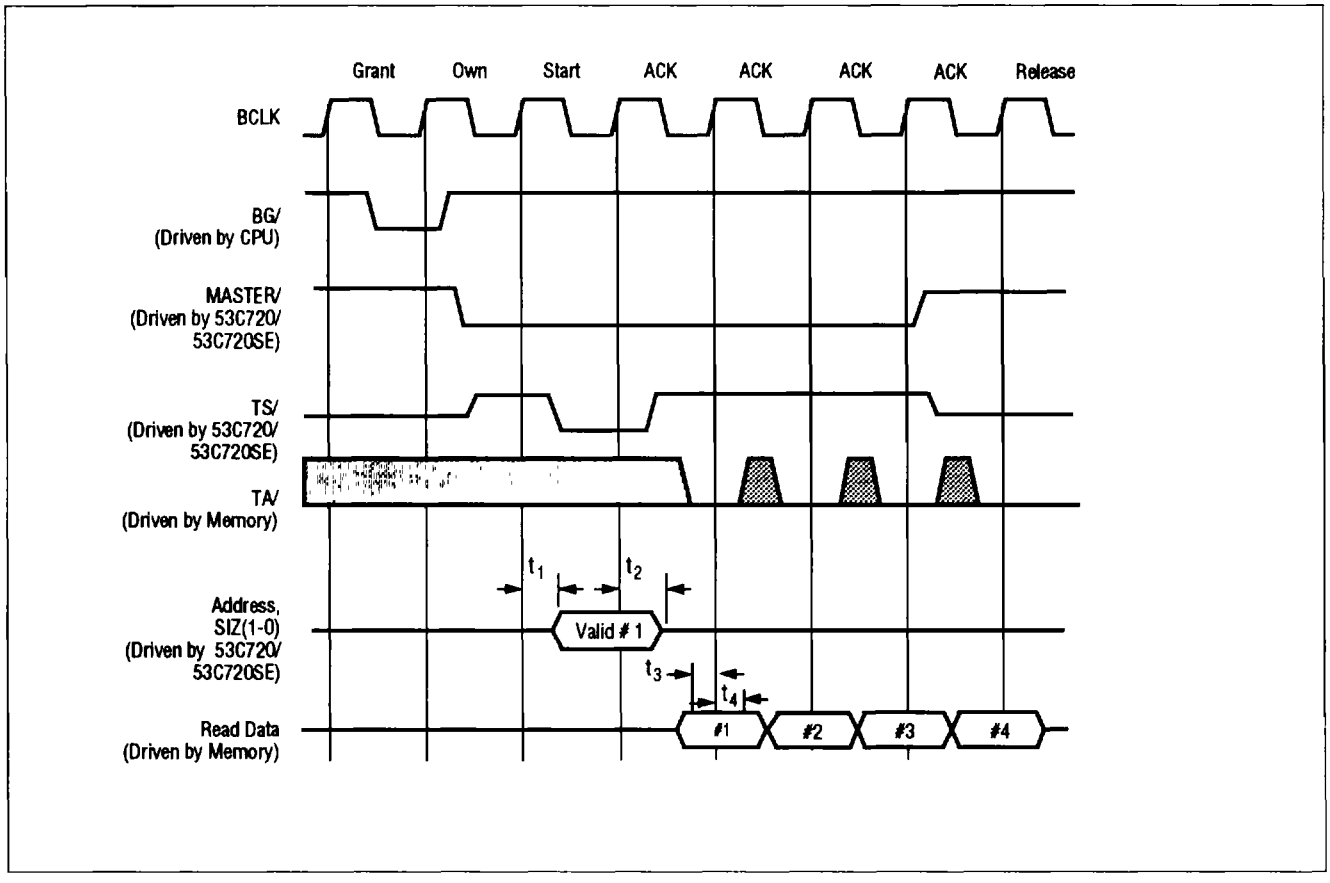


Figure 7-26: Mux Mode Read Cycle (Cache Line Burst)

Table 7-28: Bus Mode 2 Mux Mode Read Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Address driven	t_1	5	22	ns
BCLK high to Address high-Z	t_2	-	23	ns
Read Data setup to BCLK high	t_3	5	-	ns
Read data hold from BCLK high	t_4	6	-	ns

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Mux Mode Write Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the Read/Write, Snoop Control, Function Control, and Transfer Type lines.
3.
   a. The NCR 53C720/53C720SE asserts Transfer in Progress.
   b. The NCR 53C720/53C720SE asserts Transfer Start, Address, Size lines, and floats the Data lines.
4. The NCR 53C720/53C720SE deasserts Transfer Start, floats the address bus, and asserts the data bus.
5. The NCR 53C720/53C720SE waits for Transfer Acknowledge, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Transfer Acknowledge is not asserted, a bus fault condition will be generated.
   - If Transfer Acknowledge is asserted, Transfer Error Acknowledge is not asserted, and the NCR 53C720/53C720SE requires more cycles, return to step 3b.
6. The NCR 53C720/53C720SE deasserts the Control and Data lines.
7. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master and Bus Grant Acknowledge.

Note: This mode of operation expects D(31-0) to be physically tied to A(31-0), respectively.

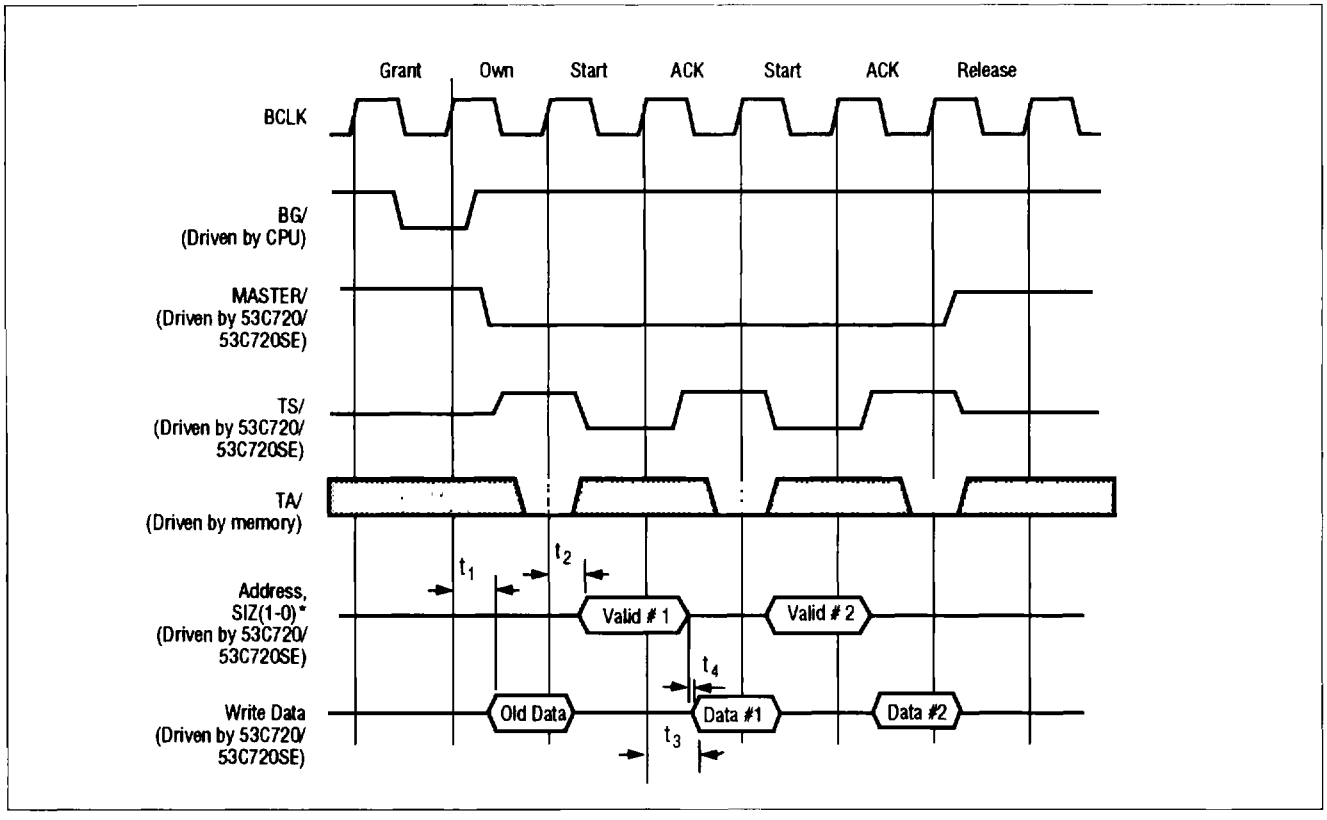

Figure 7-27: Mux Mode Write Cycle (Non-Cache Line Burst)

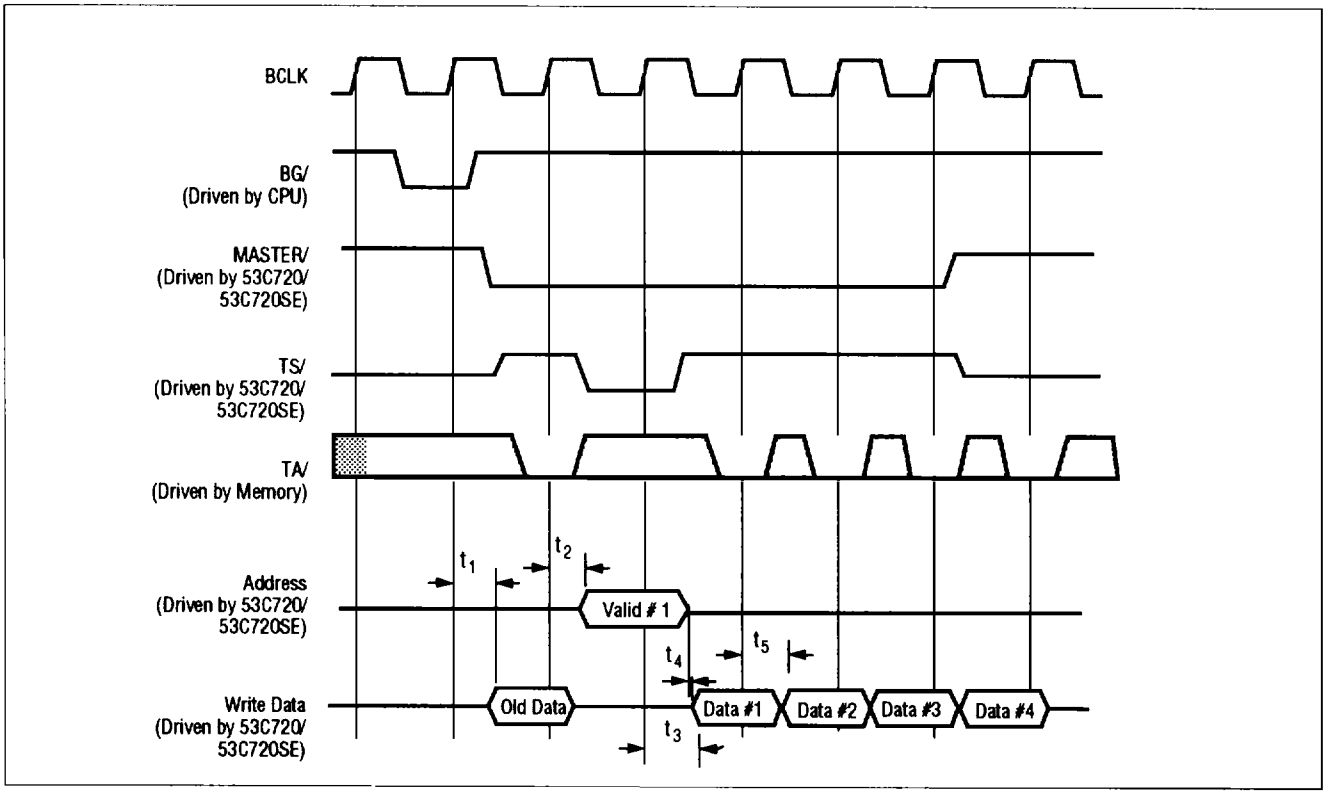

Figure 7-28: Mux Mode Write Cycle (Cache Line Burst)

Table 7-29: Bus Mode 2 Mux Mode Write Timings

Parameter	Symbol	Min	Max	Units
BCLK high to Old Data driven	t_1	-	34	ns
BCLK high to Address driven	t_2	5	22	ns
BCLK high to New Data driven	t_3	8	24	ns
Write data High-Z to driven switching time	t_4	1	-	ns
BCLK high to Next Data	t_5	-	24	ns

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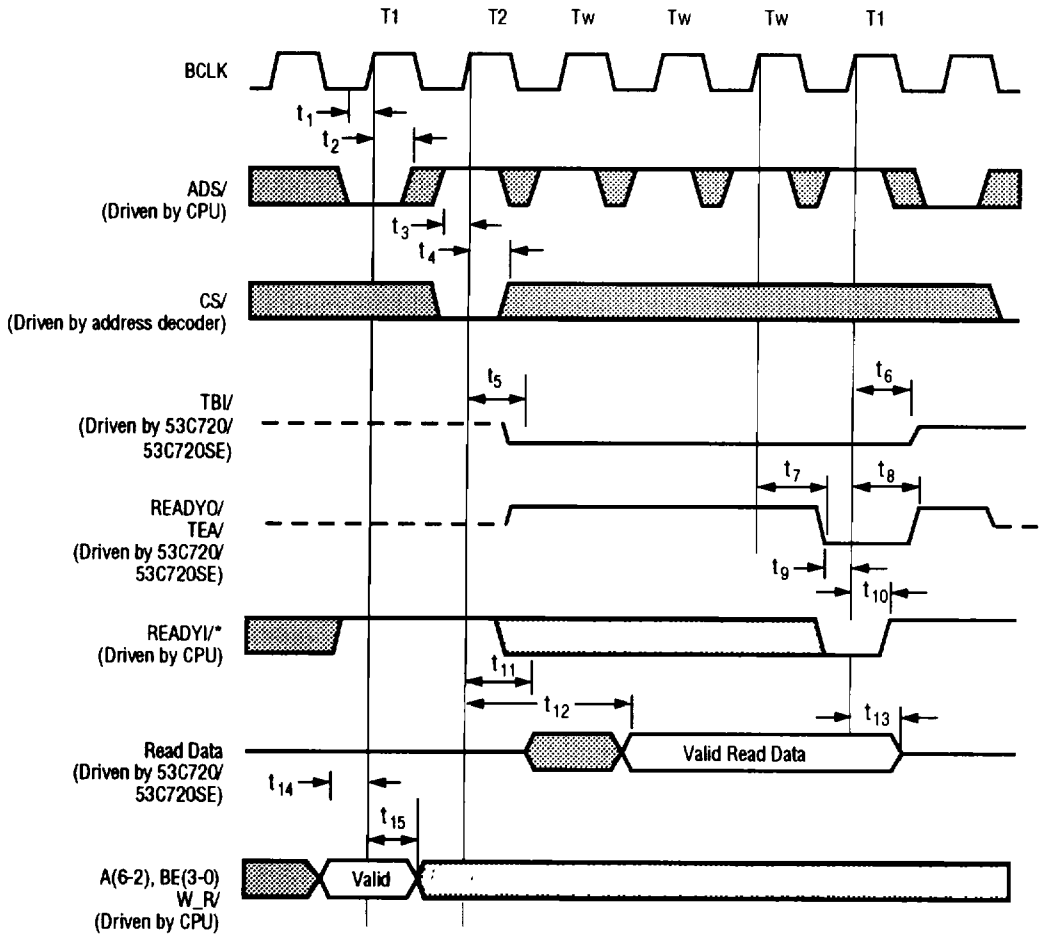
Bus Mode 3 and 4 Slave Cycle

Bus Mode 3 and 4 Slave Read Sequence

1. Address, Address Status, and the Byte Enable signals are asserted by the CPU.
2. Chip Select is validated by the NCR 53C720/53C720SE on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Address Status may be deasserted by the CPU.
5. Three clock cycles of wait state are inserted (these wait states are required) and the Data lines are asserted.
6. Ready Out is asserted by NCR 53C720/53C720SE, if no errors are detected.
7. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
8. Ready Out or Transfer Error Acknowledge is deasserted.
9. The NCR 53C720/53C720SE waits for Ready In to be asserted and then ends the slave cycle, if no errors are detected.
10. The Data lines are tristated by the NCR 53C720/53C720SE.

Recommended Setup for Bus Mode 3 and 4

1. Disable Cache Line Burst Mode (if cache line is not supported; set CTEST0, bit 7).
2. Set the Bus Mode bit (DCNTL, bit 6).
3. Set the Snoop Mode bit (CTEST3, bit0).
4. Tie BB/ high resistively.
5. Tie TEA/ high resistively.



** This signal may be driven by the NCR 53C720/53C720SE if the Enable Acknowledge bit is set (DCNTL bit 5). See the explanation in Chapter 2 of this manual for use of this signal as an output.*

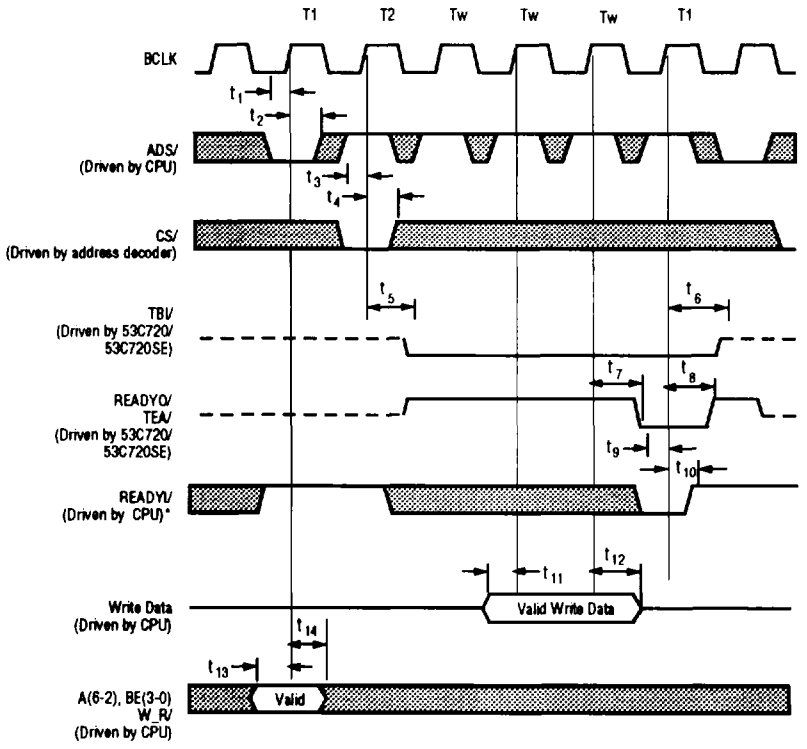
Figure 7-29: Bus Mode 3 and 4 Slave Read Cycle

Table 7-30: Bus Mode 3 and 4 Slave Read Timings

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	20	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	9	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	5	-	ns
BCLK high to data bus driven	t_{11}	8	28	ns
BCLK high to read data valid	t_{12}	-	75	ns
BCLK high to data bus high-Z	t_{13}	7	34	ns
A(6-0), SIZ(1-0), W_R/ setup to BCLK high	t_{14}	4	-	ns
A(6-0), SIZ(1-0), W_R/ hold from BCLK high	t_{15}	12	-	ns

Bus Mode 3 and 4 Slave Write Sequence

1. W_R/, the address lines, and the Address Status and Byte Enable signals are asserted by the CPU.
2. Chip Select is validated by the NCR 53C720/53C720SE on any following rising edge of BCLK.
3. Transfer Burst Inhibit is asserted.
4. Address Status may be deasserted by the CPU.
5. The data lines are asserted by the CPU.
6. Three clock cycles of wait state are inserted (these wait states are required).
7. Ready Out is asserted by the NCR 53C720/53C720SE, if no errors are detected.
8. If a bus error is detected, only Transfer Error Acknowledge is asserted and the bus cycle ends on the next rising edge of BCLK.
9. Ready Out or Transfer Error Acknowledge is deasserted.
10. The NCR 53C720/53C720SE waits for Ready In to be asserted and then ends the slave cycle, if there are no errors.



**This signal may be driven by the NCR 53C720/53C720SE if the Enable Acknowledge bit (DCNTL bit 5) is set. See the explanation in Chapter 2 of this manual for use of this signal as an output.*

Figure 7-30: Bus Mode 3 and 4 Slave Write Cycle

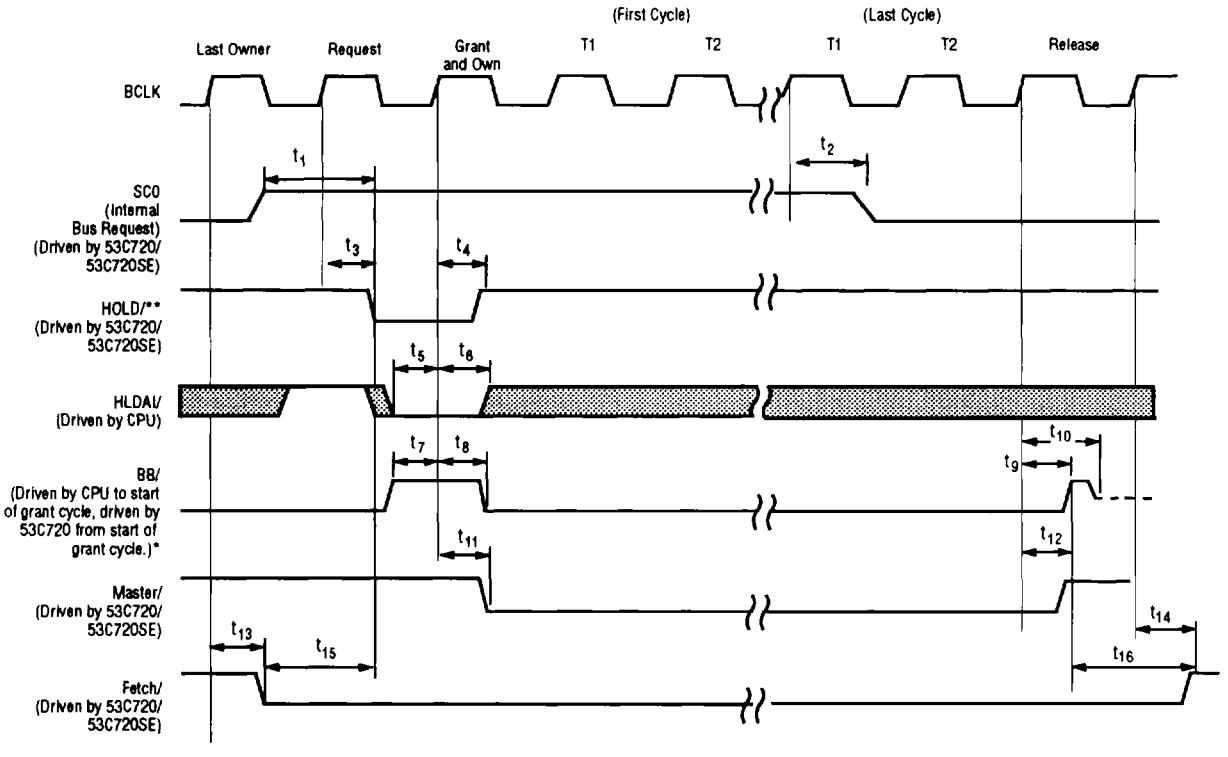
Table 7-31: Bus Mode 3 and 4 Slave Write Timings

Parameter	Symbol	Min	Max	Units
ADS/ setup to BCLK high	t_1	4	-	ns
ADS/ hold from BCLK high	t_2	4	-	ns
CS/ setup to BCLK high after ADS/	t_3	5	-	ns
CS/ hold from BCLK high after ADS/	t_4	5	-	ns
BCLK high to TBI/ low	t_5	5	30	ns
BCLK high to TBI/ high	t_6	4	22	ns
BCLK high to READYO/, TEA/ low	t_7	5	20	ns
BCLK high to READYO/, TEA/ high	t_8	4	20	ns
READYI/ setup to BCLK high during or after READYO/, TEA/	t_9	9	-	ns
READYI/ hold from BCLK high during or after READYO/, TEA/	t_{10}	5	-	ns
Valid write data setup to BCLK high	t_{11}	6	-	ns
Valid write data hold from BCLK high	t_{12}	14	-	ns
A(6-0), SIZ(1-0), W_R/ setup to BCLK high	t_{13}	4	-	ns
A(6-0), SIZ(1-0), W_R/ hold from BCLK high	t_{14}	12	-	ns

Bus Mode 3 and 4 Host Bus Arbitration

Bus Arbitration Sequence

1. The NCR 53C720/53C720SE internally determines bus mastership is required. FETCH/ is asserted during cycles in which the NCR 53C720/53C720SE is retrieving new SCRIPTS instructions.
2. HOLD/ is asserted.
3. The NCR 53C720/53C720SE waits for Hold Acknowledge and checks that Bus Busy is deasserted. Then the NCR 53C720/53C720SE asserts Hold Acknowledge and Master, and deasserts Hold.



** BB/ should be tied high resistively if not used.*

***HOLD/ may be NANDed with MASTER/ to obtain HOLD required by the 80286 or 80386 processors.*

Note: the NCR 53C720/53C720SE will periodically assert the HOLD/ signal and receive a SCSI interrupt at the same time. When this happens, the chip will wait for the HLDAI/ signal to complete the normal bus arbitration and handshake. The chip no longer wants host bus access—it deasserts the HOLD/, MASTER/, and all control lines after one BCLK, and does not assert ADS/, the signal that indicates a valid bus cycle is starting. The chip will then generate an interrupt, which the system may then service.

Figure 7-31: Bus Modes 3 and 4 Host Bus Arbitration

Table 7-32: Bus Mode 3 and 4 Bus Arbitration Timings

Parameter	Symbol	Min	Max	Units
SC0 high to HOLD/ low*	t_1	1	2	BCLK
BCLK high to SC0 low on last cycle*	t_2	5	28	ns
BCLK high to HOLD/ low	t_3	4	20	ns
BCLK high to HOLD/ high	t_4	5	25	ns
HLDAI/ setup to BCLK high (any rising edge after HOLD/)	t_5	4	-	ns
HLDAI/ hold from BCLK high (any rising edge after HOLD/)	t_6	5	-	ns
BB/ setup to BCLK high (any rising edge after HOLD/)	t_7	4	-	ns
BCLK high to BB/ low	t_8	4	24	ns
BCLK high to BB/ high	t_9	3	19	ns
BCLK high to BB/ high-Z	t_{10}	7	32	ns
BCLK high to MASTER/ low	t_{11}	5	22	ns
BCLK high to MASTER/ high	t_{12}	6	26	ns
BCLK high to FETCH/ low	t_{13}	5	36	ns
BCLK high to FETCH/ high	t_{14}	5	36	ns
RETCH/ low to HOLD/ low	t_{15}	1	2	BCLK
BB/ high to FETCH/ high**	t_{16}	1	2	BCLK

**When Snoop Mode bit 0 of CTEST3 is set to 1.*

***During a retry operation, FETCH/ will remain low until a successful completion of the op code fetch or a fatal bus error.*

Bus Mode 3 and 4 Fast Arbitration

Fast Arbitration Sequence

1. The NCR 53C720/53C720SE internally determines if bus mastership is required. FETCH/ is asserted during cycles in which the NCR 53C720/53C720SE is retrieving new SCRIPTS instructions.
2. HOLD/ is asserted.
3. The NCR 53C720/53C720SE waits for Hold Acknowledge (HLDAI). The NCR 53C720/53C720SE becomes bus master asynchronously on the leading edge of HLDAI/. The the NCR 53C720/53C720SE asynchronously asserts Bus Busy and Master, and deasserts HOLD/.
4. The NCR 53C720/53C720SE issues a start cycle on the next rising edge of BCLK.

Note: in fast arbitration mode, the NCR 53C720/53C720SE will take bus ownership on the assertion of HLDAI, regardless of the state of HOLD/ or BB/.

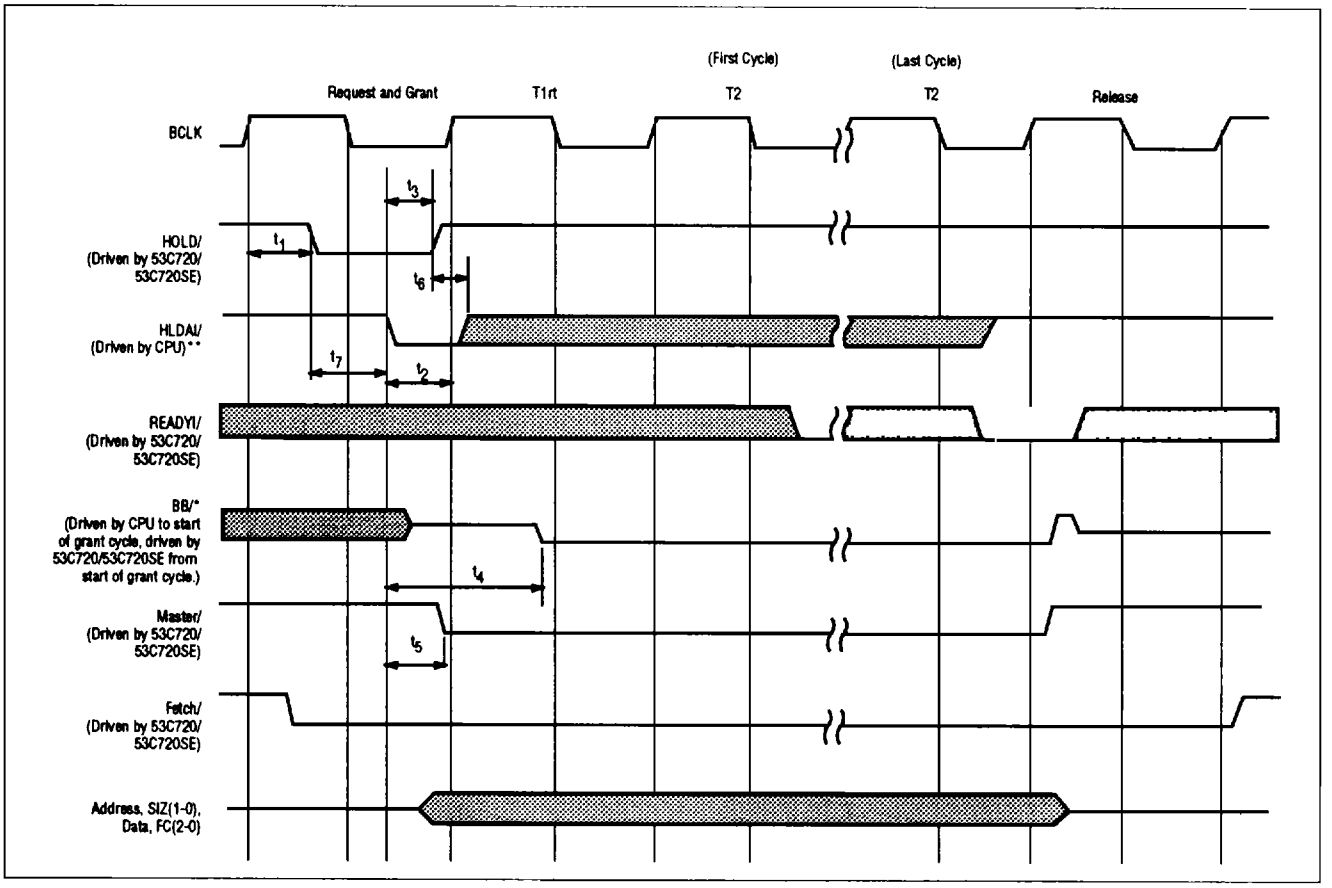


Figure 7-32: Bus Mode 3 and 4 Fast Arbitration

Table 7-33: Bus Mode 3 and 4 Fast Arbitration

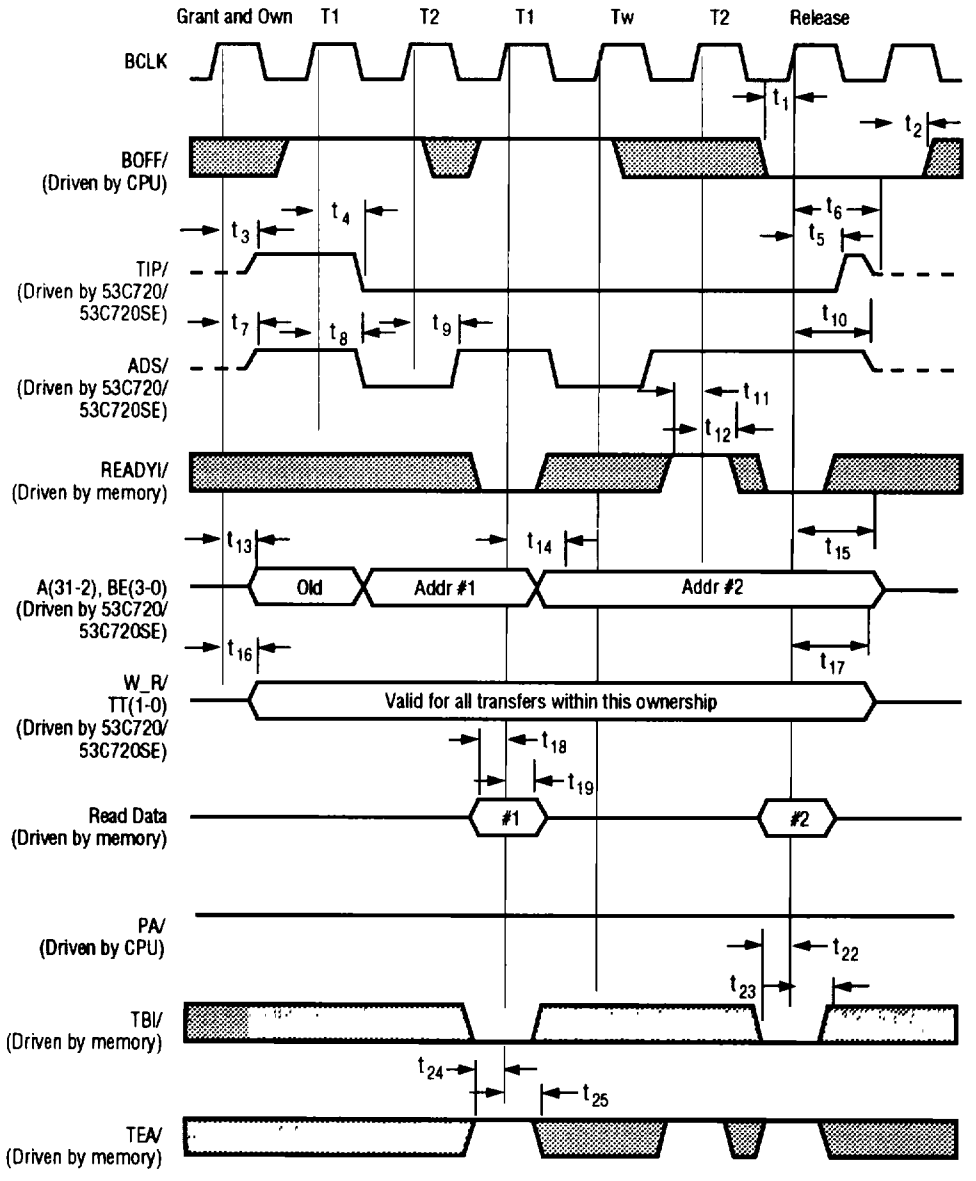
Parameter	Symbol	Min	Max	Units
BCLK high to HOLD/ asserted	t_1	-	20	ns
HLDAI/ setup to BCLK high	t_2	12	-	ns
HLDAI/ asserted to HOLD/ deasserted	t_3	-	22	ns
HLDAI/ asserted to BB/ asserted	t_4	-	20	ns
HLDAI/ asserted to MASTER/ asserted	t_5	-	16	ns
HLDAI/ hold after HOLD/ deasserted*	t_6	0	-	ns
HOLD/ asserted to HLDAI/ asserted	t_7	0	-	ns

**HLDAI/ may not be asserted prior to HOLD/*

Bus Mode 3 and 4 Master Cycle

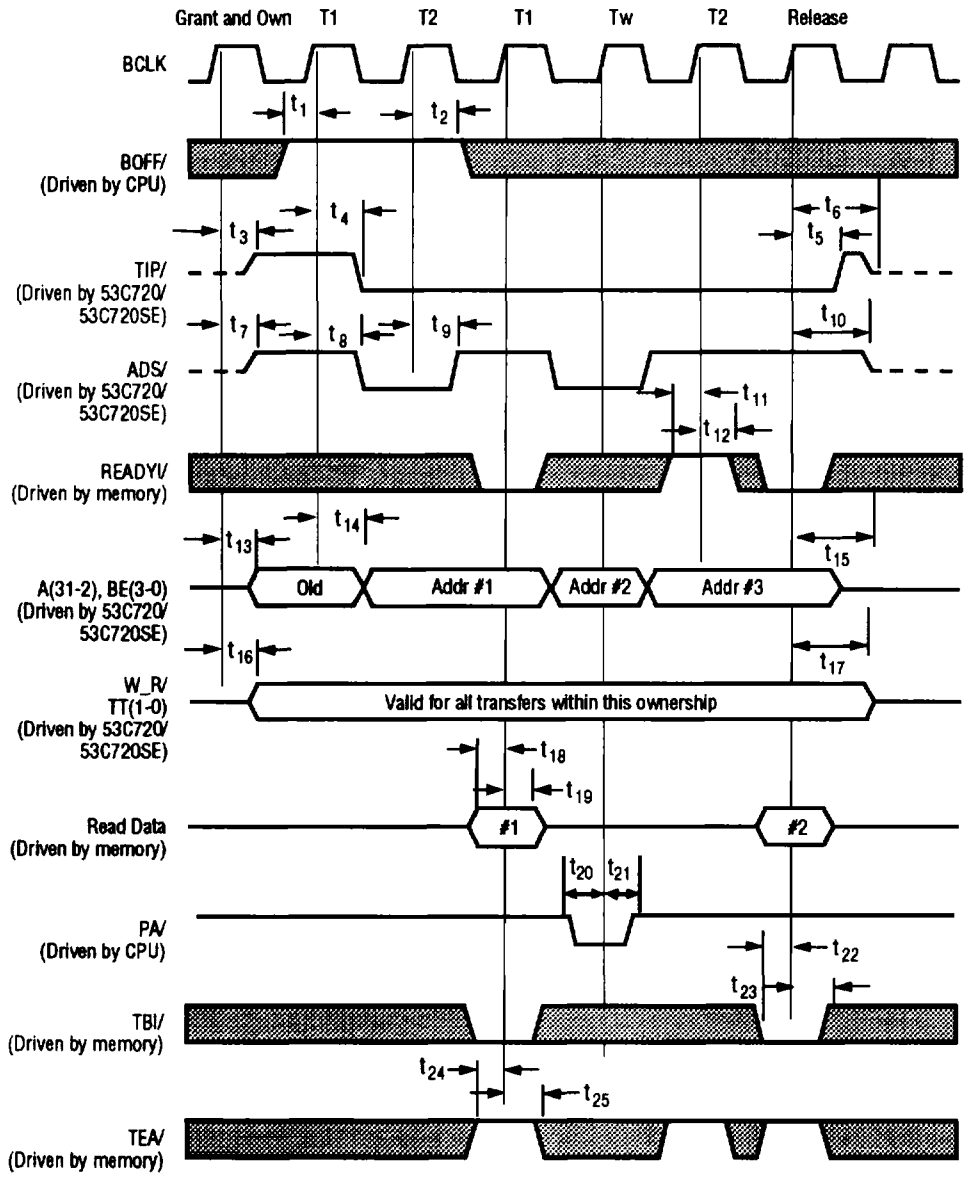
Bus Mode 3 and 4 Bus Master Read Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the W_R/, Transfer Modifier and Transfer Type lines.
3.
   a. The NCR 53C720/53C720SE asserts Transfer in Progress
   b. The NCR 53C720/53C720SE asserts Address Status, Address, and Busy Enable signals.
4. The NCR 53C720/53C720SE deasserts Address Status.
5. The NCR 53C720/53C720SE waits for Transfer Acknowledge, Valid Data, Transfer Burst Inhibit, and Transfer Error Acknowledge
   - If Transfer Burst Inhibit is not asserted attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.
   - If Ready In is asserted and Transfer Error Acknowledge is not asserted and the NCR 53C720/53C720SE requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master, Bus Busy, and Transfer in Progress.
7. The NCR 53C720/53C720SE floats the Control and Address lines.



Note: this diagram shows two back-to-back cycles for a burst size of two.

Figure 7-33: Bus Mode 3 and 4 Bus Master Read (Non-Preview of Address)

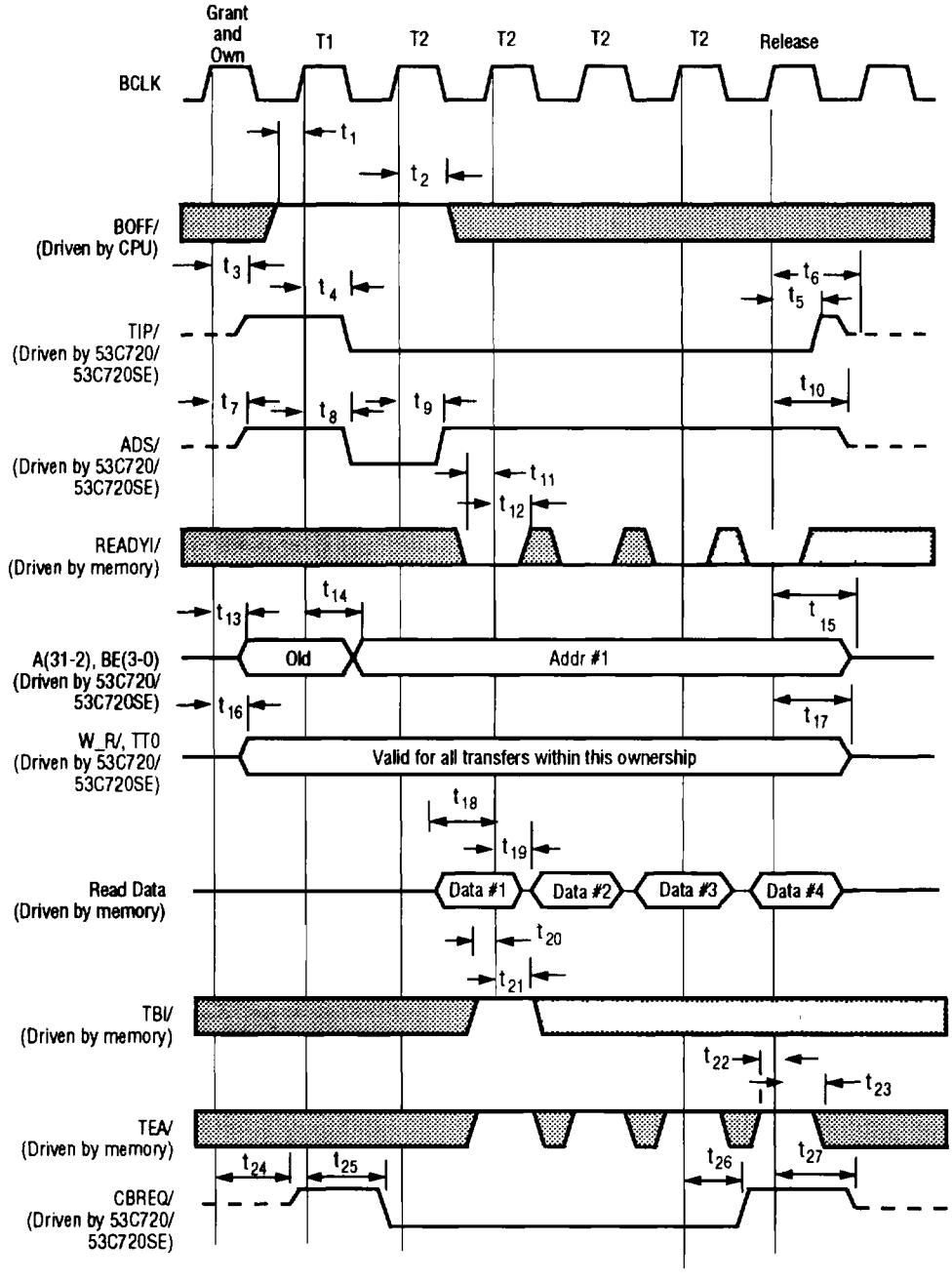


Note: this diagram shows two back-to back cycles for a burst size of two

Figure 7-34: Bus Mode 3 and 4 Bus Master Read (Preview of Address)

Table 7-34: Bus Mode 3 and 4 Bus Master Read Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READY/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	-	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
PA/ setup to BCLK high	t_{20}	5	-	ns
PA/ hold from BCLK high	t_{21}	5	-	ns
TBI/ setup to BCLK high	t_{22}	6	-	ns
TBI/ hold from BCLK high	t_{23}	4	-	ns
TEA/ setup to BCLK high	t_{24}	9	-	ns
TEA/ hold from BCLK high	t_{25}	5	-	ns



Note: this diagram shows one cache line burst of four.

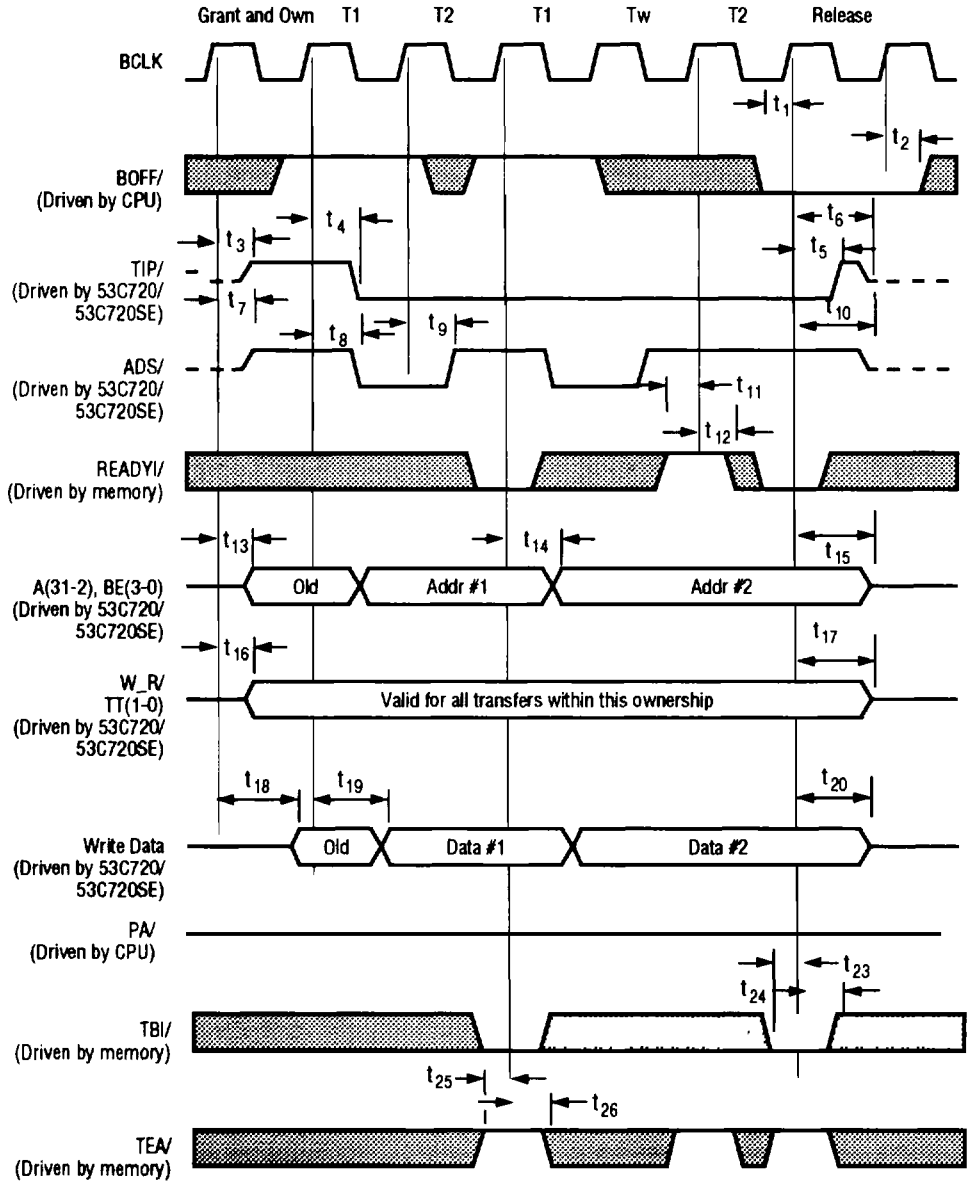
Figure 7-35: Bus Mode 4 Bus Master Read (Cache Line Burst)

Table 7-35: Bus Mode 4 Bus Master Read Timings (Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	5	32	ns
Read Data setup to BCLK high	t_{18}	6	-	ns
Read Data hold from BCLK high	t_{19}	6	-	ns
TBI/ setup to BCLK high	t_{20}	6	-	ns
TBI/ hold from BCLK high	t_{21}	4	-	ns
TEA/ setup to BCLK high	t_{22}	9	-	ns
TEA/ hold from BCLK high	t_{23}	5	-	ns
BCLK high to CBREQ/ driven	t_{24}	5	28	ns
BCLK high to CBREQ/ low	t_{25}	5	20	ns
BCLK/ high to CBREQ/ high	t_{26}	5	20	ns
BCLK high to CBREQ/ high-Z	t_{27}	7	32	ns

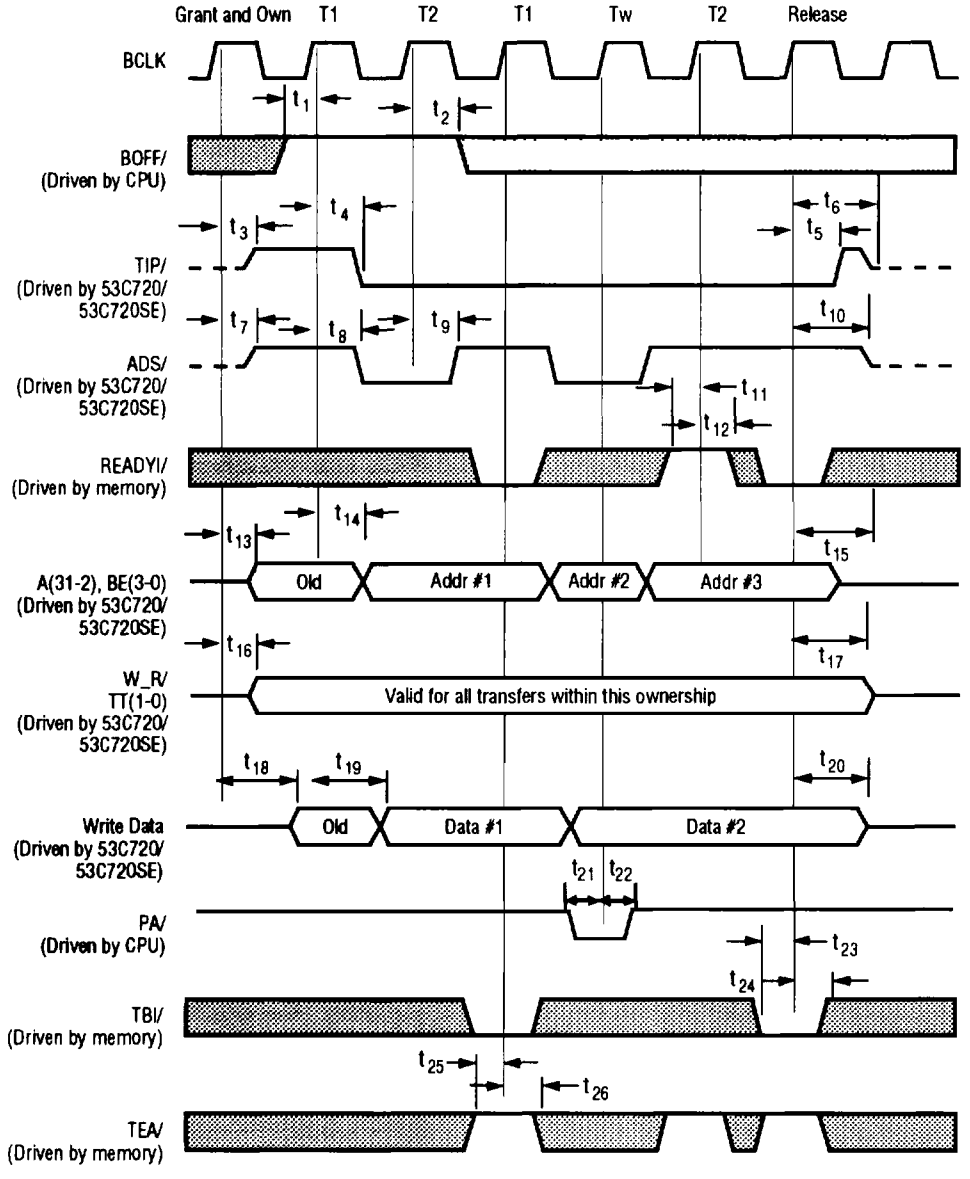
Bus Mode 3 and 4 Bus Master Write Sequence

1. The NCR 53C720/53C720SE has attained bus mastership.
2. The NCR 53C720/53C720SE asserts the W_R/, Transfer Modifier, and Transfer Type lines.
3.
   a. The NCR 53C720/53C720SE asserts Transfer in Progress.
   b. The NCR 53C720/53C720SE asserts the Address Status and Byte Enable signals, and the Address and Data lines.
4. The NCR 53C720/53C720SE deasserts Address Status.
5. The NCR 53C720/53C720SE waits for Ready In, Transfer Burst Inhibit, and Transfer Error Acknowledge.
   - If Transfer Burst Inhibit is not asserted, attempt cache bursting. Otherwise, proceed with non-cache transfers.
   - If Transfer Error Acknowledge and Transfer Acknowledge are asserted, attempt a retry.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted, a bus fault condition will be generated.
   - If Transfer Error Acknowledge is asserted and Ready In is not asserted and the NCR 53C720/53C720SE requires more cycles, then return to step 3b.
6. Upon acknowledge of the last bus cycle, the NCR 53C720/53C720SE deasserts Master, Busy, and Transfer in Progress.
7. The NCR 53C720/53C720SE floats the Control, Address, and Data Lines.



Note: this diagram shows two back-to-back transfers for a transfer size of two.

Figure 7-36: Bus Mode 3 and 4 Bus Master Write (Non-Preview of Address)

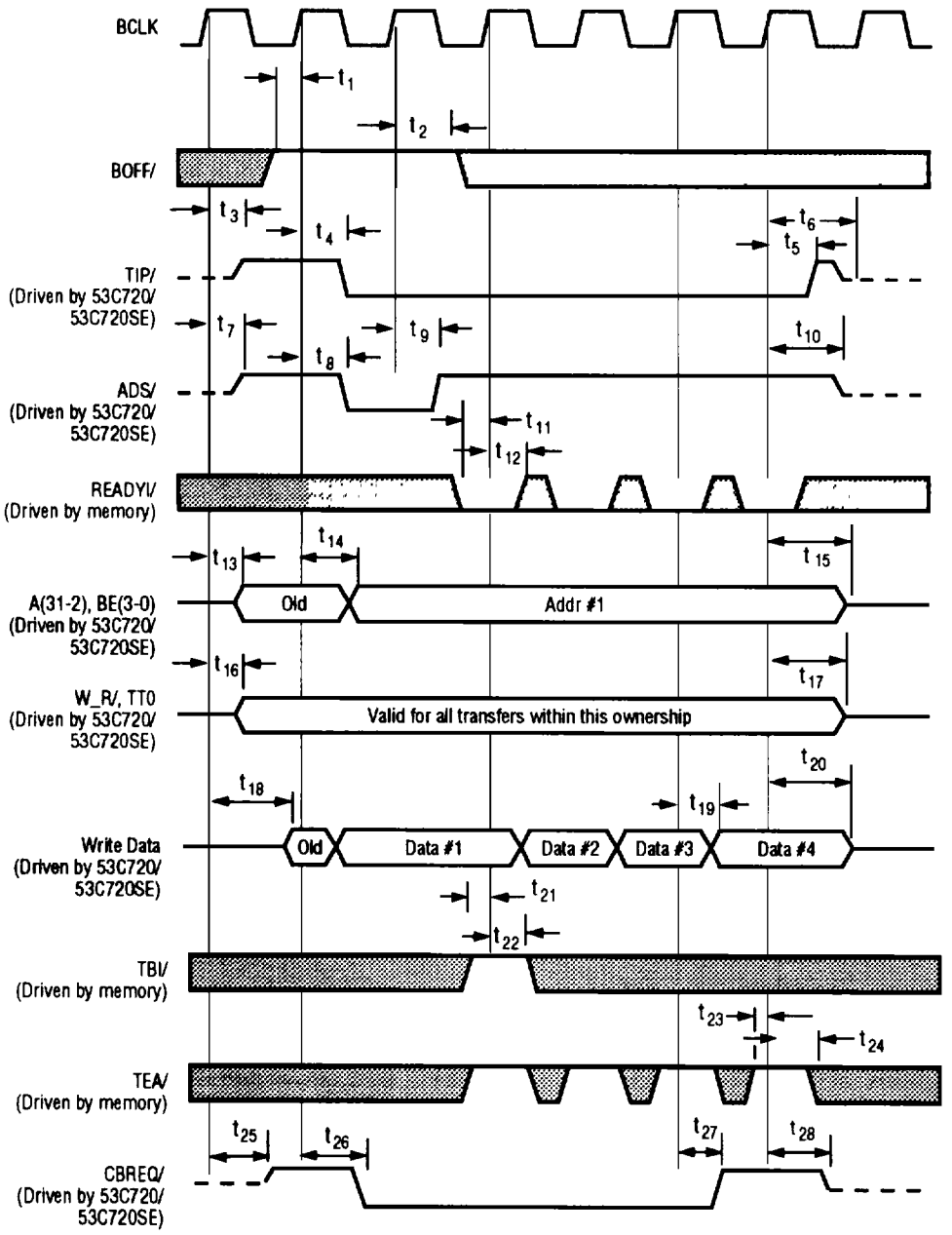


Note: this diagram shows one cahce line burst of four.

Figure 7-37: Bus Mode 3 and 4 Bus Master Write (Preview of Address)

Table 7-36: Bus Mode 3 and 4 Bus Master Write Timings

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	4	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READY/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	5	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
PA/ setup to BCLK high	t_{21}	5	-	ns
PA/ hold from BCLK high	t_{22}	5	-	ns
TBI/ setup to BCLK high	t_{23}	6	-	ns
TBI/ hold from BCLK high	t_{24}	4	-	ns
TEA/ setup to BCLK high	t_{25}	9	-	ns
TEA/ hold from BCLK high	t_{26}	5	-	ns



Note: this diagram shows two back-to-back transfers for a burst size of two.

Figure 7-38: Bus Mode 4 Bus Master Write (Cache Line Burst)

Table 7-37: Bus Mode 4 Bus Master Write Timings (Cache Line Burst)

Parameter	Symbol	Min	Max	Units
BOFF/ setup to BCLK high	t_1	8	-	ns
BOFF/ hold from BCLK high	t_2	7	-	ns
BCLK high to TIP/ driven	t_3	5	32	ns
BCLK high to TIP/ low	t_4	3	20	ns
BCLK high to TIP/ high	t_5	3	20	ns
BCLK high to TIP/ high-Z	t_6	7	32	ns
BCLK high to ADS/ driven	t_7	5	30	ns
BCLK high to ADS/ low	t_8	3	17	ns
BCLK high to ADS/ high	t_9	3	17	ns
BCLK high to ADS/ high-Z	t_{10}	7	32	ns
READYI/ setup to BCLK high	t_{11}	9	-	ns
READYI/ hold from BCLK high	t_{12}	5	-	ns
BCLK high to A(31-2), SIZ(1-0) driven	t_{13}	5	28	ns
BCLK high to A(31-2), SIZ(1-0) valid	t_{14}	3	20	ns
BCLK high to A(31-2), SIZ(1-0) high-Z	t_{15}	7	32	ns
BCLK high to W_R/, TT(1-0) driven and valid	t_{16}	5	30	ns
BCLK high to W_R/, TT(1-0) high-Z	t_{17}	5	32	ns
BCLK high to Write Data driven	t_{18}	5	34	ns
BCLK high to Write Data valid	t_{19}	5	24	ns
BCLK high to Write Data high-Z	t_{20}	5	30	ns
TBI/ setup to BCLK high	t_{21}	6	-	ns
TBI/ hold from BCLK high	t_{22}	4	-	ns
TEA/ setup to BCLK high	t_{23}	9	-	ns
TEA/ hold from BCLK high	t_{24}	5	-	ns
BCLK high to CBREQ/ driven	t_{25}	5	28	ns
BCLK high to CBREQ/ low	t_{26}	5	20	ns
BCLK high to CBREQ/ high	t_{27}	5	20	ns
BCLK high to CBREQ/ high-Z	t_{28}	7	32	ns

SCSI Timings

Initiator Asynchronous Send

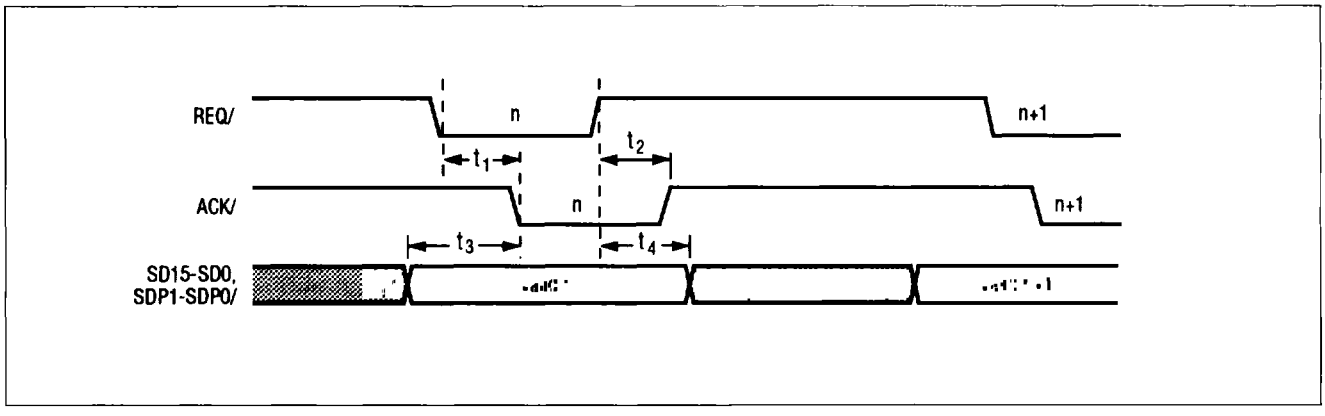


Figure 7-39: Initiator Asynchronous Send

Table 7-38: Initiator Asynchronous Send Timings

Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

Initiator Asynchronous Receive

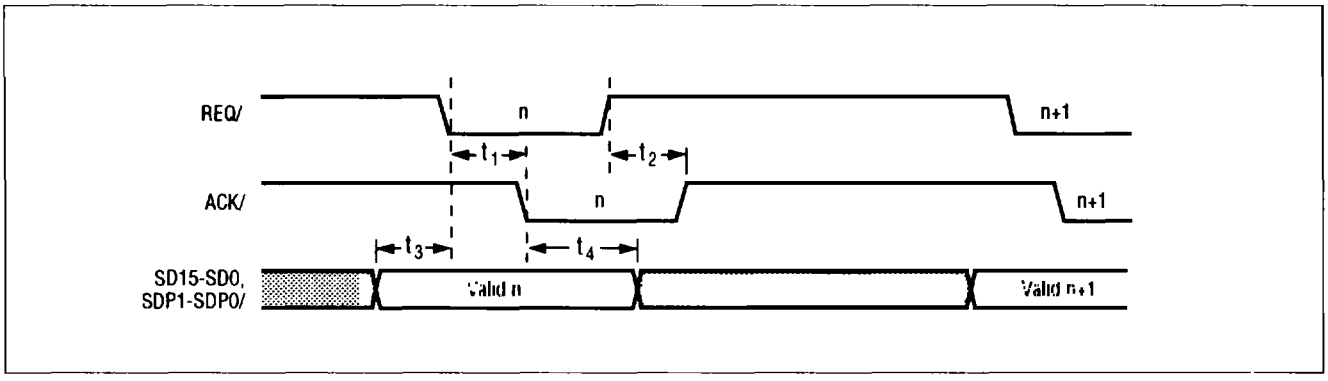


Figure 7-40: Initiator Asynchronous Receive

Table 7-39: Initiator Asynchronous Receive Timings

Parameter	Symbol	Min	Max	Units
ACK/ asserted from REQ/ asserted	t_1	10	-	ns
ACK/ deasserted from REQ/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	0	-	ns
Data hold from ACK/ asserted	t_4	0	-	ns

Target Asynchronous Send

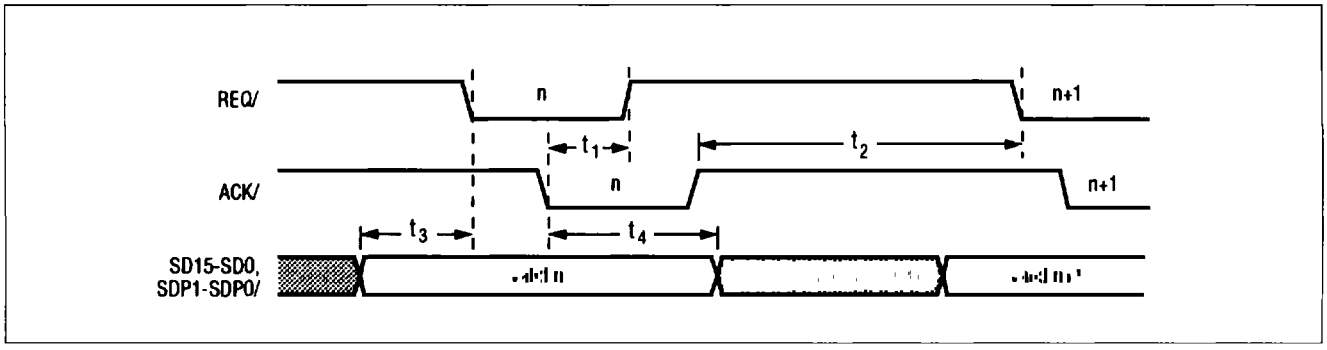


Figure 7-41: Target Asynchronous Send Waveforms

Table 7-40: Target Asynchronous Send Timings

Parameter	Symbol	Min	Max	Units
REQ/ deasserted from ACK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to REQ/ asserted	t_3	55	-	ns
Data hold from ACK/ asserted	t_4	20	-	ns

Target Asynchronous Receive

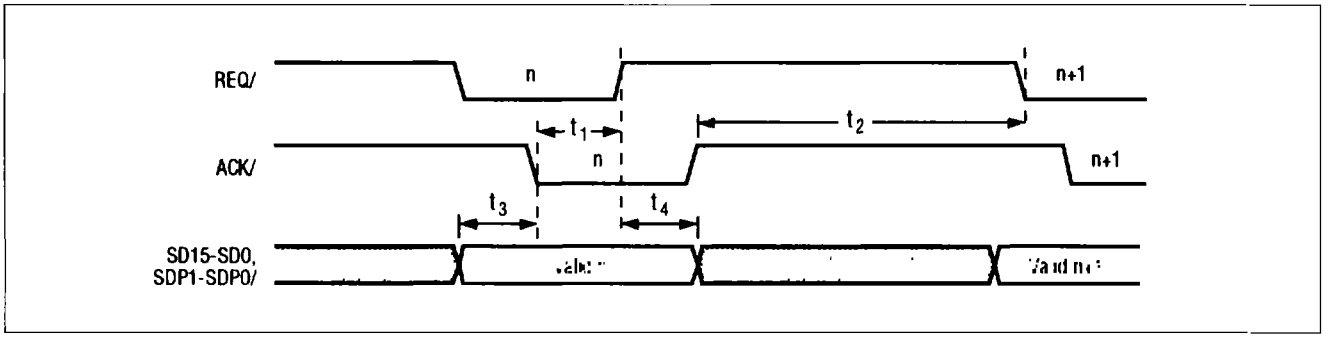


Figure 7-42: Target Asynchronous Receive

Table 7-41: Target Asynchronous Receive Timings

Parameter	Symbol	Min	Max	Units
REQ/ deasserted from CK/ asserted	t_1	10	-	ns
REQ/ asserted from ACK/ deasserted	t_2	10	-	ns
Data setup to ACK/ asserted	t_3	0	-	ns
Data hold from REQ/ deasserted	t_4	0	-	ns

Initiator and Target Synchronous Transfers

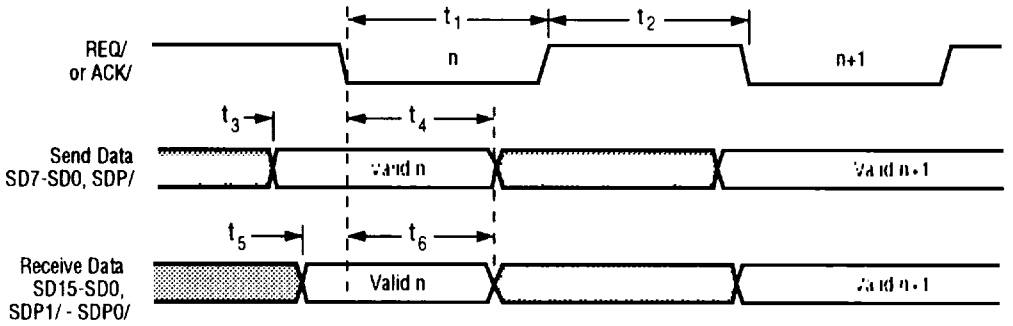


Figure 7-43: Initiator and Target Synchronous Transfers

Table 7-42: SCSI-1 Transfers (Single-ended, 5.0 MB/s)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	90	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	90	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	55	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	100	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

Table 7-43: SCSI-1 Transfers (Differential, 4.17 MB/s) (NCR 53C720 Only)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	96	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	96	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	84	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	84	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	65	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	110	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	45	-	ns

Table 7-44: SCSI-2 Fast Transfers (10.0 MB/s, 40 MHz clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	20	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	20	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	45	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

Table 7-45: SCSI-2 Fast Transfers (10.0 MB/s, 50 MHz clock)

Parameter	Symbol	Min	Max	Units
Send REQ/ or ACK/ assertion pulse width	t_1	35	-	ns
Send REQ/ or ACK/ deassertion pulse width	t_2	35	-	ns
Receive REQ/ or ACK/ assertion pulse width	t_1	20	-	ns
Receive REQ/ or ACK/ deassertion pulse width	t_2	20	-	ns
Send data setup to REQ/ or ACK/ asserted	t_3	33	-	ns
Send data hold from REQ/ or ACK/ asserted	t_4	40**	-	ns
Receive data setup to REQ/ or ACK/ asserted	t_5	0	-	ns
Receive data hold from REQ/ or ACK/ asserted	t_6	10	-	ns

**Transfer Period bits (bits 6-4 in the SXFER register) are set to zero and the extra Clock Cycle of Data Setup bit (bit 7 in SCNTL) is set.*

*** Analysis of system configuration is recommended due to reduced driver skew margin in differential systems.*

Note: for fast SCSI, the TolerANT Enable bit (STEST3 bit 7) should be set.