Floating-Point Multiplier and ALU

32-Bit, 10 Megaflops

The TMC3032 and TMC3033 are form, fit, and function compatible with the WTL1032 and WTL1033. Since the TMC3032 and TMC3033 are built using TRW's OMICRON-C™ one micron CMOS process, power consumption is greatly reduced. Power supply considerations are also eased by the requirement for only a single (+5V) supply voltage.

The TMC3032 is a digital multiplier which provides the product of two normalized floating point numbers. These numbers are expressed in the 32-bit single-precision format of the IEEE Standard 754, Version 8.0 or 10.0. When the three internal pipeline registers are enabled, the data throughput rate of the TMC3032-1 is 10 Megaflops (Million floating point operations per second). With the pipeline registers disabled, the TMC3032-1 runs at 3 Megaflops. The TMC3032 (like the WTL1032) operates from a single clock.

The TMC3033 is an arithmetic unit which adds, subtracts, and compares floating point numbers expressed in the 32-bit single-precision format of the IEEE Standard 754. It can also convert between floating point and a 24-bit two's complement integer fixed point representation. When the three internal pipeline registers are enabled, the data throughput rate of the TMC3033-1 is 10 Megaflops. With the pipeline registers disabled, the TMC3033-1 runs at 3 Megaflops. The TMC3033 (like the WTL1033) operates from a single clock.

All data and instruction inputs are registered. Each input operand enters on a half-width bus on two successive rising edges of the clock when enabled by the LOAD controls. The synchronous UNLOAD controls enable or disable the three-state output buffers and select the most or least significant output word.

Instruction and mode registers hold data format and rounding control signals. Renormalizing, rounding, and limiting logic ensure proper handling of special cases and correct output
data formatting.

Features

- Exact Replacements For WTL1032 And WTL1033
- Low-Power CMOS Construction, Single +5V Power Supply Operation
- 10 Megaflop Throughput Rate With The TMC3032-1 And TMC3033-1
- Six Additional Functional Instructions Over The WTL1033 (TMC3033)
- Complete IEEE Compare And Compare Magnitude Functions (TMC3033)
- Conforms To IEEE Standard 754 Version 8.0 Or 10.0
- Available In Commercial And Military Grades

Applications

- Matrix Operations And Geometric Transforms
- Arithmetic Section In Microprogrammed Array Processor
- Arithmetic Element In Systolic Processor
- Graphics And Image Processing
- Floating Point Digital Filters And FFTs
- Radar And Sonar Signal Processor
- Arithmetic Co-Processor
- Solids Modeling

J

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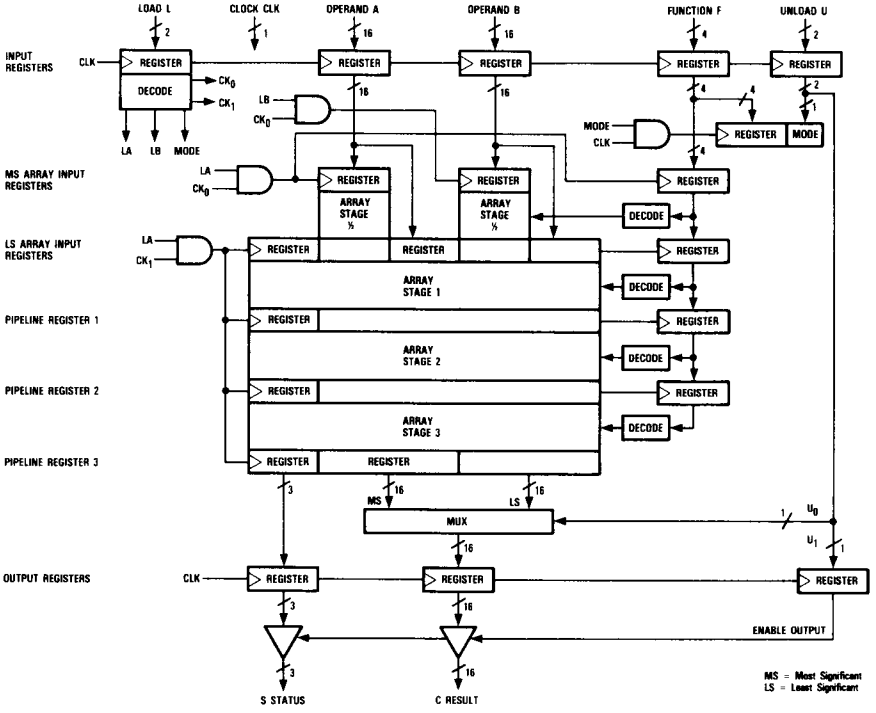
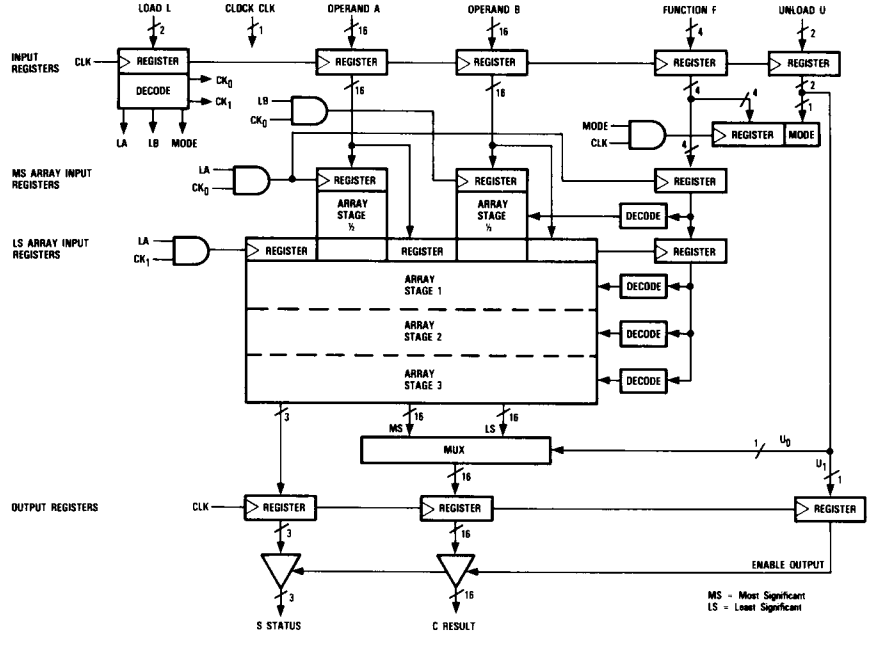
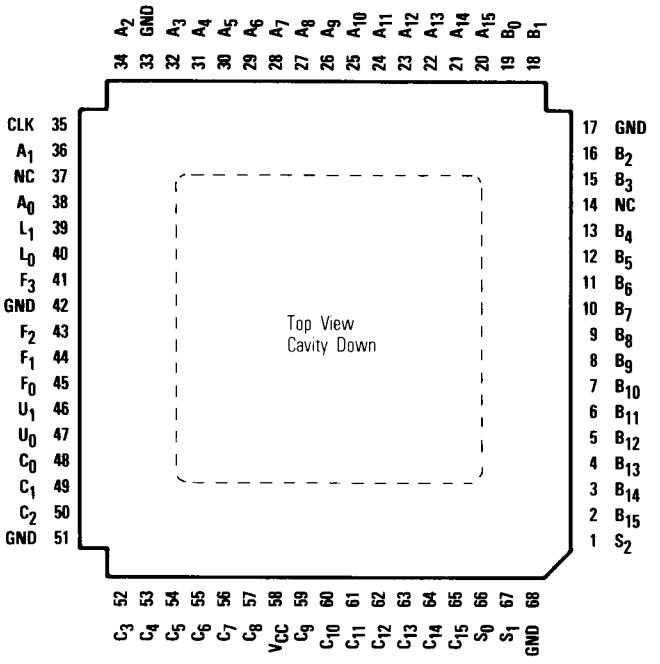
Block Diagram Pipeline Operation



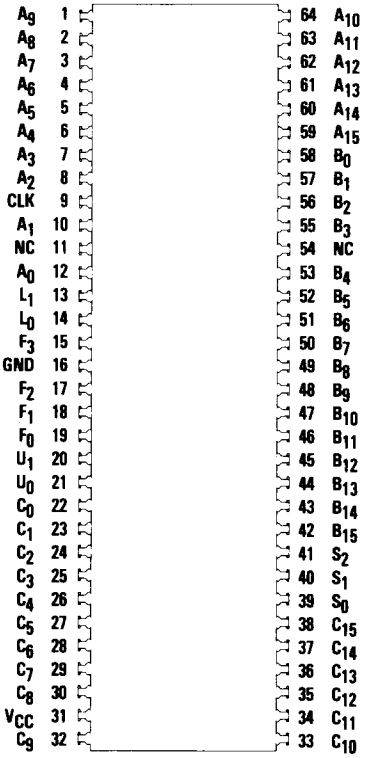
Block Diagram Flowthrough Operation



Pin Assignments



68 Contact Chip Carrier – A1 Package



64 Lead DIP – J3 Package

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Functional Description

TMC3032

The TMC3032 consists of four sections: the input stage, the significand multiplier/exponent adder, the renormalize/round/limit block and the output stage.

The input stage accepts instructions for loading data, unloading (outputting) data, and performing operations. It consists of five registers (L, A, B, F, and U) and control/sequencing logic to permit the controlled multiplexing of inputs to the proper destinations.

The multiplier/adder multiplies the significands and adds the exponents to produce a "raw" (possibly unnormalized) result.

If the significand emerging from the multiplier/adder overflows, the renormalizer right shifts the significand and increments the exponent. The rounder performs the selected rounding operation. The limiter replaces overflowing results with a properly signed infinity or maximum normalized value according to IEEE convention. In FAST mode, underflowing results are replaced with zero. In IEEE mode, they are output in wrapped format with the Underflow or Underflow/Inexact flag.

The output stage consists of registers which are loaded under the control of Unload Control U_0, and three-state output drivers which are enabled and disabled by Unload Control U_1.

TMC3033

The TMC3033 consists of five sections: the input stage, the denormalizer, the arithmetic unit, the renormalize/round/limit block and the output stage.

The input stage accepts instructions for loading data, unloading (outputting) data, and performing operations. It consists of five registers (L, A, B, F and U) and control/sequencing logic to permit the controlled multiplexing of inputs to the proper destinations.

The denormalizer shifts the smaller exponent's significand rightward. This section also executes the "UNWRAP A" and "FIX A" functions.

The arithmetic unit adds or subtracts the two significands.

The renormalize/round/limit block shifts the significand as required to produce the IEEE specified normalized or denormalized result. Rounding is then performed in this section. Finally, the results are limited according to IEEE conventions to eliminate overflow and improper handling of underflows.

The output stage consists of registers which are loaded by U_0, and three-state output drivers which are enabled and disabled by the U_1.

The TMC3033 arithmetic unit conforms to IEEE Standard 754, Version 8.0 or 10.0 data format for standard 32-bit arithmetic. The TMC3033 arithmetic unit needs two clock cycles to transfer any input or output data word, since the input and output buses are 16 bits wide.

Power

The TMC3032 and TMC3033 operate from a single +5 Volt supply. The TMC3032 and TMC3033 do not require a 3 Volt supply on the V_{DD} pins. These pins (11, 54) are not connected and permit operation in sockets wired for the WTL1032 and WTL1033.

Clock

The TMC3032 and TMC3033 operate on a single, TTL-compatible clock, CLK. All data are loaded into the appropriate registers on the rising edge of CLK as controlled by the LOAD, FUNCTION and UNLOAD commands.

Data Inputs

The TMC3032 and TMC3033 have two 16-bit multiplexed input data buses, A_{15-0} and B_{15-0}. The Most Significant Word (MSW) is loaded on the rising edge of CLK which follows the assertion of a LOAD instruction, LA or LAB. The Least Significant Word (LSW) is loaded on the next rising edge of CLK following the loading of the MSW. If the load instructions are not changed, consecutive rising edges of CLK will load alternating MSWs and LSWs continuously.

Data Outputs

The TMC3032 and TMC3033 have a single, 16-bit multiplexed output bus with three-state output drivers. The loading of the output register is controlled by the U_0 instruction. Three-state enable/disable is synchronous and is controlled by the U_1 instruction.

Controls

The load controls, L_0 and L_1, determine how data are transferred into the data input registers, A and B, and the mode control register. The load controls are read on every rising edge of CLK. All data transfers into the A, B and mode registers take place on the rising edge of CLK following the load controls commanding the data transfer. Since two consecutive clock cycles are required to load A or B operands into the data input registers, L_0 and L_1 must be valid for two consecutive clock cycles.

Unload control U_0 determines how data is transferred into the output registers. U_1 controls the enabling and disabling of the three-state output drivers. The unload controls are read on the rising edge of CLK. The state of the output drivers will change after the next rising edge of CLK following the loading of a DAB or ENB instruction on U_1. Therefore, two CLK cycles are required to enable or disable the three-state drivers.

The dual-purpose function controls F_{3-0} and U_0 select the operational mode (flow-through or pipeline), the rounding and underflow modes, and the input data formats (normalized or wrapped). The mode controls are read on the rising edge of CLK following an LMODE instruction.

Status Outputs

The TMC3032 and TMC3033 have three pins which indicate the presence of exception conditions in the result in the data output register. These flags are valid while both the MSW and the LSW are unloaded. Note that these pins are three-state under the control of the U_1 input. If the magnitude of a

TMC3033 result is smaller than the smallest normalized IEEE number, the TMC3033 produces a denormalized value (with a zero exponent). In the IEEE mode, when a TMC3032 product magnitude is smaller than the smallest normalized IEEE number, the TMC3032 produces a normalized but unrounded value with a (nonpositive) "wrapped" exponent. In this case, the UNF and UNF+INEX (underflow and underflow with inexact result) status flags can be applied to the TMC3033 along with the product to generate a properly rounded IEEE "gradual underflow" numerical representation. In FAST mode, underflowing products are flushed to zero with the UNF+INEX flag.

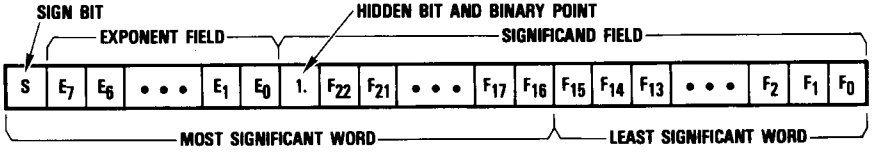
Instructions

Function codes 1010 binary through 1111 binary (listed as WTL1033 "Reserved" instructions) have been implemented as absolute value and IEEE Comparison instructions. Comparisons of infinities follow IEEE Standard 754 Version 8.0 for projective and affine modes. For IEEE Standard 754 Version 10.0, the affine infinity mode should be selected.

The FIX A instruction can be used with any user-selected type of rounding in the TMC3033, whereas the WTL1033 supports only round-toward-zero. When round-toward-zero is used, the WTL1033 and TMC3033 yield the same (correct) result.

Figure 1. Data Formats

32-bit floating point (IEEE Standard)

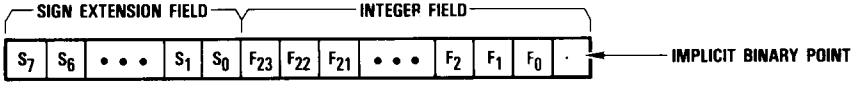


32-bit floating point values are determined by:

Exponent	Significand	Value	Name	Mnemonic
255	Not all zeros	-	Not a number	NaN
255	All zeros	$(-1)^S$	Infinity	INF
1-254	Any	$(-1)^S(1.F)2^{E-127}$	Normalized number	NRM
0	Not all zeros	$(-1)^S(0.F)2^{E-126}$	Denormalized number	DNRM
0	Zero	$(-1)^S(0.0)$	Zero	ZERO

Note: The F_{23} bit of the significand (hidden bit) is always one except for zero and denormalized numbers, when it is zero.

24-bit fixed point two's complement



Note: The 8-bit sign extension is a repeat of bit F_{23}, the sign bit of the two's complement representation. Values can range between $+2^{23}-1$ and -2^{23}.

Table 1. Load Instructions

L_{1-0}	Mnemonic	Operation
00	NOP	No loading of A, B or mode - Internal registers disabled
01	LAB	Load operands A & B into array from A & B registers
10	LA	Load only operand A into array from A register
11	LMODE	Load only MODE register from F and U registers

Table 2. Unload Instructions

U_{1-0}	Mnemonic	Operation
1X	DAB	Disable output driver (Hi-Z state)
0X	ENB	Enable output driver
X0	UMS	Load output register MSW from array
X1	ULS	Load output register LSW from array

Table 3. Mode Instructions

F_{3-0}	U_0	Mnemonic	Operation
XXXX	0	FLOW	Pipeline registers are disabled
XXXX	1	PIPE	Pipeline registers are enabled
XX00	X	RN	Round to nearest number, or nearest even number if distances are equal
XX01	X	RZ	Round toward zero (truncate product significand)
XX10	X	RP	Round toward positive infinity
XX11	X	RM	Round toward negative infinity
X0XX	X	AI	Affine infinity (sign preserved) IEEE Standard 754 Version 8.0 or 10.0
X1XX	X	PI	Projective infinity (sign ignored) IEEE Standard 754 Version 8.0
0XXX	X	IEEE	Gradual Underflow (use wrap for exponent underflow, TMC3032 only)
1XXX	X	FAST	Flush-to-zero (replace underflowing numbers with zero, TMC3032 only)

Table 4. TMC3032 Load Instructions

F_{3-0}	Mnemonic	Operation
0000	A x B	Multiply normalized A times normalized B
0001	WA x B	Multiply wrapped A times B
0010	A x WB	Multiply A times wrapped B
0011	WA x WB	Multiply wrapped A times wrapped B
01XX	-	Reserved
1XXX	-	Reserved

Table 5. Status Outputs

S_{2-0}	Mnemonic	Exceptions
000	OK	No exceptions
001	INEX	Inexact result
010	UNF	Exponent underflow
011	UNF+INEX	Exponent underflow and inexact result
100	-	Unused
101	OVF+INEX	Exponent overflow and inexact result
110	INV	Invalid operands or invalid operation
111	DIN	Denormalized operand, TMC3032

Table 6. TMC3033 Function Instructions

F_{3-0}	Mnemonic	Operation
0000	WRAP A	Convert a "gradual underflow" denormalized A operand (exponent zero) to normalized form with a negative (wrap-around) exponent. Used before multiplying a denormalized number.
0001	UNWRAP A	Convert a normalized A operand with a nonpositive (wrap-around) exponent to a denormalized number with a zero exponent. Used after an underflowing multiplication. The LSB of the B operand must contain the S_0 (inexact) bit from the multiplier STATUS word.
0010	FLOAT A	Convert a 24-bit two's complement integer at the A input to 32-bit normalized floating point.
0011	FIX A	Convert 32-bit normalized floating point number to 24-bit integer. All rounding modes usable.
0100	A+B	Add A and B in 32-bit floating point.
0101	A-B	Subtract B from A in 32-bit floating point.
0110	B-A	Subtract A from B in 32-bit floating point.
0111	(ABS A)+(ABS B)	Add the absolute values of A and B in 32-bit floating point.
1000	ABS (A-B)	Take the absolute value of the difference between A and B in 32-bit floating point.
1001	ABS (A+B)	Take the absolute value of the sum of A and B in 32-bit floating point.
1010	COMP A, B [1]	Compare A and B; result is A-B. Status flags indicate B > A, A=B, A > B.
1011	-A-B [1]	Subtract B from minus A, 32-bit floating point.
1100	COMP ABS A, ABS B [1]	Compare the absolute values of A and B; result is (ABS A)-(ABS B). Status flags indicate B > A, A=B, A > B.
1101	(ABS A)-(ABS B) [1]	Subtract the absolute value of B from the absolute value of A in 32-bit floating point.
1110	(ABS B)-(ABS A) [1]	Subtract the absolute value of A from the absolute value of B in 32-bit floating point.
1111	(-ABS A)-(ABS B) [1]	Subtract the absolute value of B from minus the absolute value of A 32-bit floating point.

Note:

1. These instructions are not implemented on the WTL1033 ALU device.

Table 7. TMC3033 Status Outputs for Comparison Operations

S_{2-0}	Mnemonic	Comparison Result
000	IOP	Invalid operation: one operand is not a number.
001	A > B	A operand greater than B operand.
010	A=B	A operand equal to B operand.
100	A < B	A operand less than B operand.

Table 8. Multiplication Exception Flags and Outputs

A Operand	B Operand				
	ZERO	DNRM	NRM/WNRM	INF	NaN
ZERO	OK, ZERO	OK, ZERO	OK, ZERO	INV, NaN	INV, NaN
DNRM	OK, ZERO	DIN [1], ZERO	DIN [1], ZERO	OK, INF	INV, NaN
NRM/WNRM	OK, ZERO	DIN [1], ZERO	See Note 2	OK, INF	INV, NaN
INF	INV, NaN	OK, INF	OK, INF	OK, INF	INV, NaN
NaN	INV, NaN	INV, NaN	INV, NaN	INV, NaN	INV, NaN

Notes: 1. In FAST mode, DIN becomes OK.

2. In the case of NRM.WNRM x NRM.WNRM:

OVF: Output is OVF, -NRM.MAX if (RM,RZ) and (TRESULT > NRM.MAX
OVF, -NRM.MAX if (RP,RZ) and (TRESULT < -NRM.MAX
OVF, -INF if (RN,RP) and (TRESULT > NRM.MAX
OVF, INF if (RN,RM) and (TRESULT < -NRM.MAX

UNF: Output is zero with UNF or UNF.INEX if (TRESULT < NRM.MIN (FAST mode)
Output is WNRM with UNF or UNF.INEX if (TRESULT < NRM.MIN (IEEE mode)

ELSE: Output is OK or INEX with normalized value
NRM.MIN ≤ |TRESULT| ≤ NRM.MAX

3. Terms used in this table include:

OK = No exceptions raised
NRM = Normalized number.
DNRM = Denormalized number
WNRM = Wrapped number.
INEX = Inexact result, output differs from infinite precision value.
TRESULT = Normalized, rounded, true result before limiting
NRM.MAX = Maximum allowable positive normalized number, $2-128-2-104$
NRM.MIN = Minimum allowable positive normalized number, 2^{-126}

Table 9. Conversion of 32-bit Floating Point to 24-bit Fixed Point

32-Bit Floating Point Operand	24-Bit Result	Status
$+1.XXX...XXX \times 2^{+128}$ (NaN OR INF)	0111...111	OVF
•	•	•
•	•	•
•	•	•
$+1.XXX...XXX \times 2^{+23}$	0111...111	OVF
$+1.111...111 \times 2^{+22}$	0111...111	INEX
$+1.111...110 \times 2^{+22}$	0111...111	OK
•	•	•
•	•	•
•	•	•
$+1.000...000 \times 2^{0}$	000...0001	OK
•	•	•
•	•	•
•	•	•
$+1.000...000 \times 2^{-126}$	000...0000	INEX
•	•	•
•	•	•
•	•	•
$+0.000...001 \times 2^{-126}$ (DNRM)	000...0000	INEX
$+0.000...000 \times 2^{-126}$ (ZERO)	000...0000	OK
$-0.000...000 \times 2^{-126}$ (ZERO)	000...0000	OK
•	•	•
•	•	•
•	•	•
$-0.111...111 \times 2^{-126}$ (DNRM)	000...0000	INEX
$-1.000...000 \times 2^{-126}$	000...0000	INEX
•	•	•
•	•	•
•	•	•
$-1.000...000 \times 2^{0}$	1111...111	OK
•	•	•
•	•	•
•	•	•
$-1.111...110 \times 2^{+22}$	1000...001	OK
$-1.111...111 \times 2^{+22}$	1000...001	INEX
$-1.000...000 \times 2^{+23}$ Note 1	1000...000	OVF
•	•	•
•	•	•
•	•	•
$-1.000...010 \times 2^{+23}$	1000...000	OVF
$-1.XXX...XXX \times 2^{+128}$ (NaN or INF)	1000...000	OVF

Note:

1. The indicated operation causes the OVF flag but is actually OK.

DNRM and WNRM represent numbers in which the fraction is normalized and the exponent is allowed to wrap through the biased exponent value of zero.

The multiplier accepts wrapped inputs from the ALU over the WNRM range. The smallest positive WNRM is $2^{-126} \times 2^{-23} = 2^{-149}$. The multiplier outputs wrapped numbers over the DNRM range. The smallest positive result is $2^{-149} \times 2^{-149} = 2^{-298}$.

Table 10. DNRM and WNRM Floating Point Numbers (IEEE Mode)

Exponent	Biased Value	Unbiased Value
0	0	-127
255	-1	-128
•	•	•
•	•	•
•	•	•
234	-22	149
232	-23	150
•	•	•
•	•	•
•	•	•
85	-171	-298

WNRM

DNRM

Package Interconnections

Signal Type	Signal Name	Function	J3 Package	A1 Package
Power	V_{CC}	Positive Supply Voltage	31	58
Ground	GND	Ground	16	17, 33, 42, 51, 68
Data Inputs	A_{15-0}	A Operand Input Bus	59-64, 1-8, 10, 12	20-32, 34, 36, 38
	B_{15-0}	B Operand Input Bus	42-53, 55-58	2-13, 15, 16, 18, 19
Data Outputs	C_{15-0}	Result Output Bus	38-32, 30-22	65-59, 57-52, 50-48
Clock	CLK	Timing Reference	9	35
Controls	L_{1-0}	Load Instructions	13, 14	39, 40
	U_{1-0}	Unload Instructions	20, 21	46, 47
	F_{3-0}	Mode/Format Select	15, 17-19	41, 43-45
Flags	S_{2-0}	Status Outputs	41-39	1, 67, 66
No Connection	NC	None	11, 54	14, 37

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Figure 2. Input and Output Timing

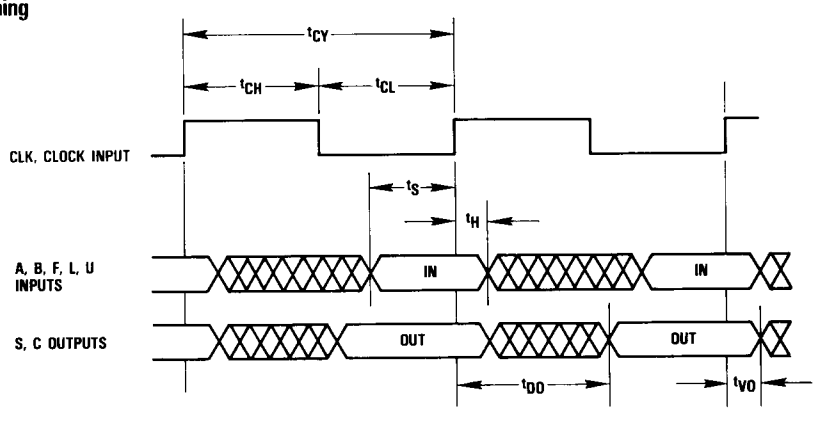


Figure 3. Flowthrough Mode Timing

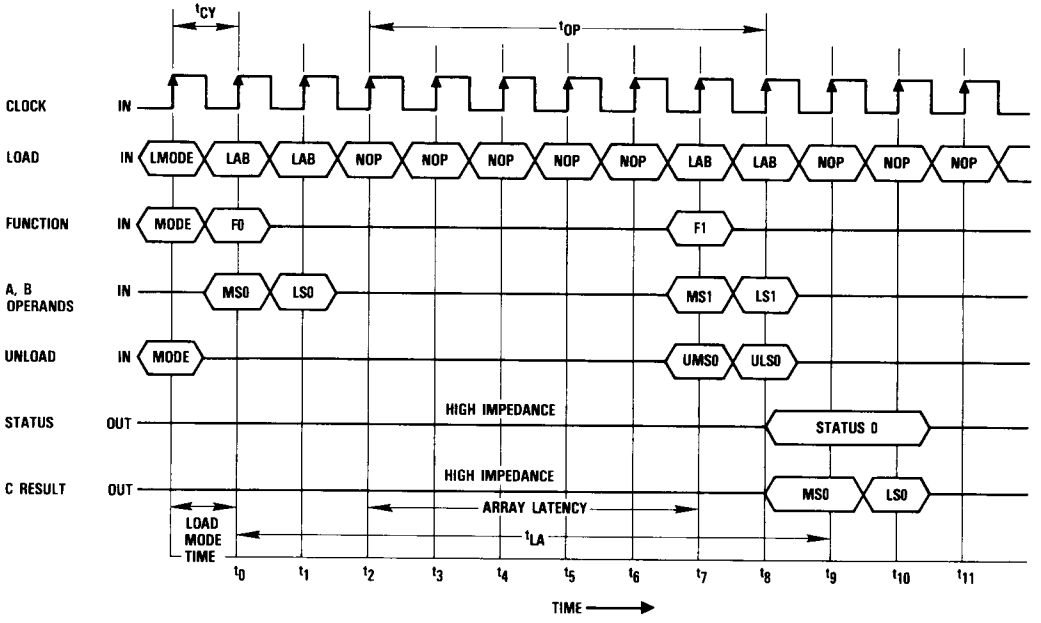


Figure 4. Pipeline Mode Timing

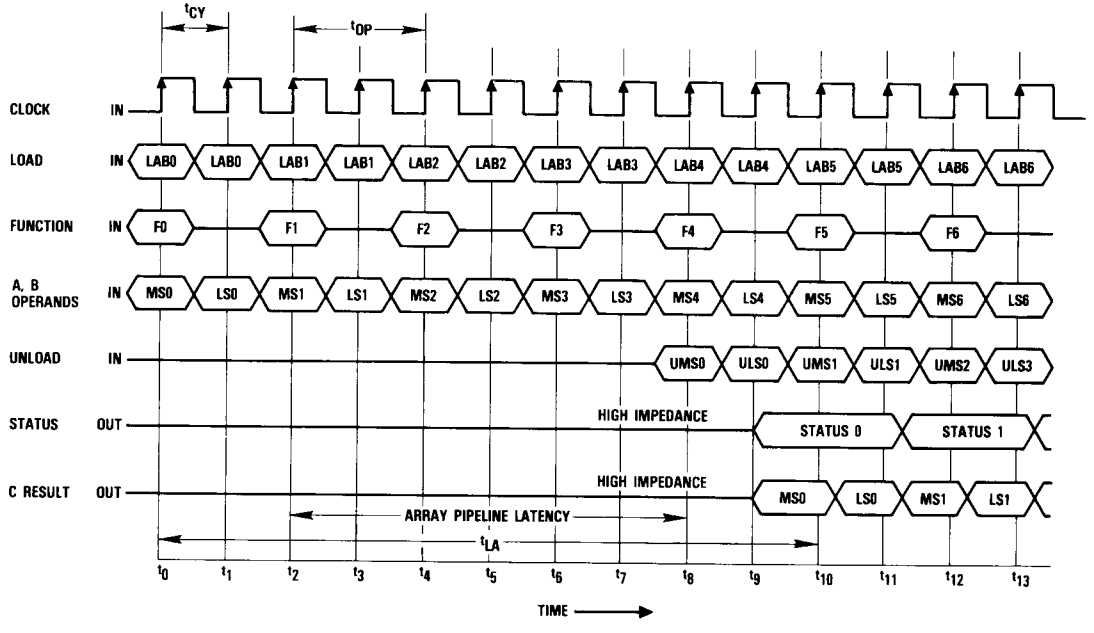


Figure 5. Equivalent Input Circuit

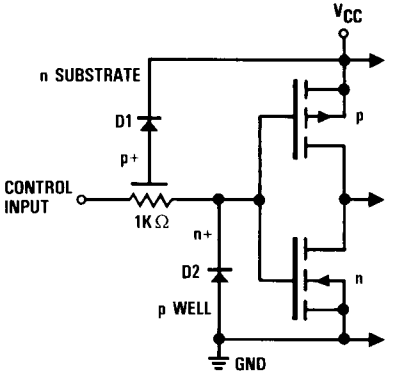
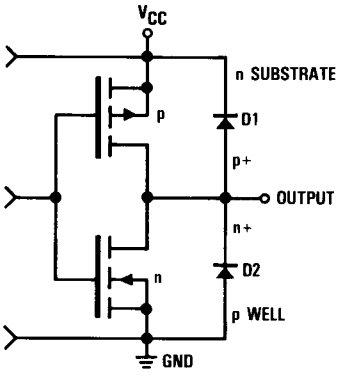


Figure 6. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{CC} + 5.5V)

Output

Applied voltage ..... −0.5 to +5.5V [2]

Forced current ..... −1.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −55 to 125°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if the Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Military Min	Military Nom	Military Max	Units
V_{CC}	Supply Voltage	4.75	5.0	5.25	4.50	5.0	5.5	V
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

DC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range								Units
			Standard				Military [2]				
			3032/3033		3032-1/3033-1		3032		3033		
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		2.5		2.5		V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8		0.8		0.8	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC}=Min, I_{OH}=−2mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output Voltage, Logic LOW	V_{CC}=Min, I_{OL}=4mA		0.4		0.4		0.5		0.5	V
I_{LI}	Input Leakage Current	V_{CC}=Max, V_{IN}=0 to 5V		10		10		10		10	μA
I_{LO}	Output Leakage Current (Outputs Disabled)	V_{CC}=Max, V_{OUT}=0 to 5V		40		40		40		40	μA
C_{IN}	Input Capacitance	V_{CC}=Max, V_{IN}=0 to 5V		15		15		15		15	pF
C_{OUT}	Output Capacitance (Outputs Disabled)	V_{CC}=Max, V_{IN}=0 to 5V		15		15		15		15	pF
I_{CCQ}	Supply Current, Quiescent	V_{CC}=Max, V_{IN}=0V		10		10		10		10	mA
I_{CCU}	Supply Current, Unloaded	V_{CC}=Max, f=10MHz		40		40		50		40	mA

Notes: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Contact factory for final values.

AC characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range								Units
			Standard				Military [2]				
			3032/3033		3032-1/3033-1		3032		3033		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CY}	Clock Cycle Time	V_{CC}=Min	62.5		50		60		60		ns
t_{CH}	Clock HIGH Time	V_{IH}=2.4V	30		20		25		25		ns
t_{CL}	Clock LOW Time	V_{IL}=0.8V	30		20		25		25		ns
t_S	Input Setup Time	V_{OH}=2.8V, I_{OH}=−1mA	25		15		25		25		ns
t_H	Input Hold Time	V_{OL}=0.4V, I_{OL}=5mA	0		0		2		2		ns
t_{DO}	Output Delay Time	C_{LOAD}=50pF		35		35		40		40	ns
t_{VO}	Output Valid Time	See Figure 2	10		10		8		8		ns
t_{OP}	Flowthrough Operation Time	See Figure 3		375		300		360		360	ns
t_{LA}	Total Flowthrough Latency			565		450		540		540	ns
t_{OP}	Pipelined Time Per Stage	See Figure 4		125		100		120		120	ns
t_{LA}	Total Pipeline Latency			625		500		600		600	ns

Notes: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Contact factory for final values.

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC3032J3C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3032J3C
TMC3032J3C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3032J3C1
TMC3032J3V[1]	MIL – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	3032J3V
TMC3033J3C	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3033J3C
TMC3033J3C1	STD – T_A = 0°C to 70°C	Commercial	64 Pin Hermetic Ceramic DIP	3033J3C1
TMC3033J3V[1]	MIL – T_C = –55°C to 125°C	MIL-STD-883	64 Pin Hermetic Ceramic DIP	3033J3V
TMC3032A1C	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3032A1C
TMC3032A1C1	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3032A1C1
TMC3033A1C	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3033A1C
TMC3033A1C1	STD – T_A = 0°C to 70°C	Commercial	68 Contact Chip Carrier	3033A1C1

Note: 1. Contact factory for availability.

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