

DESCRIPTION

The HYM7V64400/ 64401/ 64430/ 64431 Q-Series are high speed 3.3-Volt synchronous dynamic RAM Modules composed of four 4Mx16 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit E²PROM on a 144-pin Zig Zag Dual pin glass-epoxy printed circuit board. Two 0.22 μ F and two 0.0022 μ F decoupling capacitors per each SDRAM are mounted on the module.

The HYM7V64400/ 64401/ 64430/ 64431 Q-Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 32M bytes memory. All addresses, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipelined to achieve very high bandwidths.

FEATURES

- 144-Pin Unbuffered SO DIMM
- Serial Presence Detect with Serial E²PROM
- Meets all the other JEDEC specifications
- Single 3.3V \pm 0.3V power supply
- All device pins are LVTTTL compatible
- 4096 refresh cycles every 64ms or 8192 refresh cycles every 128ms
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Dual or Quad internal banks with single pulsed /RAS
- Auto precharge/precharge all banks by A10 flag
- Possible to assert random column address every clock cycle
- Interleaved auto refresh mode
- Programmable burst lengths and sequences
 - 1,2,4,8,full page for Sequential type
 - 1,2,4,8 for Interleave type
- Programmable /CAS latency ; 1,2,3 clocks
- Support clock suspend/power down mode by CKE0
- Data mask function by DQM
- Mode register set programming
- Burst termination command
- Self refresh provides minimum power, full internal refresh control

ORDERING INFORMATION

Part No.	Max. Frequency	SDRAM Bank	Refresh	Package	Plating
HYM7V64400TQG - 10/12/15	100/ 83/ 66 MHz	2 Banks	4K	TSOP	Gold
HYM7V64401TQG - 10/12/15	100/ 83/ 66 MHz	4 Banks	4K	TSOP	Gold
HYM7V64430TQG - 10/12/15	100/ 83/ 66 MHz	2 Banks	8K	TSOP	Gold
HYM7V64431TQG - 10/12/15	100/ 83/ 66 MHz	4 Banks	8K	TSOP	Gold

PIN DESCRIPTION

Pin Name	Pin Type	Description
CK0, CK1	INPUT	System Clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
CKE0	INPUT	Clock Enable; Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
/S0	INPUT	Chip select; Functions command mask(NOP).
/RAS	INPUT	Row address strobe; See functional truth table in 4Mx16 Data Sheets for details.
/CAS	INPUT	Column address strobe; See functional truth table in 4Mx16 Data Sheets for details.
/WE	INPUT	Write Enable; See functional truth table in 4Mx16 Data Sheets for details.
DQM0-7	INPUT	Data Input / Output Mask
DQ0-DQ63	INPUT/ OUTPUT	Data Input / Output; Include inputs, outputs, or Hi-z state.
Vcc	SUPPLY	Power Supplies; 3.3V±0.3V
Vss	SUPPLY	Ground
SDA	INPUT/ OUTPUT	Serial Address and Data Input / Output.
SCL	INPUT	Serial Clock

HYM7V64400/HYM7V64430 Q-Series (2Bank 4Mx16 SDRAM Based)

Pin Name	Pin Type	Description
BA0	INPUT	Bank select address inputs; Select one of dual banks during both /RAS and /CAS activity.
A0-A12	INPUT	Address Inputs; A0-A7; X&Y addresses, A0-A13; Opcode for mode register set, A10; Precharge flag, A8-A12; X addresses only.

HYM7V64401/HYM7V64431 Q-Series (4Bank 4Mx16 SDRAM Based)

Pin Name	Pin Type	Description
BA0, BA1	INPUT	Bank address inputs; Select one of quad banks during both /RAS and /CAS activity.
A0-A11	INPUT	Address Inputs; A0-A7; X&Y addresses, A0-A13; Opcode for mode register set, A10; Precharge flag, A8-A11; X addresses only.

4MX64 BIT SDRAM SO DIMM Q-SERIES

based on 4Mx16 SDRAM, LVTTTL, 2/4-Banks & 4K/BK-Refresh
HYM7V64400/ HYM7V64401/ HYM7V64430/ HYM7V64431

I-1 SERIAL PRESENCE DETECT

[HYM7V64400/HYM7V64430 Q-Series; 2 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	2 Banks; 13	0Dh	1
BYTE4	# of Column Addresses on This Assembly	8	08h	
BYTE5	# of Module Banks on This Assembly	1 Bank	01h	
BYTE6	Data Width of This Assembly	64 Bits	40h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	tCLK (A) 10ns (B) 12ns (C) 15ns	(A) A0h (B) C0h (C) F0h	3
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, @Cycle Time=10ns @ /CAS Latency=3, @Cycle Time=12ns @ /CAS Latency=3, @Cycle Time=15ns	tAC (A) 8ns (B) 9ns (C) 10ns	(A) 80h (B) 90h (C) A0h	3
BYTE11	DIMM Configuration Type	None	00h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x16	10h	
BYTE14	Error Checking SDRAM Width	None	00h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 Latency	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device 2 Bank 4Mx16 Based	2 Banks	02h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Neither Buffered nor Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Precharge All, Auto Precharge)	-	06h	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	tCLK (A) 12ns (B) 15ns (C) 15ns	(A) C0h (B) F0h (C) F0h	3

I-2 SERIAL PRESENCE DETECT

[HYM7V64400/HYM7V64430 Q-Series; 2 Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE24	SDRAM Access Time from Clock @ /CAS Latency=2, @Cycle Time=12ns @ /CAS Latency=2, @Cycle Time=15ns @ /CAS Latency=2, @Cycle Time=15ns	tAC (A) 9ns (B) 9ns (C) 10ns	(A) 90h (B) 90h (C) A0h	3
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	tCLK (A) 30ns (B) 30ns (C) 30ns	(A) 78h (B) 78h (C) 78h	3
BYTE26	SDRAM Access Time from Clock @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns	tAC (A) 24ns (B) 24ns (C) 24ns	(A) 60h (B) 60h (C) 60h	3
BYTE27	Minimum Row Pre-charge Time @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRP (A) 30ns (B) 36ns (C) 45ns	(A) 1Eh (B) 24h (C) 2Dh	3
BYTE28	Minimum Row Active to Row Active Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRRD (A) 30ns (B) 24ns (C) 30ns	(A) 1Eh (B) 18h (C) 1Eh	3
BYTE29	Minimum /RAS to /CAS Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRCD (A) 30ns (B) 36ns (C) 45ns	(A) 1Eh (B) 24h (C) 2Dh	3
BYTE30	Minimum /RAS Pulse width @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRAS (A) 50ns (B) 48ns (C) 45ns	(A) 32h (B) 30h (C) 2Dh	3
BYTE31	Module Bank Density	32MB	08h	
BYTE32-61	Superset Information (May Be Used in the Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62 @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	(A) Decimal 241 (B) Decimal 85 (C) Decimal 186	(A) F1h (B) 55h (C) BAh	3
BYTE64-127	Manufacturer Information	-	-	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

- Note : 1. The bank address is excluded.
 2. In interleaved type, the burst lengths supported is 1,2,4,8.
 3. In case of (A): 10ns, (B): 12ns, and (C): 15ns part.
 * All above data can be changed, if the JEDEC standard is modified.

4MX64 BIT SDRAM SO DIMM Q-SERIES

based on 4Mx16 SDRAM, LVTTTL, 2/4-Banks & 4K/8K-Refresh
HYM7V64400/ HYM7V64401/ HYM7V64430/ HYM7V64431

II-1 SERIAL PRESENCE DETECT

[HYM7V64401/HYM7V64431 Q-Series; 4 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	4 Banks; 12	0Ch	1
BYTE4	# of Column Addresses on This Assembly	8	08h	
BYTE5	# of Module Banks on This Assembly	1 Bank	01h	
BYTE6	Data Width of This Assembly	64 Bits	40h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	tCLK (A) 10ns (B) 12ns (C) 15ns	(A) A0h (B) C0h (C) F0h	3
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, @Cycle Time=10ns @ /CAS Latency=3, @Cycle Time=12ns @ /CAS Latency=3, @Cycle Time=15ns	tAC (A) 8ns (B) 9ns (C) 10ns	(A) 80h (B) 90h (C) A0h	3
BYTE11	DIMM Configuration Type	None	00h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x16	10h	
BYTE14	Error Checking SDRAM Width	None	00h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 Latency	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device 4 Bank 4Mx16 Based	4 Banks	04h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Neither Buffered nor Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Precharge All, Auto Precharge)	-	06h	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	tCLK (A) 12ns (B) 15ns (C) 15ns	(A) C0h (B) F0h (C) F0h	3

II-2 SERIAL PRESENCE DETECT

[HYM7V64401/HYM7V64431 Q-Series; 4 Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE24	SDRAM Access Time from Clock @ /CAS Latency=2, @Cycle Time=12ns @ /CAS Latency=2, @Cycle Time=15ns @ /CAS Latency=2, @Cycle Time=15ns	tAC (A) 9ns (B) 9ns (C) 10ns	(A) 90h (B) 90h (C) A0h	3
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	tCLK (A) 30ns (B) 30ns (C) 30ns	(A) 78h (B) 78h (C) 78h	3
BYTE26	SDRAM Access Time from Clock @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns	tAC (A) 24ns (B) 24ns (C) 24ns	(A) 60h (B) 60h (C) 60h	3
BYTE27	Minimum Row Pre-charge Time @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRP (A) 30ns (B) 36ns (C) 45ns	(A) 1Eh (B) 24h (C) 2Dh	3
BYTE28	Minimum Row Active to Row Active Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRRD (A) 30ns (B) 24ns (C) 30ns	(A) 1Eh (B) 18h (C) 1Eh	3
BYTE29	Minimum /RAS to /CAS Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRCD (A) 30ns (B) 36ns (C) 45ns	(A) 1Eh (B) 24h (C) 2Dh	3
BYTE30	Minimum /RAS Pulse width @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRAS (A) 50ns (B) 48ns (C) 45ns	(A) 32h (B) 30h (C) 2Dh	3
BYTE31	Module Bank Density	32MB	08h	
BYTE32-61	Superset Information (May Be Used in the Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62 @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	(A) Decimal 242 (B) Decimal 86 (C) Decimal 187	(A) F2h (B) 56h (C) BBh	3
BYTE64-127	Manufacturer Information	-	-	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

- Note : 1. The bank address is excluded.
 2. In interleaved type, the burst lengths supported is 1,2,4,8.
 3. In case of (A): 10ns, (B): 12ns, and (C): 15ns part.
 * All above data can be changed, if the JEDEC standard is modified.

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based on 4Mx16 SDRAM, LVTTTL, 2/4-Banks & 4K/8K-Refresh
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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 125	°C
VIN, VOUT	Voltage on Any Pin relative to Vss	-1.0 to 4.6	V
VCC	Voltage on VCC relative to Vss	-1.0 to 4.6	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	4	W
TSOLDER	Soldering Temperature-Time	260-10	°C-sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(TA=0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
VCC	Power Supply Voltage	3.0	3.3	3.6	V	
Vss	Power Supply Voltage	0	0	0	V	
VIH	Input High Voltage	2.0	-	VCC + 0.4	V	LVTTTL
VIL	Input Low Voltage	-0.3	-	0.8	V	LVTTTL

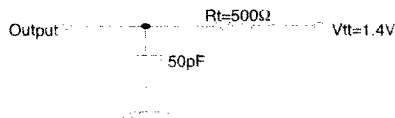
RECOMMENDED AC OPERATING CONDITIONS*

(TA=0°C to 70°C, VCC=3.3V±10%, Vss=0V)

Symbol	Parameter	Value	Unit	Note
VIH / VIL	AC Input High/Low Level Voltage	2.4/0.4	V	LVTTTL
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V	LVTTTL
tr / tf	Input Rise/Fall Time	1	ns	
Voutref	Output Reference Voltage	1.4	V	LVTTTL
CL	Output Load Capacitance for Access Time Measurement	Note	pF	

Note : Output load to measure access times is equivalent to two TTL gates and one capacitance(50pF).

Note : * DC Output Load Circuit



AC Output Load Circuit



(TA=0 °C to 70 °C, VCC=3.3V±10%, VSS=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Note
ILI	Input Leakage Current	VI=0 to 3.6V, All other pins not undertest=0V	-4	4	μA	
ILO	Output Leakage Current	DOUT is disabled, VO=0 to 3.6V	-1	1	μA	
VOL	Output Low Voltage	IO=2.0mA	-	0.4	V	LVTTTL
VOH	Output High Voltage	IO=-2.0mA	2.4	-	V	LVTTTL

DC CHARACTERISTICS II

(TA=0 °C to 70 °C, VCC=3.3V±10%, VSS=0V)

Symbol	Parameter	Test Condition	Max.	Unit	Note	
ICC1	Operating current	Burst Length=1, One bank active tRAS≥tRAS(min), tRP≥tRP(min), IO=0mA	10ns	340	mA	Note 2
			12ns	280		
			15ns	240		
ICC2P	Precharge Standby Current in Power Down Mode	CKE≤VIL(max)	8	mA		
ICC2N	Precharge Standby Current in Non Power Down Mode	CKE≥VIH(min), All other pins≥VCC-0.2V or ≤0.2V	48	mA	LVTTTL ¹	
ICC3P	Active Standby Current in Power Down Mode	CKE≤VIL(max), All banks active	12	mA		
ICC3N	Active Standby Current in Non Power Down Mode	CKE≥VIH(min), All other pins≥VCC-0.2V or ≤0.2V All banks active	140	mA	LVTTTL ¹	
ICC4	Operating Current (Burst Mode)	tCLK≥tCLK(min), tRAS≥tRAS(min), IO=0mA, /CAS Latency=3	10ns	600	mA	Note 2
			12ns	480		
			15ns	400		
ICC5	Refresh Current	tRC≥tRC(min), Two banks active (8K/128ms)	10ns	440	mA	Note 2
			12ns	360		
			15ns	300		
		tRC≥tRC(min), Four banks active (4K/64ms)	10ns	640	mA	Note 2
			12ns	520		
			15ns	420		
ICC6	Self Refresh Current	CKE≤0.2V	8	mA		

Note :

1. It depends on the number of each pin's transition. It is assumed there is no transition to measure this current.
2. ICC1 depends on output loads and cycle rates. Specified values are obtained with the output open. In addition this ICC1 is measured on condition that addresses are changed only one time during tCLK(Min.)

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AC CHARACTERISTICS

Synchronous Characteristics I

Parameter	100MHz (10ns)			83MHz (12ns)			66MHz (15ns)			Unit
/CAS Latency	3	2	1	3	2	1	3	2	1	Latency
Frequency	100	83	33	83	66	33	66	66	33	MHz
Clock Cycle Time	10	12	30	12	15	30	15	15	30	ns
tRCD	3	2	1	3	2	1	3	2	1	CLK(s)
tRAS	5	4	2	4	4	2	3	4	2	CLK(s)
tRP	3	3	1	3	2	1	3	2	1	CLK(s)
tRC	8	7	3	7	6	3	-	6	3	CLK(s)
tRRD	3	2	1	2	2	2	2	2	2	CLK(s)
tDPL	1	1	1	1	1	1	-	1	1	CLK(s)
tDAL	4	3	2	3	3	2	-	3	2	CLK(s)
tSRE	1	1	1	1	1	1	-	1	1	CLK(s)
tT	1			1			1			ns
Refresh Cycle	8K/128ms, 4K/64ms									Cycles
Asynchronous Characteristic	50ns Part									ns

Note : tRRD -Bank Active to Active Command
tDPL -DIN to Precharge Command
tDAL -DIN to Active(Ref.) Command (After Write with Autoprecharge)
tSRE -Self Refresh Exit Time

Synchronous Characteristics II

Symbol	Parameter	-10		-12		-15		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tAC	Access Time from CLK	/CAS Lat.=3	-	8	-	9	-	10	ns
		/CAS Lat.=2	-	9	-	9	-	10	ns
		/CAS Lat.=1	-	24	-	24	-	24	ns
tCH	CLK High Level Width	3.5	-	3.5	-	3.5	-	ns	
tCL	CLK Low Level Width	3.5	-	3.5	-	3.5	-	ns	
tOH	Data-out Hold Time	3	-	3	-	3	-	ns	
tOLZ	Data-out Low-Impedance Time	3	-	3	-	3	-	ns	
tOHZ	Data-out High-Impedance Time	0	8	0	9	0	10	ns	
tDS	Data-in Set-up Time	3	-	3	-	3	-	ns	
tDH	Data-in Hold Time	1	-	1	-	1	-	ns	
tAS	Address Set-up Time	3	-	3	-	3	-	ns	
tAH	Address Hold Time	1	-	1	-	1	-	ns	
tCKS	CKE Set-up Time	3	-	3	-	3	-	ns	
tCKH	CKE Hold Time	1	-	1	-	1	-	ns	
tCS	Command Set-up Time	3	-	3	-	3	-	ns	
tCH	Command Hold Time	1	-	1	-	1	-	ns	
tPDE	Power Down Exit Set-up Time	3	-	3	-	3	-	ns	

Latency

Symbol	Parameter	Latency	
tCKED	CKE to CLK Suspend / Power Down Mode Entry	1	
tDQMOZ	DQM to Data Output in Hi-z	2	
tDQMIM	DQM to Data Input Mask	0	
tWTL	Write Command to Data Input Valid	0	
tPROZ	Precharge Command to Data Output in Hi-z	/CAS Latency=1	1
		/CAS Latency=2	2
		/CAS Latency=3	3
tMRD	Mode Register Set to New Command	1	
tCCD	Min. Column Address to Column Address Delay	1	
tPPD	Min. Precharge to Precharge Time	1	

Note :

1. All voltages referenced Vss(Ground).
2. An initial pause of 100µS is required after power-on followed by Power On Sequence & Auto Refresh before proper device operation is achieved.
3. AC measurements assume $t_r=1ns$.
4. Reference level for measuring timing of input signals is 1.40V for LVTTL
Transition times are measured between V_{IH} and V_{IL} .
5. An access time is measured at 1.40V for LVTTL

CAPACITANCE

($T_A=25^\circ C$, $f=1MHz$)

Symbol	Parameter	Pin	Typ.	Max.	Unit
CIN1	Input Capacitance	A0-A11/12, BA0/BA1	-	40	pF
CIN2	Input Capacitance	/RAS, /CAS, /WE	-	40	pF
CIN3	Input Capacitance	/S0	-	40	pF
CIN4	Input Capacitance	CK0	-	40	pF
CIN5	Input Capacitance	CKE0	-	40	pF
CIN6	Input Capacitance	DQM0-DQM7	-	15	pF
COUT	Output Capacitance	DQ0-DQ63	-	15	pF

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PROGRAMMABLE MODE REGISTER

MODE REGISTER SET(WRITE)

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	/CAS Latency			BT	Burst Length		

A3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round)

A6	A5	A4	/CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full page ¹

Note : 1. Full page burst supports only sequential type.

TEST MODE

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
0	0	0	0	1	X	X	X	X	X	X	X	Refresh Counter Test

Note : Test Mode - Used to test the counter of Auto Refresh.
- Exit test mode using 'Precharge All banks'.

SDRAM Controller (M17) (M18)

BURST LENGTH AND SEQUENCE

Burst Length	Initial Address	Burst Type	
	A2 A1 A0	Sequential	Interleave
2	X X 0	0,1	0,1
	X X 1	1,0	1,0
4	X 0 0	0,1,2,3	0,1,2,3
	X 0 1	1,2,3,0	1,0,3,2
	X 1 0	2,3,0,1	2,3,0,1
	X 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Full page	Note	0,1,2,3,4, ..., m 1,2,3,4,5, ..., 0 ⋮ m,0,1,2,3, ..., m-1	Not supported

Table 1. Address sequence for different burst lengths

Note : 2Mbit x 2banks x 16i/O - Initial addresses: A7-A0, Page length: 1024, m=1023
 1Mbit x 4banks x 16i/O - Initial addresses: A7-A0, Page length: 1024, m=1023

