

# 64K x 32 3.3V Static RAM Module

## Features

- High-density 3.3V 2-megabit SRAM module
- High-speed SRAMs
  - Access time of 12 ns
- Low active power
  - 1.512W (max.) at 12 ns
- 64 pins
- Available in ZIP format

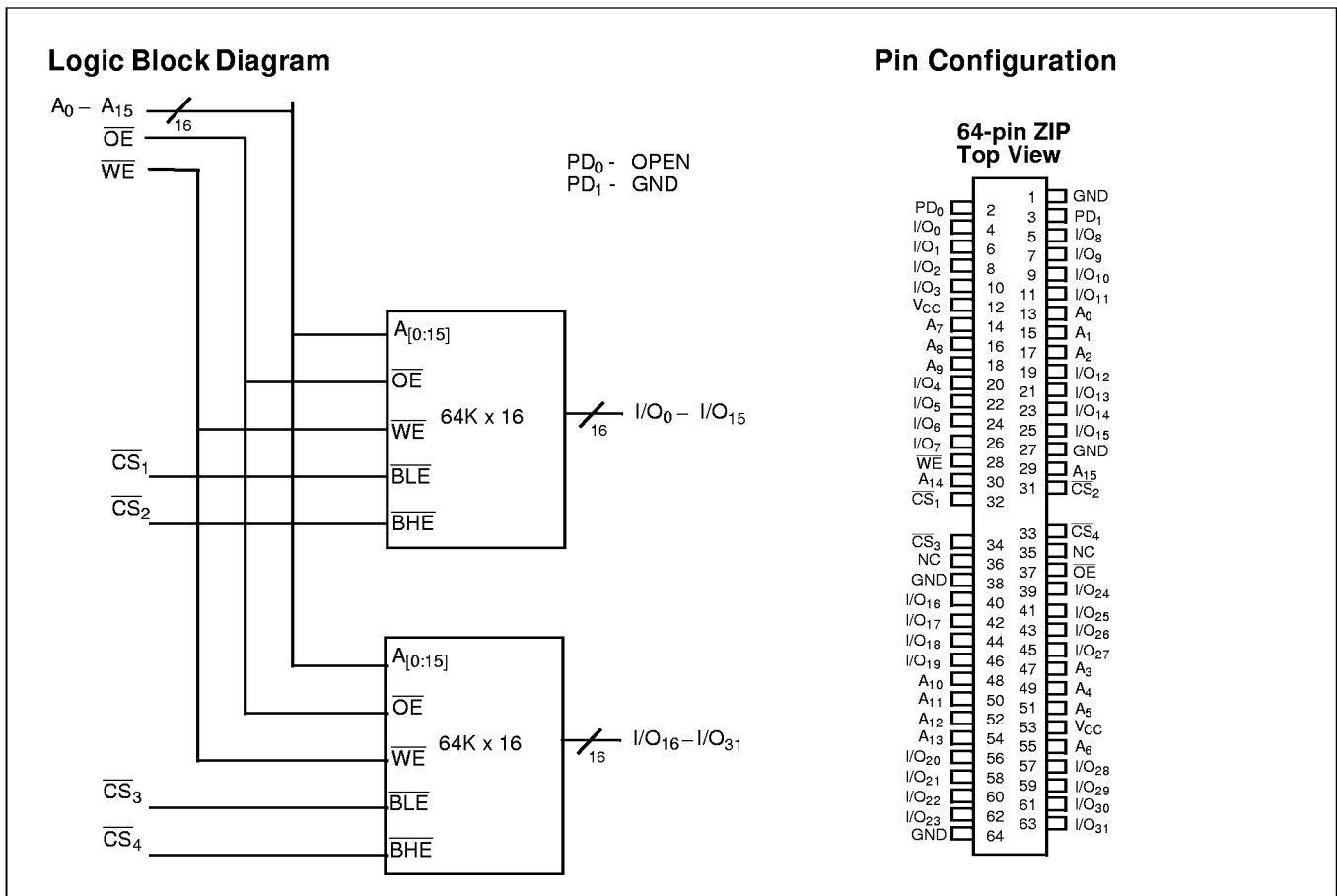
## Functional Description

The CYM1831V33 is a high-performance 3.3V 2-megabit static RAM module organized as 64K words by 32 bits. This mod-

ule is constructed from two 64K x 16 SRAMs in SOJ packages mounted on an epoxy laminate substrate. Four chip selects are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The CYM1831V33 is designed for use with standard 64-pin ZIP sockets. The pinout is compatible with the 64-pin JEDEC ZIP module family (CYM1821, CYM1831, CYM1836, and CYM1841). Thus, a single motherboard design can be used to accommodate memory depth ranging from 16K words (CYM1821) to 256K words (CYM1841). The CYM1831V33 is offered in a vertical ZIP configuration.

Presence detect pins (PD<sub>0</sub>-PD<sub>1</sub>) are used to identify module memory density in applications where modules with alternate word depths can be interchanged.



## Selection Guide

	1831V33-12	1831V33-15	1831V33-20	1831V33-25	1831V33-35
Maximum Access Time (ns)	12	15	20	25	35
Maximum Operating Current (mA)	420	400	380	380	380
Maximum Standby Current (mA)	250	250	250	250	250



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C  
 Ambient Temperature with Power Applied ..... -10°C to +85°C  
 Supply Voltage to Ground Potential ..... -0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to +V<sub>CC</sub>  
 DC Input Voltage ..... -0.5V to +4.6V

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V (+10%/-5%)

**Electrical Characteristics** Over the Operating Range

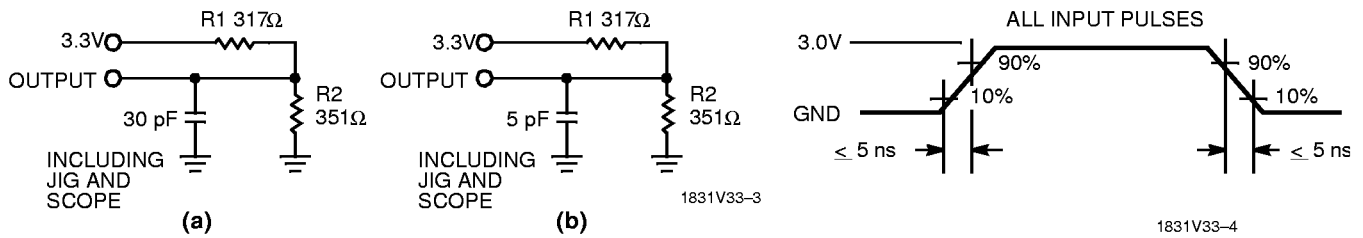
Parameter	Description	Test Conditions	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 4.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> ; Output Disabled	-10	+10	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, CS <sub>N</sub> ≤ V <sub>IL</sub>	-12 -15 -20, -25, -35	420 400 380	mA
I <sub>SB1</sub>	Automatic CS Power-Down Current <sup>[1]</sup>	Max. V <sub>CC</sub> ; CS ≥ V <sub>IH</sub> ; Min. Duty Cycle = 100%	-12, -15, -20, -25, -35	250	mA
I <sub>SB2</sub>	Automatic CS Power-Down Current <sup>[1]</sup>	Max. V <sub>CC</sub> ; CS ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V	-12, -15, -20, -25, -35	250	mA

**Capacitance<sup>[2]</sup>**

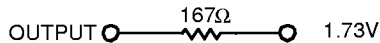
Parameter	Description	Test Conditions	Max.	Unit
C <sub>INA</sub>	Input Capacitance (WE, OE, A <sub>0-19</sub> )	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	12	pF
C <sub>INB</sub>	Input Capacitance (CS)		6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Notes:**

1. A pull-up resistor to V<sub>CC</sub> on the CS input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
2. Tested on a sample basis.

**AC Test Loads and Waveforms**


Equivalent to: THÉVENIN EQUIVALENT


**Switching Characteristics** Over the Operating Range<sup>[3]</sup>

Parameter	Description	1831V33-12		1831V33-15		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	12		15		ns
$t_{AA}$	Address to Data Valid		12		15	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACS}$	$\overline{CS}$ LOW to Data Valid		12		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z		7		8	ns
$t_{LZCS}$	$\overline{CS}$ LOW to Low Z <sup>[4]</sup>	3		3		ns
$t_{HZCS}$	$\overline{CS}$ HIGH to High Z <sup>[4, 5]</sup>		7		8	ns
$t_{PD}$	$\overline{CS}$ HIGH to Power-Down		12		15	ns
<b>WRITE CYCLE<sup>[6]</sup></b>						
$t_{WC}$	Write Cycle Time	12		15		ns
$t_{SCS}$	$\overline{CS}$ LOW to Write End	9		10		ns
$t_{AW}$	Address Set-Up to Write End	9		10		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	1		1		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		ns
$t_{SD}$	Data Set-Up to Write End	7		8		ns
$t_{HD}$	Data Hold from Write End	1		1		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5]</sup>	0	7	0	8	ns

**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCS}$  is less than  $t_{LZCS}$  for any given device. These parameters are guaranteed and not 100% tested.
- $t_{HZCS}$  and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of AC Test Loads and Waveforms. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CS}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

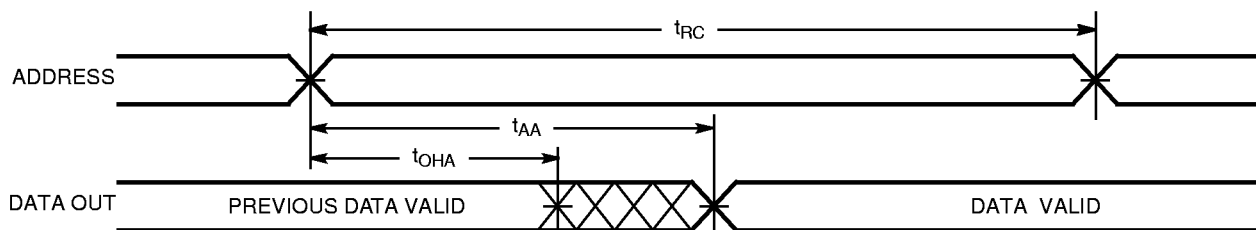


Switching Characteristics Over the Operating Range<sup>[3]</sup>(continued)

Parameter	Description	1831V33-20		1831V33-25		1831V33-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
$t_{RC}$	Read Cycle Time	20		25		35		ns
$t_{AA}$	Address to Data Valid		20		25		35	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACS}$	$\overline{CS}$ LOW to Data Valid		20		25		35	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		12		15		18	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z		10		12		15	ns
$t_{LZCS}$	$\overline{CS}$ LOW to Low Z <sup>[4]</sup>	3		3		3		ns
$t_{HZCS}$	$\overline{CS}$ HIGH to High Z <sup>[4, 5]</sup>		10		12		15	ns
$t_{PD}$	$\overline{CS}$ HIGH to Power-Down		20		25		35	ns
<b>WRITE CYCLE<sup>[6]</sup></b>								
$t_{WC}$	Write Cycle Time	20		25		35		ns
$t_{SCS}$	$\overline{CS}$ LOW to Write End	17		20		30		ns
$t_{AW}$	Address Set-Up to Write End	17		20		30		ns
$t_{HA}$	Address Hold from Write End	3		3		3		ns
$t_{SA}$	Address Set-Up to Write Start	2		2		2		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	15		20		30		ns
$t_{SD}$	Data Set-Up to Write End	12		15		20		ns
$t_{HD}$	Data Hold from Write End	2		2		2		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5]</sup>	0	12	0	12	0	15	ns

Switching Waveforms

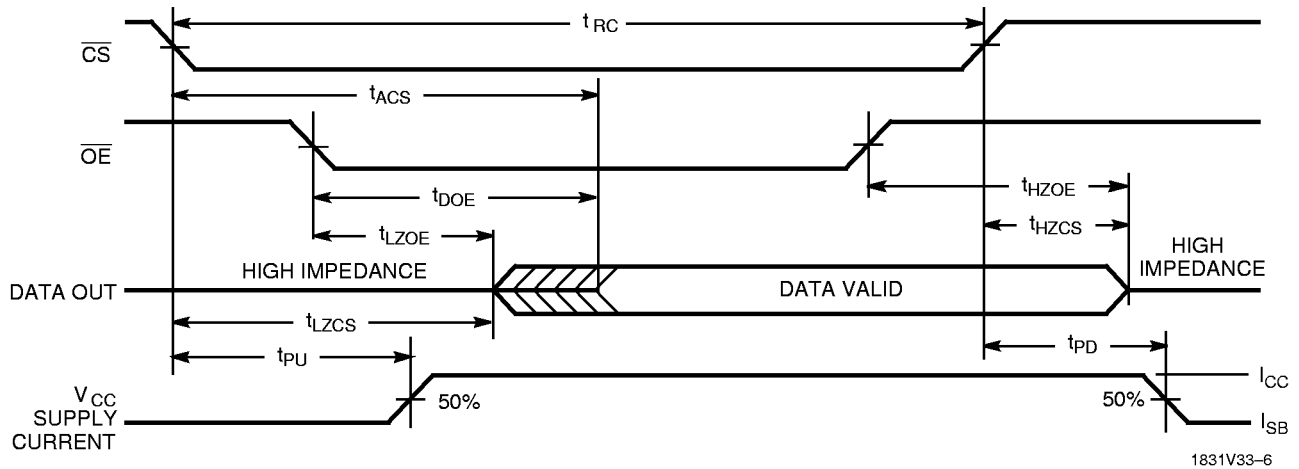
Read Cycle No. 1 <sup>[7, 8]</sup>



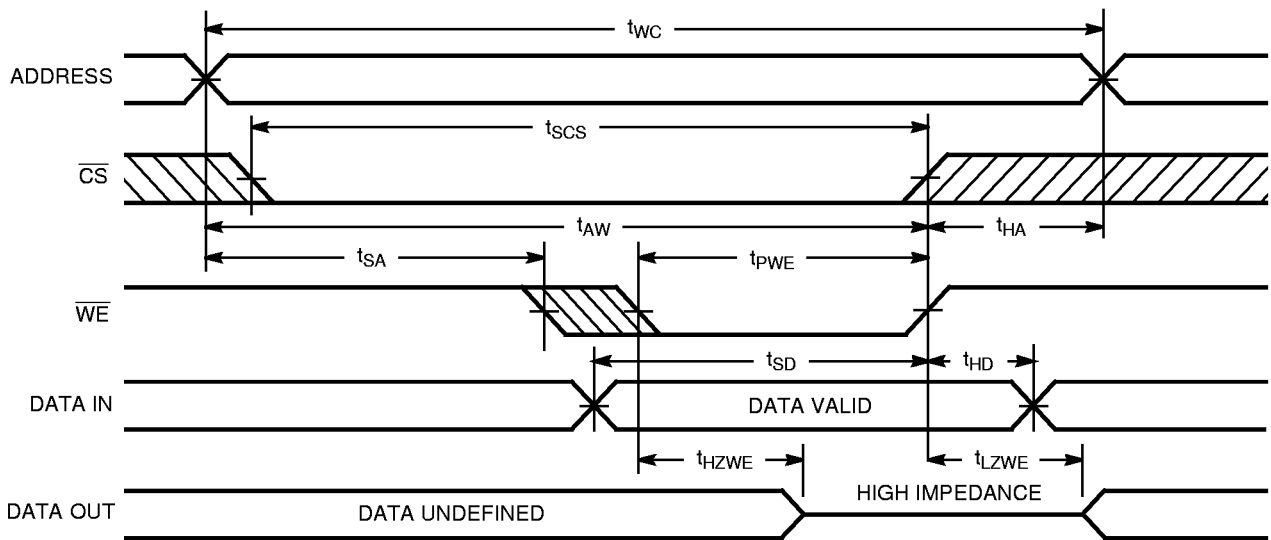
1831V33-5

Notes:

7.  $\overline{WE}$  is HIGH for read cycle.
8. Device is continuously selected,  $\overline{CS} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .

**Switching Waveforms (continued)**
**Read Cycle No. 2 [7, 9]**


1831V33-6

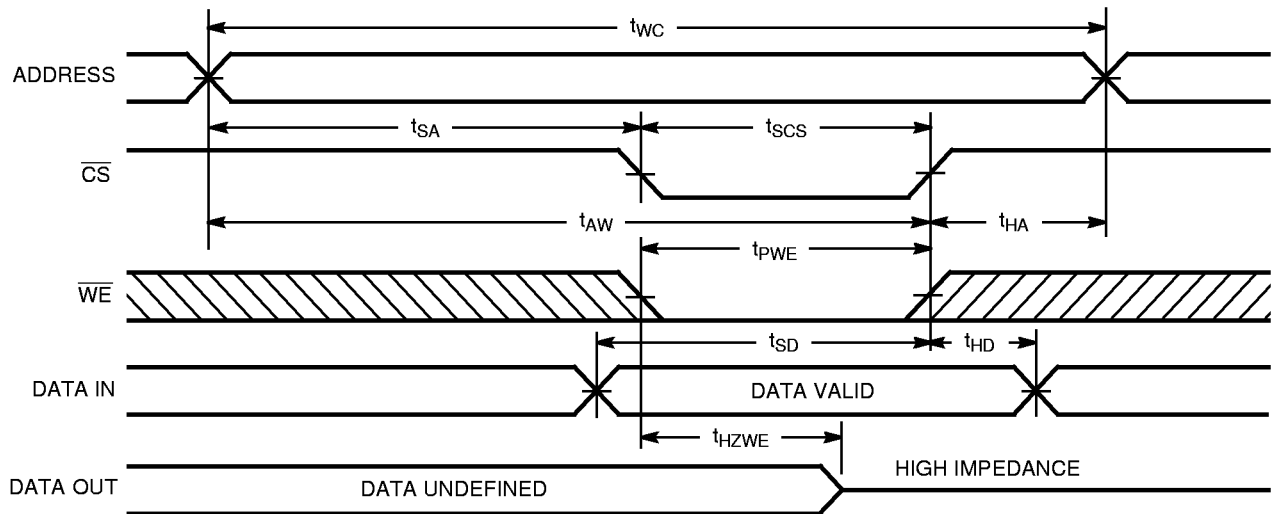
**Write Cycle No. 1 ( $\overline{WE}$  Controlled) [6]**


1831V33-7

**Note:**

9. Address valid prior to or coincident with  $\overline{CS}$  transition LOW.

**Switching Waveforms** (continued)

**Write Cycle No. 2 ( $\overline{\text{CS}}$  Controlled)** <sup>[6,10]</sup>


1831V33-8

**Note:**

 10. If  $\overline{\text{CS}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.

**Truth Table**

$\overline{\text{CS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

**Ordering Information**

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
12	CYM1831V33PZ-12C	PZ12	64-Pin Plastic ZIP Module	Commercial
15	CYM1831V33PZ-15C			
20	CYM1831V33PZ-20C			
25	CYM1831V33PZ-25C			
35	CYM1831V33PZ-35C			

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Package Diagram

64-Pin Plastic ZIP Module PZ12

