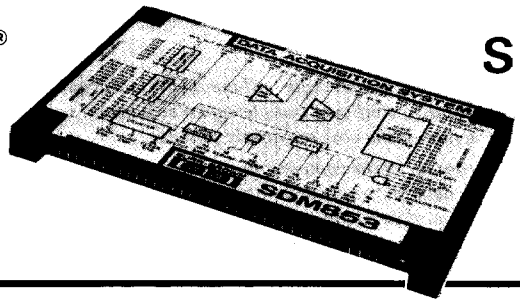
BURR-BROWN®



SDM853

023775

DATA ACQUISITION SYSTEM

FEATURES

- SAVES DESIGN TIME
- RELIABLE - 168-hour bake
- LOW LEVEL OR HIGH LEVEL INPUTS
- SAVES SPACE
- FLEXIBLE - Up to four modes of operation
- LOW COST

DESCRIPTION

The SDM853 is a complete 8- or 16-channel data acquisition system in a compact 4.6" x 3.0" x 0.375" metal case. This system differs from most in that it can acquire and digitize low level or high level analog signals. A built-in high quality instrumentation amplifier allows input signal ranges of ±10mV to ±10V. This means that the SDM853 can be connected to low level sensors such as thermocouples and strain gauges without external signal conditioning.

This expandable module accepts either 16 single-ended or 8 differential inputs and converts the multiplexed data signals into 12-bit digial words with an accuracy of ±0.025% at throughput rates of up to 33,000 samples per second.

International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

DISCUSSION OF PERFORMANCE

The SDM853 is a complete modular "off-the-shelf" data acquisition system. With this system it is possible to configure complete data acquisition systems in one-fourth the space for a fraction of the cost previously possible.

These systems contain all the components necessary to multiplex and convert ±10mV to ±10V analog data into equivalent digital outputs yielding resolutions of 2.4μV to 2.4mV. The minimum throughput sampling rates are up to 30kHz for 12-bit and up to 43kHz for 8-bit resolution. The model SDM853 contains an analog multiplexer which can be connected in a 16-channel single-ended or 8-channel differential mode, instrumentation amplifier, sample/hold, 12-bit successive approximation A/D converter and programming logic. The amplifier and sample/hold are not internally interconnected. This allows maximum application flexibility. These systems can be expanded without limit using Burr-Brown's MPC-16S and MPC-8D monolithic multiplexers. Figure 1 shows the components of the SDM853. The system is designed to be mounted on a printed circuit card. The only requirement for system operation are input signals, power and the interconnection of the system components into the desired operating configuration.

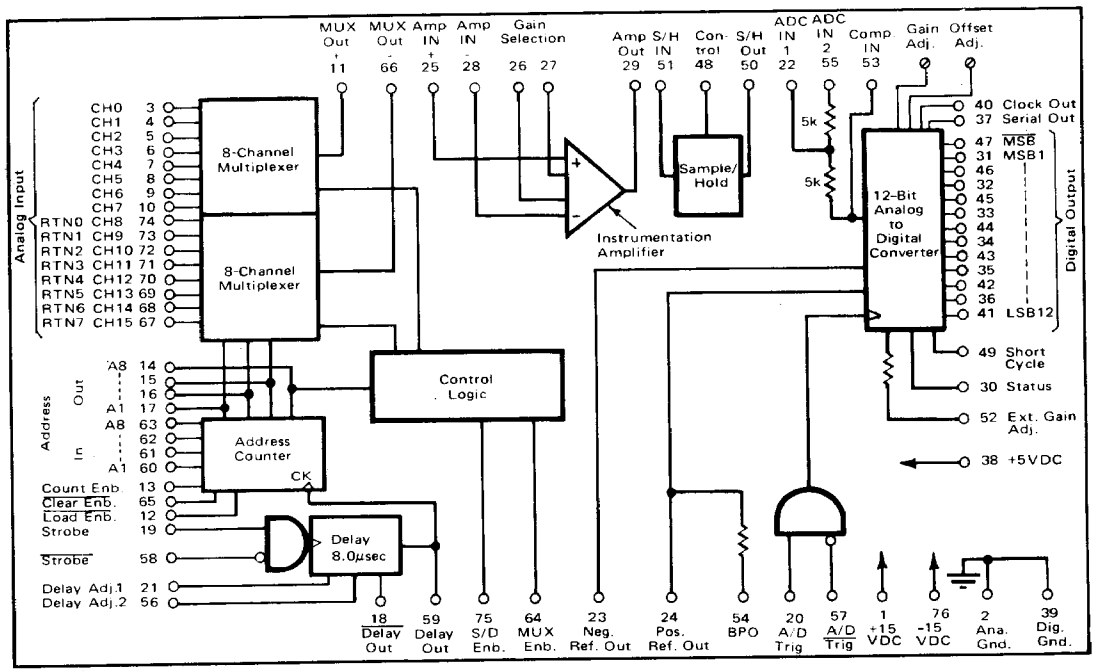


FIGURE 1. SDM853 Block Diagram.

ANALOG MULTIPLEXER

Two one-of-eight CMOS analog multiplexers are used to allow user selection by external jumpers of 16 single-ended channel or 8 double-ended channel operation. In 16-channel operation the multiplexer may be used in a pseudo differential mode by connecting the amplifier inverting input to a common, remote, signal ground. Channel selection is by a 3- or 4-bit binary word stored in a presettable address counter. Channel capacity is expandable without limit.

INSTRUMENTATION AMPLIFIER

The instrumentation amplifier is a low drift, differential amplifier featuring high speed at gains above unity, and external gain-programming with an external resistor. With the gain-programming pins open, the gain is unity. Gain may be selected from unity to 60 dB.

SAMPLE AND HOLD AMPLIFIERS

The sample and hold amplifier is a complete, stand alone, sample and hold circuit featuring buffered output, 7μsec acquisition time, and 30nsec aperture time. Input, output and mode control functions are brought to separate connector pins. This allows maximum system flexability for performing such functions as automatic gain ranging with no loss of aperture time.

ANALOG-TO-DIGITAL CONVERTER

The ADC is a ceramic packaged, 12-bit converter featuring 24μsec conversion time and 0.01% accuracy. Thin-film networks and current switching are used to assure linearity over wide temperature ranges.

ADDRESS COUNTER

A 4-bit binary address counter is connected to the multiplexer. This counter may be externally loaded, cleared, clocked or enabled. The address outputs are brought to connector pins for convenient system control.

DELAY TIMER

The delay timer is provided to allow for the settling time of the multiplexer, amplifier, and sample and hold circuits. The delay time is adjustable over a wide range by an external potentiometer and, or external capacitor. This allows for the longer settling time of the instrument amplifier at high gains.

CONTROL LOGIC

Delay and ADC trigger functions are edge-triggered and gated. Counter control functions are synchronous with the counter clock which is internally connected to the delay timer output.

CHANNEL EXPANSION

The number of analog input channels of these systems can easily be increased using Burr-Brown's MPC8D and MPC16S CMOS multiplexers. the MPC8D is an 8-channel differential model and the MPC16S is a 16-channel single-ended model. These are latch-free devices which contain internal binary decoding, TTL or MOS logic levels, and may be integrated into a system with minimum external logic.

SYSTEM PERFORMANCE

The SDM853 can be configured to continuously sequence through all analog channels, to accept random addresses or to sequence through all analog channels on command from an external trigger.

The status signal, pin 30, is connected to the strobe not input of the delay timer, pin 58, for normal program sequencing with a minimum throughput sampling rate of 30kHz for 12-bit resolution.

By using "overlap" programming, the settling time effects of the analog multiplexer and instrumentation amplifier can be reduced, extending throughput sampling rates up to 32kHz for 12-bit and 43kHz to 8-bit resolution. This mode of operation is most useful when converting low level inputs to accommodate the increased settling time of the instrumentation amplifier. Overlap programming is accomplished by connecting the status signal, pin 30, to the strobe input of the delay timer, pin 19, and extending the delay time. The internal logic will then select analog channel (n + 1) while channel n is being converted.

SYSTEM PERFORMANCE

(Typical at 25°C and rated supplies)

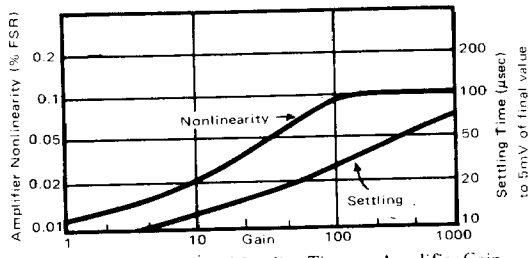


FIGURE 2. Nonlinearity and Settling Time vs. Amplifier Gain.

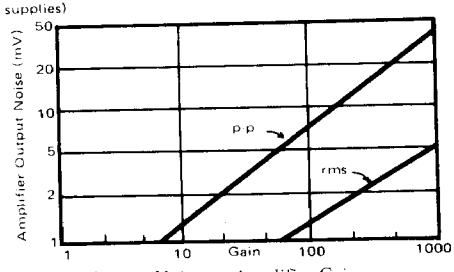


FIGURE 3. Output Noise vs. Amplifier Gain.

System Gain	System Accuracy	Throughput Rate (Channels/sec)		Delay Time (μsec)	
V/V		Normal	Overlap	Normal	Overlap
1	±0.025% FSR	30k	32k	9	31
10	±0.035% FSR	25k	32k	18	31
100	±0.08% FSR	20k	32k	25	31
1000	±0.1% FSR	10k	14k	70	70

TABLE I. Throughput Rate vs. Gain for Normal and Overlap Modes.

FSR	ADC Range	Amplifier Gain	Resolution	Delay for Settling to ±0.2% (μsec)	Delay for Settling to ±0.05% (μsec)	Delay for Settling to 0.01% (μsec)
20V	±10V	1	4.88mV	7	8	9
1V	0 to 10V	10	244μV	10	15	18
0.1V	0 to 10V	100	24.4μV	20	25	30
10mV	0 to 10V	1000	2.44μV*	60	70	-

TABLE II. This table shows the delay timer setting required to allow for the settling time of the instrumentation amplifier to the accuracies specified. Add the 24μsec conversion time of the A/D converter to the above delay times to obtain channel conversion times. * Depends on desired S/N ratio.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

MODEL	SDM853
TRANSFER CHARACTERISTICS	
Throughput Rate, min	30kHz, 33μsec/channel
Resolution	12 Bits
Number of Channels	16 single-ended, 8 differential
ANALOG INPUTS	
ADC gain ranges	0-5V, 0-10V, ±2.5V, ±5V, ±10V
Amplifier gain range	1 to 1000
Amplifier gain equation	$G = 1 + 20k\Omega/R_{EXT}$[1]
Max. input voltage without damage	±16V
Max. input voltage for multiplexer operation	±10.24V
Input impedance	100MΩ, 10pF OFF channel 100MΩ, 100pF ON channel
Bias current	
25°C	20nA
0°C to 70°C	50nA
Differential Bias Current (25°C)	10nA
Differential Bias Current Drift	0.1nA/°C
Amplifier output noise (Gain = 100, R_s = 500Ω)	1.2mV, rms; 7mV, p-p
Amplifier input offset voltage, max	400μV
Amplifier voltage offset drift	2 + 20/GμV/°C
ACCURACY[2]	
System RSS accuracy at 25°C (Gain = 1)	±0.025% FSR[3] at 30kHz throughput
Linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Differential linearity (Gain = 1)	±1/2LSB, at 30kHz throughput
Quantizing error	±1/2LSB
Gain error	Adjustable to zero
Offset error	Adjustable to zero
Power supply sensitivity	±0.005% FSR/% change of supply voltage
STABILITY OVER TEMPERATURE	
System accuracy drift, max	±30ppm/°C of reading
Linearity drift	±3ppm of FSR/°C
DYNAMIC ACCURACY	
Sample & Hold aperture time	30nsec
Aperture time uncertainty	±5nsec
Error for full scale transition between successively addressed channels	1LSB at 30kHz
Differential amplifier CMRR (Gain = 1)	74dB at 1kHz 65dB at 3kHz (100dB at 60Hz Gain = 1000)
Channel cross talk	80dB down at 2kHz, for OFF channel to ON channel
Sample & Hold feedthrough	80dB down at 5kHz
Sample & Hold decay rate	10μV/μsec
OUTPUT	
Output Coding (Complementary)	Unipolar Straight Binary, Bipolar Offset, Binary Two's Complement
Gain trim[4]	Adjustable to zero error
Offset trim[4]	Adjustable to zero error
A/D Conversion Time	24μsec
Delay	9μsec nominal, externally adjustable from 5.5μsec to 14μsec[5]
POWER REQUIREMENTS	±15VDC ±3% at +50mA, 5mV, rms, ripple -15VDC ±3% at -75mA, 5mV, rms, ripple +5VDC ±5% at +300mA, 25mV, rms, ripple
ENVIRONMENTAL	
Operating temperature	0°C to 70°C
Storage temperature	-25°C to +85°C
Relative humidity	95% noncondensing

1. With R_{EXT} between pins 26 and 27.
2. No missing codes guaranteed.
3. FSR means Full Scale Range.
4. Gain and Offset controls are located in the module. The adjustment ranges are ±0.1% FSR for Gain and ±0.1% FSR for Offset.
5. Adjustable to 10 seconds with external capacitor.

DIGITAL INPUT SPECIFICATIONS

Address inputs	One standard TTL load, positive true
Coding	4-bit binary
Load Enable	One standard TTL load, negative true, address loaded with strobe inputs.
Clear Enable	One standard TTL load, negative true, address loaded with strobe inputs.
Strobe & Strobe	One standard TTL load, STROBE and $\overline{\text{STROBE}}$ edge trigger the delay timer and clock the address counter. STROBE must be high to enable $\overline{\text{STROBE}}$ and $\overline{\text{STROBE}}$ must be low to enable STROBE.
Count Enable	Two standard TTL loads, positive true, logic "0" allows the Strobe inputs to trigger the delay timer, but prevents the MUX address counter from being clocked.
ADC trigger	One standard TTL load, a positive going edge at TRIG initiates conversion, a negative going edge at $\overline{\text{TRIG}}$ initiates conversion; $\overline{\text{TRIG}}$ must be "0" to enable TRIG; TRIG must be "1" to enable $\overline{\text{TRIG}}$.
Short cycle	One standard TTL load, logical 1 for 12-bit resolution, connected to the N + 1 bit output for N bit resolution.
Multiplexer Enable	Two standard TTL loads, logical 1 enable multiplexer output and logical 0 turns off all channels.
Multiplexer Enable	Two standard TTL loads, logical 1 enables 16-channel single-ended operation and logical 0 enable 8-channel differential operation.
S, D select	

DIGITAL OUTPUT SPECIFICATIONS

Data outputs	2 Standard TTL loads, negative true.
Parallel B1, B1 . . . B12	2 Standard TTL loads, negative true, time serial data output beginning with B1, (see timing diagram).
Serial out	5 Standard TTL loads, positive true, 4-bit binary code, internal 2kΩ pull-up resistors.
Address outputs	5 Standard TTL loads high (low) during the delay period, triggered by Strobe and Strobe inputs.
Delay out (Delay Out)	5 Standard TTL loads for synchronizing serial out data (see timing diagram).
Clock	5 Standard TTL loads, high during the A/D conversion.
Status	

SYSTEM TIMING DIAGRAMS

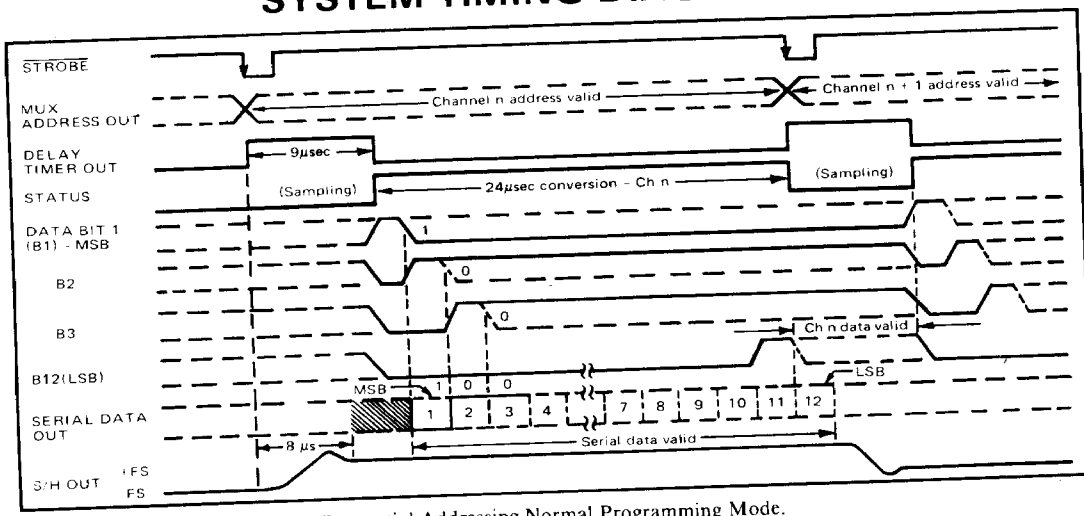


FIGURE 4. Timing Diagram for Sequential Addressing Normal Programming Mode.

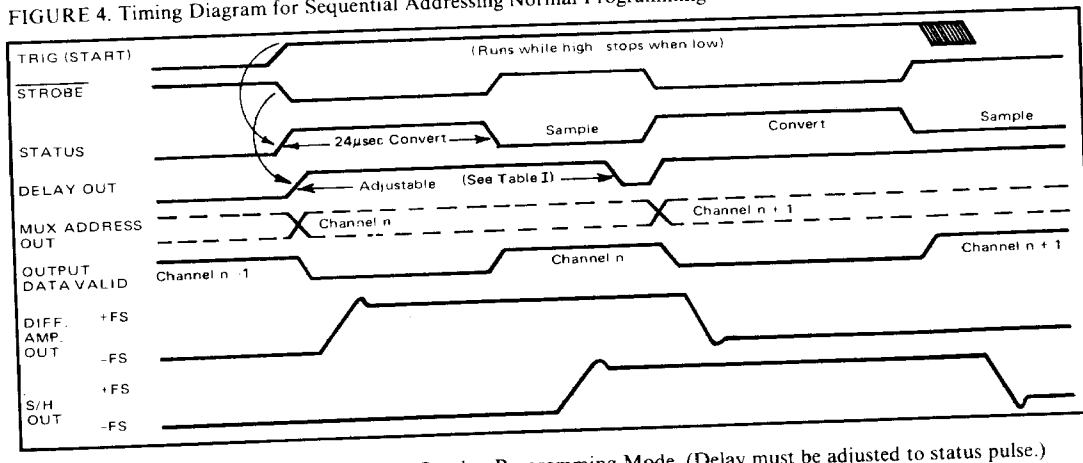
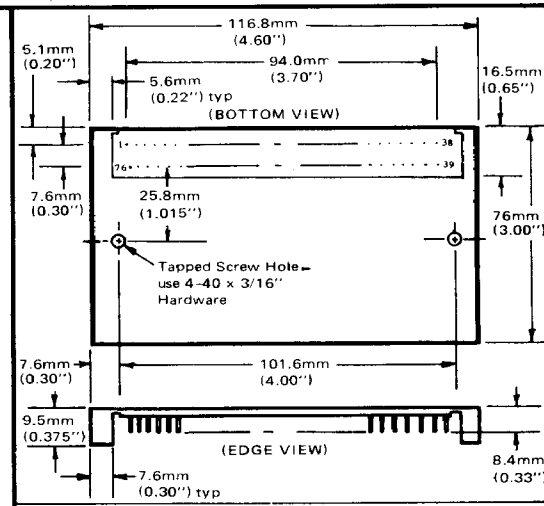


FIGURE 5. Timing Diagram for Sequential Overlap Programming Mode. (Delay must be adjusted to status pulse.)

PACKAGE AND PIN CONFIGURATION

SDM853 CONNECTOR PIN DIAGRAM

+15VDC	1	76	-15VDC
ANA. GND.	2	75	S/D ENB
CH 0 IN	3	74	CH 8 IN (0 RTN)
CH 1 IN	4	73	CH 9 IN (1 RTN)
CH 2 IN	5	72	CH 10 IN (2 RTN)
CH 3 IN	6	71	CH 11 IN (3 RTN)
CH 4 IN	7	70	CH 12 IN (4 RTN)
CH 5 IN	8	69	CH 13 IN (5 RTN)
CH 6 IN	9	68	CH 14 IN (6 RTN)
CH 7 IN	10	67	CH 15 IN (7 RTN)
MUX OUT HI	11	66	MUX OUT LO
$\overline{\text{LOAD ENB}}$	12	65	$\overline{\text{CLR ENB}}$
COUNT ENB	13	64	MUX ENB
A8 OUT	14	63	A8 IN
A4 OUT	15	62	A4 IN
A2 OUT	16	61	A2 IN
A1 OUT	17	60	A1 IN
$\overline{\text{DLY.}}$	18	59	DLY.
STROBE	19	58	$\overline{\text{STROBE}}$
ADC TRIG	20	57	ADC $\overline{\text{TRIG}}$
DLY. ADJ. 1	21	56	DLY. ADJ. 2
R1	22	55	R2
NEG REF OUT	23	54	BPO
POS. REF OUT	24	53	COMP IN
AMP IN HI	25	52	GAIN ADJ.
G2	26	51	S/H IN
G1	27	50	S/H OUT
AMP IN LO	28	49	SHT. CYC.
AMP OUT	29	48	S/H CONTROL
STATUS	30	47	$\overline{\text{B1}}$
B1 MSB	31	46	B2
B3	32	45	B4
B5	33	44	B6
B7	34	43	B8
B9	35	42	B10
B11	36	41	B12 LSB
SER OUT	37	40	CLK. OUT
+5	38	39	DIG RTN



CASE MATERIAL: Insulated Steel
CONNECTOR PINS: Gold Flashed
WEIGHT: 145 grams (5 oz.)

MOUNTING INSTRUCTIONS:

MOUNTING FLUSH ON PC CARD

1. Use strip connectors or two 14-pin and three 16-pin low profile IC sockets (shipped with each unit).
2. Use 4-40 x 3/16" (4.8mm) LG Pan HD Hardware to secure the SDM853 to PC Card.

ORDERING INFORMATION

Model	Description			Model	Description		
SDM853	16 Channel Single-ended or 8 Channel Differential Data Acquisition System			MPC16S	16 Channel Single-ended CMOS Multiplexer in 28 pin DIP		
MPC 8D	8 Channel Differential CMOS Multiplexer in 28 pin DIP			546	+5V to ±15VDC/DC Converter		