SSI 32P547
High Performance Pulse Detector

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DESCRIPTION

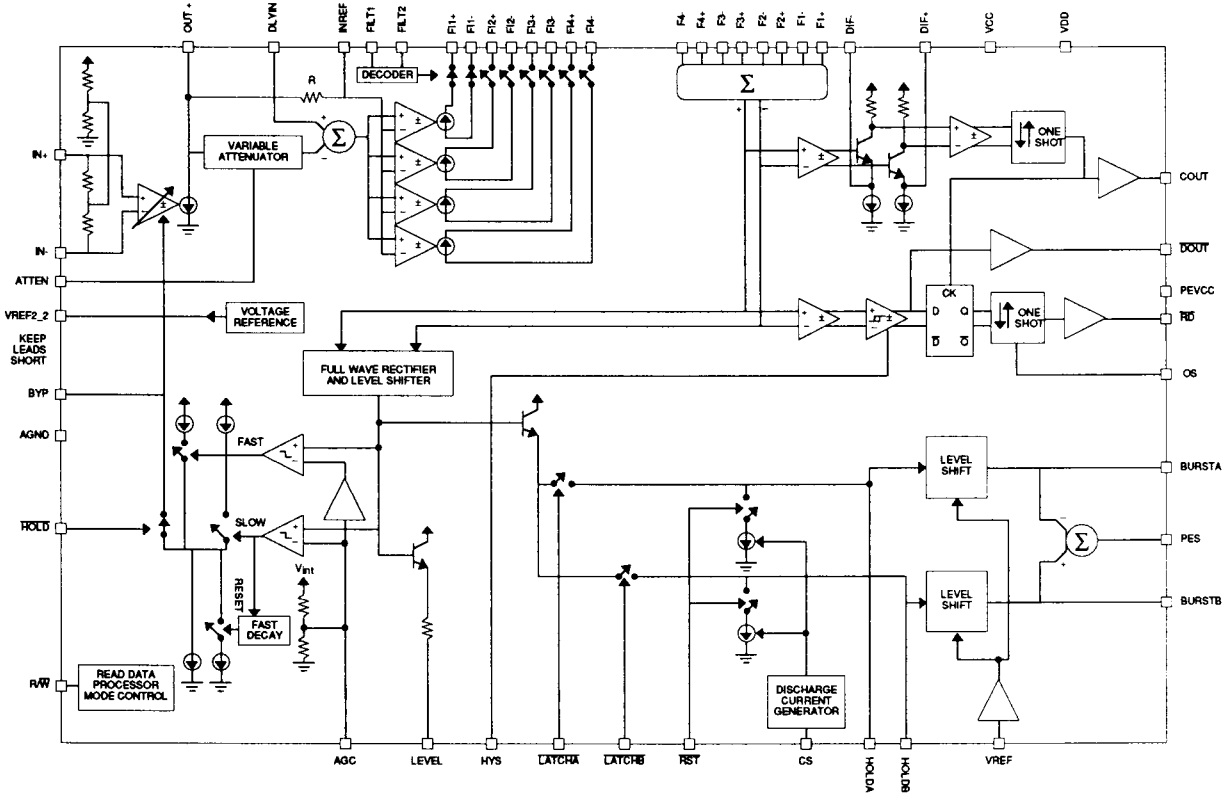
The SSI 32P547 Read Data Processor and Servo Demodulator with Variable Pulse Slimming and Zone Filter Mux is a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

Time and amplitude qualification are used to provide a PECL output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier.

FEATURES

- **Wide bandwidth AGC input amplifier**
- **Uses standard +12V and +5V ± 10% supplies**
- **Level qualification supports MFM or RLL codes**
- **Servo burst capture circuit for use in embedded servo**
- **Four input differential filter MUX**
- **Pulse Slimming with Variable Attenuation**

BLOCK DIAGRAM



CIRCUIT OPERATION

Level qualification can be implemented as fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output.

The SSI 32P547 requires standard ±10% tolerance +5V and +12V supplies and is available in a 52-pin Quad PLCC package.

MODE CONTROL

The circuit mode is controlled by the R/$\overline{W}$, and $\overline{HOLD}$ as shown in Table 1.

READ MODE

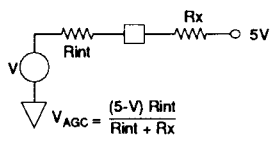
The circuit is placed in the read mode when the R/$\overline{W}$ pin is high or open and is disabled (write mode) when the R/$\overline{W}$ pin is low. In the write mode the digital circuitry is disabled, the AGC amplifier gain is set to maximum and the input impedance of the input analog stage is reduced to allow more rapid settling of the input coupling capacitors from the read/write circuit (such as the SSI 32R510A) upon transition to the read mode. Write to read transition timing is controlled to allow settling of the coupling capacitors between the read/write circuit and the SSI 32P547 before the AGC circuitry is activated when going to the read mode. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow for more rapid settling. When the R/$\overline{W}$, and $\overline{HOLD}$ pins are high or open the input amplifier is in the read data AGC mode and gain is controlled to keep a constant read data peak level. When the $\overline{HOLD}$ pin is pulled low the gain of the analog circuit is held at the level determined when the $\overline{HOLD}$ pin was high (the gain will slowly drift due to leakage).

READ DATA AUTOMATIC GAIN CONTROL CIRCUIT

In this mode an amplified head output signal, such as the output of the SSI 32R117, 32R501, or 32R510A read/write circuits, is AC coupled to the IN+ and IN- inputs. In the read mode the level at the Fx +/- pins is controlled by full wave rectifying the level at the summer output and comparing it to a reference level supplied at the AGC pin. When the input level at the filter outputs is greater than 125% of the desired level as set by the AGC pin, the circuit is in a fast attack mode and will supply about 1.8 mA of charging current at the BYP pin. When the input level is between 125% and 100% of the desired level, the circuit enters a slower attack mode and will supply about 0.18 mA of charging current. This allows the AGC to rapidly recover when going from write to read but reduces zero crossing distortion once the AGC amplifier is in range.

To reduce the effect of gain attack overshoot on settling time (due to offsets) a fast decay mode is entered if slow decay mode exceeds 1.6 µsec (nom). Fast decay discharge current is 0.8 mA and slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the level at the filter input pins is 0.83 Vpp. The level at the filter input pins can be increased by tying a resistor from the AGC pin to VCC or reduced by tying a resistor from the AGC pin to GND.



Where:

V = Voltage at AGC with pin open (2.4V, nom.)

Rint = AGC pin input impedance (6.7 KΩ, typ.)

Rx = External resistor.

The new DIN+/- input target level is nominally 0.43 Vp-p/V_{AGC}.

Gain of the AGC section in the AGC mode is approximately: $\left(\frac{Av1}{Av2}\right) = \exp\left[6.9 \times (V2 - V1)\right]$

Where:

Av1, Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

READ DATA PULSE SLIMMING CIRCUIT

The Pulse Slimming Circuit uses an external delay line and an analog controllable Variable Attenuator to implement pulse slimming. Input biasing for this stage is accomplished by low pass filtering the signal at the

OUT+ pin with an on chip resistor and external capacitor tied to the INREF pin and using that signal as a reference to the single-ended-to-differential gain stage which follows.

$$\text{Freq}(-3\text{dB}) = \frac{1}{2\pi RC}$$

Where: R (lowpass) is the on-chip resistor = 6 kΩ nom
C (ext) is the external capacitor

The ratio between the gains of the attenuated and non-attenuated signal paths (K) is controlled by varying the gain of the on-chip attenuator:

K = Av (attenuated) / Av (non-attenuated)
= Ko - G x V (ATTEN) / VREF2_2

Where G is the gain factor, V (ATTEN) is the voltage applied to the ATTEN pin. VREF2_2 is the voltage on the VREF2_2 pin and Ko is the value for K when V(ATTEN) = 0.0V.

SELECTABLE EXTERNAL FILTER DRIVER/RECEIVER

The on-chip circuitry allows four separate filters to be used for support of constant density recording. A filter is selected by using the two TTL input filter select pins; FILT1, and FILT2. Filter selection is as follows:

Filter1	Filter 2	Channel
0	0	FI1
0	1	FI2
1	0	FI3
1	1	FI4

READ MODE DIGITIZING SECTION

In the data path the signal is sent to a hysteresis comparator. The comparator hysteresis level can be set at a fixed level or, with the addition of an external filter network, a fraction of the signal level.

The latter approach allows setting the AGC circuit decay and slow attack times slow enough to minimize distortion of the signal going into the clocking path and setting a short time constant for the hysteresis level. Thus when switching to a head with a different output level or when switching from write to read the circuit is properly decoding data before the AGC circuit gain has settled to its final steady state value. The output of the hysteresis comparator is the "D" input of a D flip-flop. The $\overline{\text{DOUT}}$ pin provides a PECL comparator output digital signal for testing purposes and, if required, for use in the servo circuit.

In the clocking path the signal is sent to a differentiator circuit whose characteristics are set by external components. The differentiator transfer expression from Fx+/- to the comparator input (which is not the DIF+/- output) is:

$$Av = \frac{-2C_{ex}R_i s}{2L_{ex}C_{ex}s^2 + C_{ex}(R_{ex} + 2R_e)s + 1}$$

Where: R_i= on chip resistors = 1.0 KΩ nominally; R_e= emitter resistance seen at DIF+ or DIF- = 46 Ω nominally; C_{ex}= external capacitor, allowable range is 20 pF to 150 pF; R_{ex}= external resistor; L_{ex}= external inductor.

The output of the differentiator circuit is sent to the edge trigger circuit which creates an output pulse on every zero crossing of the output of the differentiator. The output of the edge trigger is the clock input of the D flip-flop. During normal system operation the differentiator circuit clocks the D flip-flop once every positive and negative peak of the input signal.

The data path D input to the flip-flop only changes state when the signal applied to the filter inputs exceeds the hysteresis comparator threshold in a polarity opposite the polarity of the peak which last exceeded the threshold. Therefore, the clocking path determines signal timing and the data path blocks spurious peaks if they do not exceed the hysteresis comparator threshold. Figure 6 shows circuit operation of the digital section. The two digital signal path delays between the Fx+ and Fx- inputs to the flip-flop clock and data inputs are well matched.

SERVO BURST CAPTURE SECTION

Rectified servo data peaks are latched into the A or B servo channels by pulling the TTL compatible inputs $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low, respectively. A chip-generated discharge current is turned on for channels A or B by pulling the TTL compatible input $\overline{\text{RST}}$ low. The magnitude of this discharge current is set by a resistor tied to the CS pin.Outputs of the BURSTA, BURSTB, and PES are referenced to an externally generated reference applied at the VREF pin.

PIN DESCRIPTIONS

POWER SUPPLY AND CONTROL

NAME	I/O	DESCRIPTION
VCC		5 Volt power supply.
PEVCC		Collector of PECL emitter follower output which is to be connected to the 5 volt power supply.
VDD		12 volt power supply
AGND		Analog ground pin
R/$\overline{W}$	I	TTL compatible read/write control pin

AGC GAIN STAGE

IN+,IN-		Analog signal input pins
OUT+		Transconductance output for the AGC amplifier and input to the variable attenuator
DLYIN		Delayed input signal to the pulse slimming amplifier
INREF		Reference DC voltage to the single ended to differential gain stage
VREF2_2		Internally generated voltage used as a reference by the external DAC used to control the attenuator gain
BYP		The AGC timing capacitor is tied between this pin and AGND
$\overline{HOLD}$	I	TTL compatible control pin which holds the input AGC amplifier AGC level when pulled low
ATTEN		An Analog input which controls the attenuation value for the Variable Attenuator
AGC		Reference input voltage for the AGC circuit

SERVO BURST CAPTURE STAGE

$\overline{LATCHA}$ $\overline{LATCHB}$	I	TTL inputs which initiates capture of a servo burst Peak on channel A or B when pulled low
HOLDA HOLDB		Peak holding capacitors are tied from each pin to GND
$\overline{RST}$	I	TTL input which initiates discharge of channel A and B hold capacitors when pulled low
CS		Pin to control magnitude of discharge current during active discharge of channel A and B hold capacitors
VREF		Reference level for servo circuit
BURSTA BURSTB		Buffered burst peak outputs
PES		BURST B minus BURST A output

DIGITAL PROCESSING STAGE

NAME	I/O	DESCRIPTION
FIx± Fx±		Differential filter I/O pins for the four external filters
FILT1 FILT2	I	TTL compatible inputs to control multiplexer for selection of 1 of 4 filters
HYS		Hysteresis level setting input to the hysteresis level detect comparator
LEVEL		Provides rectified signal level for input into the hysteresis circuit
$\overline{DOUT}$	O	A Pseudo ECL D input into D flip-flop provided for testing or servo use
DIF+,DIF-		Pins for external differentiator components
COUT	O	Clock input into D flip-flop provided for testing
OS		Pin for external capacitor in the one shot which determines read channel output one-shot pulse width
$\overline{RD}$	O	A Pseudo ECL (PECL) read output

TABLE 1: Mode Control

MODE	R/$\overline{W}$	$\overline{HOLD}$	CONDITIONS
Read/AGC	1	1	Read amp on, AGC active and controlled by data, Digital section active
Read/Hold	1	0	Read amp on at fixed gain, AGC level held constant Digital section active
Write	0	-	Read amp on with reduced input impedance AGC level pulled low, Digital section deactivated, BYP pin set for maximum AGC gain

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATING

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNITS
+5V Supply Voltage,VCC, PEVCC	6.0	V
+12V Supply Voltage,VDD	14.0	V
Pin Voltage BYP, AGC, LEVEL, HYS, HOLD A/B, VREF, BURST A/B, PES, DIF+/-, FIx±	-0.3 to VDD+0.3	V
Pin Voltage IN+/-, $\overline{HOLD}$, R/$\overline{W}$, $\overline{RST}$, ATTEN, $\overline{LATCHA/B}$, CS, OS, FILT1-2, Fx±, OUT+, DLYIN, INREF, VREF2_2	-0.3 to VCC+0.3	V

ABSOLUTE MAXIMUM RATING (continued)

PARAMETER	RATING	UNITS
$\overline{RD}$, $\overline{DOUT}$, COUT	-0.3 to VCC+0.3 or +12mA	V
Storage Temperature	-65 to +150	°C
Lead temperature (soldering 10 sec)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCC	Supply Voltage		4.5	5.0	5.5	V
VDD	Supply Voltage		10.8	12.0	13.2	V
Tj	Junction Temperature		25		145	C
Ta	Ambient Temperature		0		70	C

ELECTRICAL CHARACTERISTICS

POWER SUPPLY

Recommended conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	VCC Supply Current	Outputs unloaded			50.0	mA
IDD	VDD Supply Current	Outputs unloaded			80.0	mA
Pd	Power dissipation	Ta=70° C Outputs unloaded			1.25	W

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Read-to-Write Transition time	R/$\overline{W}$ Pin High → Low			1.0	µs
Write to Read Transition time	R/$\overline{W}$ Pin Low → High AGC settling not included	1.2		3.0	µs
Hold On ↔ Hold off Transition time	$\overline{HOLD}$ Pin High ↔ Low R/$\overline{W}$ Pin High			1.0	µs

LOGIC SIGNALS ($\overline{HOLD}$, FILT1-2, R/$\overline{W}$, $\overline{LATCHA}$,$\overline{B}$, $\overline{RST}$ Pins)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	0.0		* -0.4	mA
IIH	Input High Current	VIH = 2.4V			100	µA

*For $\overline{RST}$ only, limit is -0.8 mA

PECL OUTPUT: $\overline{RD}$, $\overline{DOUT}$ PINS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Low Voltage				VCC-1.625	V
Output High Voltage		VCC-1.02			V
Output Rise Time	10 to 90 %			5.0	ns
Output Fall Time	90 to 10 %			5.0	ns

*Output load is a 2.5 kΩ resistor to GND, and a 5 pF capacitor to ground.

AUTOMATIC GAIN CONTROL CIRCUIT

All of the measurements in the AGC gain mode are made with the following conditions unless otherwise stated:

1. The circuit is in the read mode (R/$\overline{W}$, and $\overline{HOLD}$ pins high).
2. The circuit is connected as in Figure 5.
3. The amplifier inputs, IN+ and IN- , are AC coupled.
4. The OUT+ pin is loaded with 100 Ω to Vcc and Fx+, Fx- 200Ω each to VDD (through series capacitors).
5. A 1000 pF capacitor is tied between BYP and GND.
6. The AGC pin is left open.

READ DATA MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Slow AGC Capacitor Discharge Current	V(Fx+ - Fx-)=0.0 Volts Vary V(AGC) until slow discharge begins		4.5		µA
Fast AGC Capacitor Discharge Current	V(Fx+ - Fx-)=0.0 Volts Vary V(AGC) until fast discharge begins		0.8		mA
Fast Decay Hold Off Time	Slow Attack Threshold Not Reached	0.7	1.6	3.0	µs
AGC Capacitor Leakage Current	R/$\overline{W}$ pin high, $\overline{HOLD}$ low	-0.2		0.2	µA

ELECTRICAL CHARACTERISTICS (continued)

READ DATA MODE (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Slow AGC Capacitor Charge Current	V(Fx+ - Fx-)=0.41 Vdc, Vary V(AGC) until slow charge begins	-0.14		-0.22	mA
Fast AGC Capacitor Charge Current	V(Fx+ - Fx-)=0.8 Vdc Vary AGC until fast charge begins	-1.3		-2.0	mA
Fast → Slow Attack Switchover Point	Minimum V(Fx ±) in fast attack mode; Minimum V(Fx ±) in slow attack mode		0.15		V
Gain Attack Time (Ta) See Fig. 1	R/$\overline{W}$ = low → high, changing Vin from 200 to 400 mVpp @ 2.5 MHz, V(Fx±) to 110% of final value		4		µs
Fx+ - Fx- Input Voltage Swing vs AGC Input Voltage	15 mVpp < V(IN+ - IN-) < 250 mVpp, 0.4 Vpp < V(Fx+ - Fx-) < 1.25 Vpp, V(ATTEN) = V(VREF2_2)	0.25		0.48	Vpp/V
Fx+ - Fx- Input Voltage Swing Variation	15 mVpp < V(IN+ - IN-) < 250 mVpp 0.4 Vpp < V(Fx+ - Fx-) < 1.25 Vpp			8.0	%
AGC Pin Input Impedance		5.0		8.3	kΩ
AGC Pin Voltage	AGC pin open	2.28	2.4	2.52	V

AGC AMPLIFIER CHARACTERISTICS

Gain Range	Z Load = 100Ω	0.3		16.5	V/V
Output DC Voltage Variation	V(IN+) = V(IN-); over actual gain range			±150	mV
Maximum Allowable Output Voltage Swing on OUT+ pin				360	mVpp
Differential Input Resistance	V(IN+ - IN-)=100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	V(IN+ - IN-)=100 mVpp @ 2.5 MHz			10.0	pF
Common Mode Input Impedance	R/$\overline{W}$ pin = high		1.8		kΩ
(Both Sides)	R/$\overline{W}$ pin = low		250		Ω
Input Noise	Gain set to 16 V/V, RS = 0, BW = 15 MHz			25	$\frac{nV}{\sqrt{(Hz)}}$

AGC AMPLIFIER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Bandwidth	Transconductance (Iout/Vin) ± 3 dB bandwidth, referenced to 2.5 MHz	40			MHz
Common Mode Rejection Ratio (Input Referred)	V(IN+) = V(IN-) = 100 mV, 5 MHz, gain set to 16 V/V	40			dB
Output DC Current on OUT+ Pin	IN+, IN- shorted together		4.5		mA
Output Impedance, OUT+ Pin			50		kΩ
Output Capacitance OUT+ Pin			5		pF
Allowable DC Load Resistance To VCC on OUT+ Pin		88		112	Ω
Allowable AC Load Impedance on OUT+ Pin		88		112	Ω
Power Supply Rejection Ratio (input referred)	ΔV(VDD) or ΔV(VCC) = 100 mVpp, 5 MHz, gain set at 16 V/V	22			dB

PULSE SLIMMER, EXTERNAL FILTER DRIVERS AND VARIABLE ATTENUATOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain from OUT+ pin to (FIx+ - FIx-)	V (ATTEN) = VREF2_2		9		V/V
Kmin, minimum attenuator gain	V(ATTEN) = VREF2_2			0.05	
Kmax, maximum attenuator gain	V(ATTEN) = 0.0V	0.81			
Gain Factor G Tolerance	G(ideal) = 0.83, V(ATTEN) = VREF2_2	-4		+4	%
Ko Tolerance	Ko(ideal) = 0.84, V(ATTEN) = 0.0V	-4		+4	%
Attenuator Gain K Ratio Linearity	0.0 < V(ATTEN) < VREF2_2 end point method	-0.0		-4.5	%
OUT+ to INREF pin resistance		5		9	kΩ
Output Voltage Ref VREF2_2 Pin	Iload = 0 to -1 mA	1.95	2.28	2.45	V
Output Voltage Resistance VREF2_2 Pin	Iload = -.7mA		4		Ω
Maximum Output Voltage Swing	FIx±	1.25			Vpp

ELECTRICAL CHARACTERISTICS (continued)

PULSE SLIMMER AND EXTERNAL FILTER DRIVERS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Resistance DLYIN Pin			200		kΩ
Input Capacitance DLYIN Pin			5		pF
Bandwidth referenced to 2.5 MHz	Transconductance I(Flx± /V(OUT+)	40			MHz
Allowable External DC Load Resistance	Flx± to VDD	190		210	Ω
Power Supply Rejection Ratio (Input Referred)	ΔV (12) or ΔV (5) = 100 mVpp, 5 MHz delayline shorted	45			dB
Input Resistance ATTEN Pin			200		kΩ
Input Bias Current ATTEN Pin			8		μA

READ MODE DIGITIZING SECTION

All of the measurements in the read mode digital section are made with the following conditions unless otherwise stated:

1. The circuit is in the read mode (R/$\overline{W}$ pin is high).
2. The summer input pins, (Fx+, Fx-) receive AC coupled 2.5 MHz, 0.83 Vpp sine wave input signal.
3. 100 Ω in series with 65 pF are tied between DIF+ and DIF-.
4. A 1.8 Vdc voltage is applied to the HYS pin.
5. OS is tied to the 5V supply with a 60 pF capacitor, Cos.
6. The $\overline{DOUT}$ pin is loaded with a 2.5 kΩ resistor to GND and a 5 pF capacitor to GND.
7. The $\overline{RD}$ pin is loaded with a 2.5 kΩ resistor to GND and a 5 pF capacitor to GND.

SUMMER AND BUFFER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Allowable Input Signal Range	V(Fx+ - Fx-)			1.25	Vpp
Differential Input Resistance	V(Fx+ - Fx-) =100 mVpp DC	10		18	kΩ
Differential Input Capacitance	V(Fx+ - Fx-) =100 mVpp @2.5 MHz		4.0		pF
Common Mode Input Impedance	On all Fx+ to Fx- Fx+/- tied together	2.5		4.5	kΩ
Bandwidth referenced to 2.5 MHz	V(DIF±)/V(Fx±)	35			MHz

HYSTERESIS COMPARATOR CIRCUIT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
LEVEL Pin Output Voltage vs Fx+ - Fx- Input Voltage	0.4 < V(Fx+ -Fx-) < 1.25 Vpp, 10 kΩ between LEVEL pin and GND	1.8		3.0	V/Vpp
LEVEL Pin Output Impedance	I(LEVEL) = 0.5 mA		180		Ω
LEVEL Pin Maximum Output Current	V(Fx±) = 0.415V, ΔV(Level) ≤0.8 V	3.0			mA
Comparator and Summer Offset Voltage	HYS pin at GND, ≤1.5 kΩ across Fx+,Fx-.			30	mV
Input referred Hysteresis Voltage (at Fx+ - Fx- Pins) vs HYS Pin Voltage	1 V < V(HYS) < 3 V	0.16		0.25	V/V
Hysteresis threshold tolerance as a % of V(Fx+ - Fx-) peak	Set V(HYS) such that Hysteresis Threshold (Ideal) is 60% of V(Fx±), V(Fx±) = .415V (see Figures 2 & 3)	-15		+15	%
HYS Pin Input Current	1 V < V(HYS) < 3 V	0.0		-20	µA

* In an open loop configuration where reference is V(AGC), tolerance can be slightly higher.

DIFFERENTIATOR CIRCUIT

Voltage Gain from Fx+/- to DIF+/-	R(DIF+ to DIF-) = 2.0 kΩ	2.0		3.06	V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±1.3			mA
Comparator Offset Voltage	DIF+, DIF- AC coupled not directly measured			10.0	mV
COUT Pin Output Low Voltage	0.0 ≤ Iol ≤ 0.5 mA		VDD-3.0		V
COUT Pin Output Pulse Voltage Swing, V(high) - V(low)	0.0 ≤ Ioh ≤ 0.5 mA		+0.4		V
COUT Pin Output Pulse Width	0.0 ≤ Ioh ≤ 0.5 mA		30		ns
Required DFF Set-up Time, Td1 in Fig. 6	Minimum allowable time delay from V(Fx+,Fx-) exceeding hysteresis point to V(DIF+,DIF-) hitting peak value	0			ns
Propagation Delay, Td3 in Fig. 6				110	ns
Output Data Pulse Width at $\overline{RD}$ Pin, Td5 in Fig. 6	Td5(ideal) = 900 x Cos @ V($\overline{RD}$) = 50% 30 ≤ Cos ≤ 200 pF			±15	%

ELECTRICAL CHARACTERISTICS (continued)

READ DIGITAL SECTION AS SYSTEM

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Pulse Pairing |Td3 - Td4| Fig. 6	0.83 Vpp into Fx+/- pins at 2.5 MHz			1.5	ns
	0.83 Vpp into Fx+/- pins at 9.0 MHz			1.0	ns

SERVO BURST CAPTURE CIRCUIT

All of the measurements are made with the following conditions unless otherwise stated:

1. The circuit is connected as in Figure 5.
2. A and B bursts are sampled onto $\overline{\text{BURSTA}}$ and $\overline{\text{BURSTB}}$ pins.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Allowable VREF Voltage Range		3.9		6.0	V
BURSTA, BURSTB Pin Output Voltage vs (Fx+ - Fx-) Input Voltage	$AV=\frac{V(BURST)-VREF}{V(Fx+-Fx-)}=2.6V/Vpp$ $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ = Low			±11	%
BURSTA, BURSTB Output Offset Voltage	V(BURST) - V(VREF), $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low, V(Fx+) = V(Fx-), RCS = 38.3 kΩ, $\overline{\text{RST}}$ low			±60	mV
BURSTA - BURSTB Output Offset Voltage Match	V(BURSTA)-V(BURSTB), $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low, V(Fx+) = V(Fx-)			±15	mV
PES Pin Output Offset Voltage	V(PES) - V(VREF), $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low, V(Fx+) = V(Fx-)			±50	mV
PES Pin Output Voltage vs. Va(Fx)pp - Vb(Fx)pp	$AV=\frac{V(PES)-VREF}{Va(Fx)pp-Vb(Fx)pp}=2.6V/Vpp$			±15	%
Output Resistance BURSTA, BURSTB PES pins				20.0	Ω
HOLDA/B Charge Current		25			mA
HOLDA/B Discharge Current	$\overline{\text{RST}}$ = Low; Idis = 2.6/(RCS + 750)	-15		+15	%
	$\overline{\text{RST}}$ = High, LATCH_A/B = High			±0.5	µA
Allowable Load Resistance; BURSTA/B,PES pins	Resistor to VREF	10.0			kΩ
Allowable Load Capacitance; BURSTA/B,PES pins				20.0	pF

SERVO BURST CAPTURE CIRCUIT (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{LATCHA/B}}$ Pin Setup Time (Tds1 in Fig. 2)		150			ns
$\overline{\text{LATCHA/B}}$ Pin Hold Time, (Tds2 in Fig. 2)		150			ns
Channel A/B Discharge Current Turn On Time (Tds3 in Fig. 2)				150	ns
Channel A/B Discharge Current Turn Off Time (Tds4 in Fig. 2)				150	ns

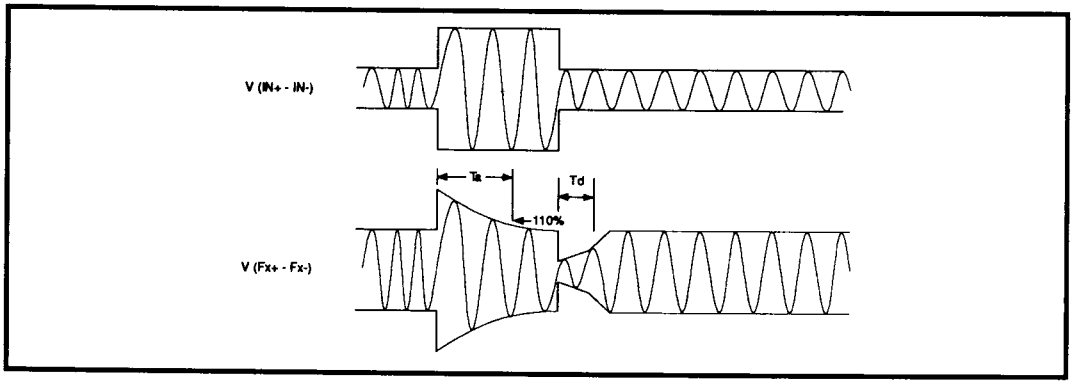


FIGURE 1: AGC Timing Diagram

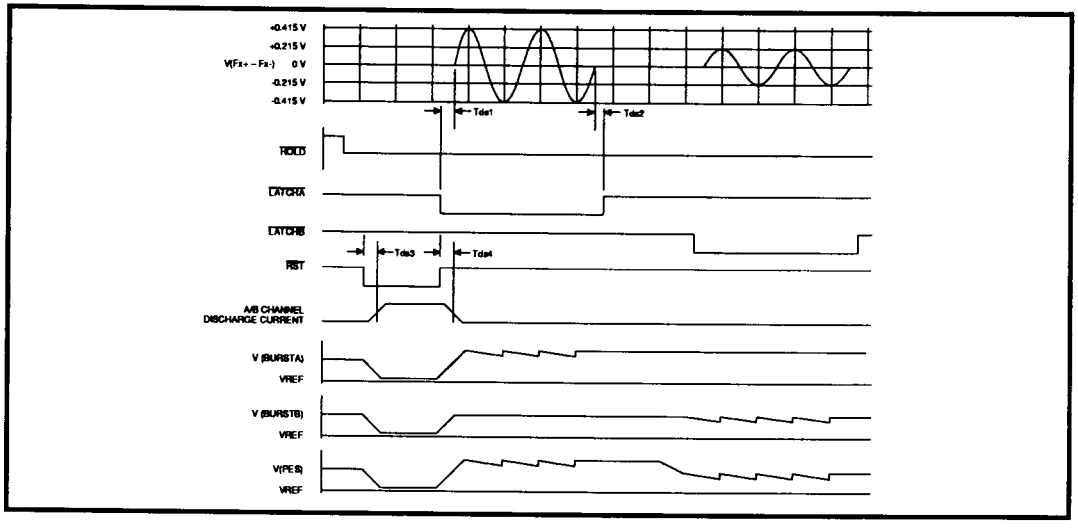


FIGURE 2: Servo Timing Diagram

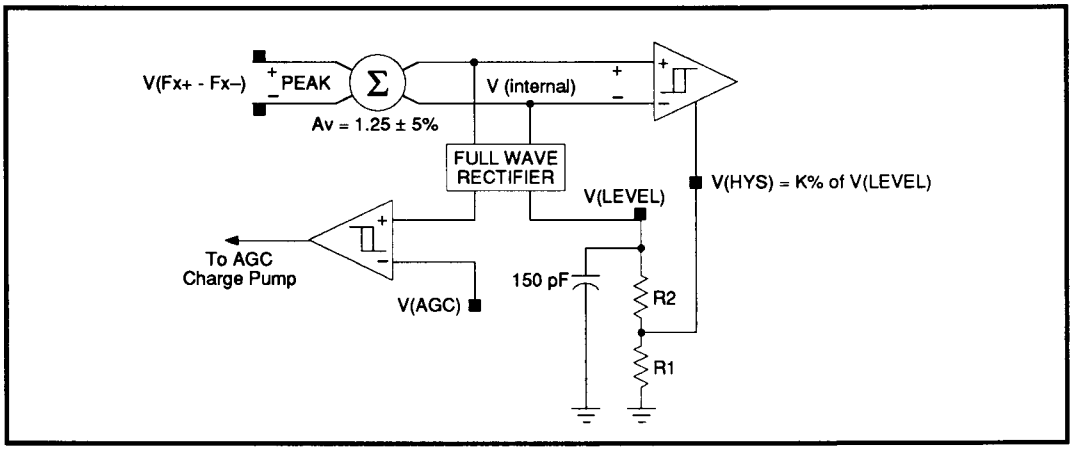


FIGURE 3: Feed Forward Mode

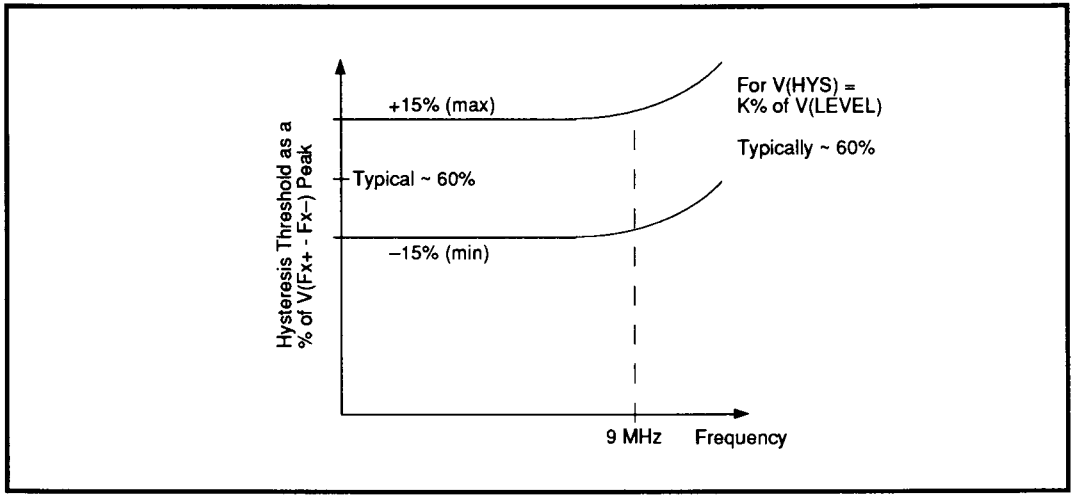


FIGURE 4: Percentage Threshold vs. Frequency

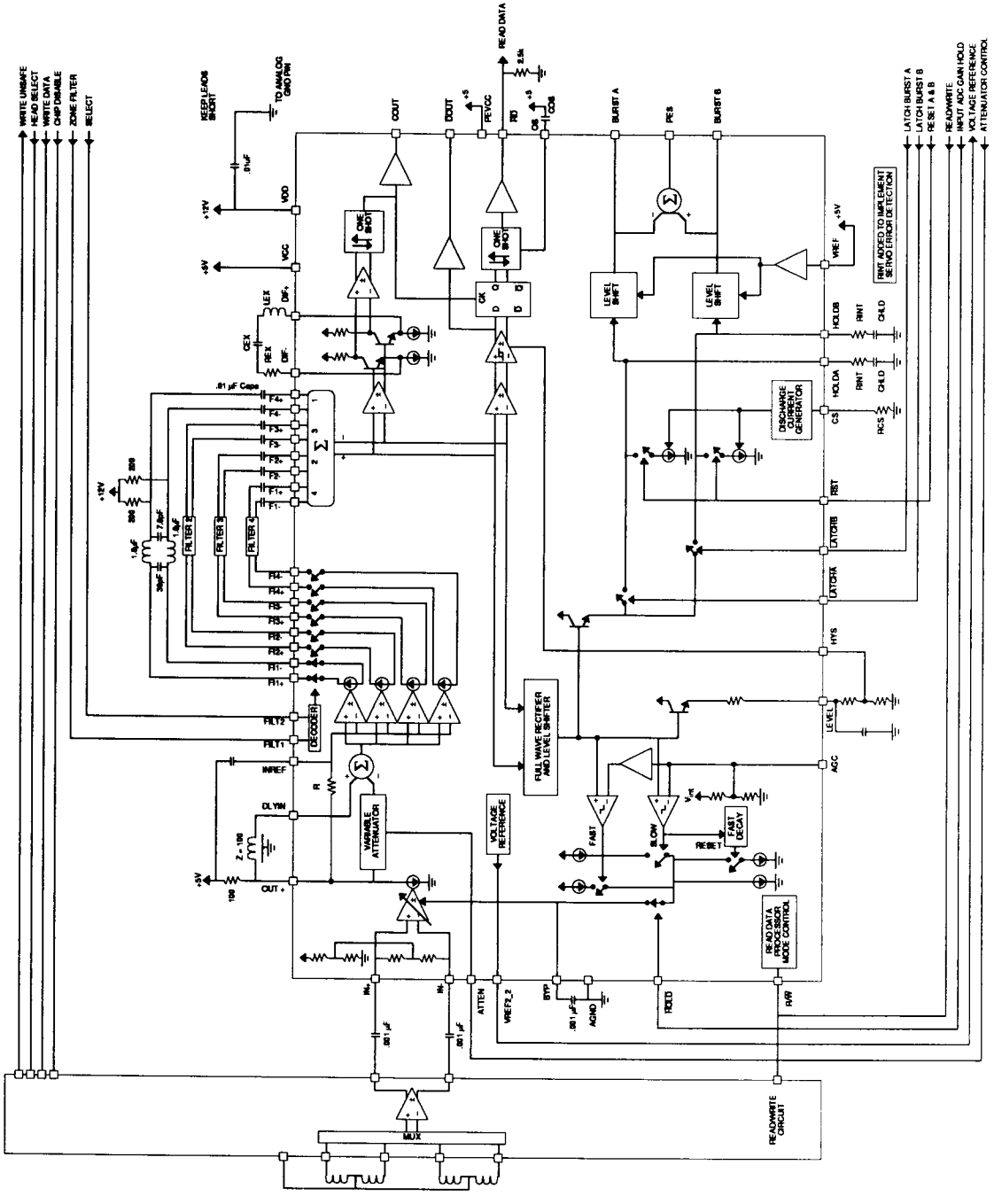


FIGURE 5: Applications Circuit Diagram

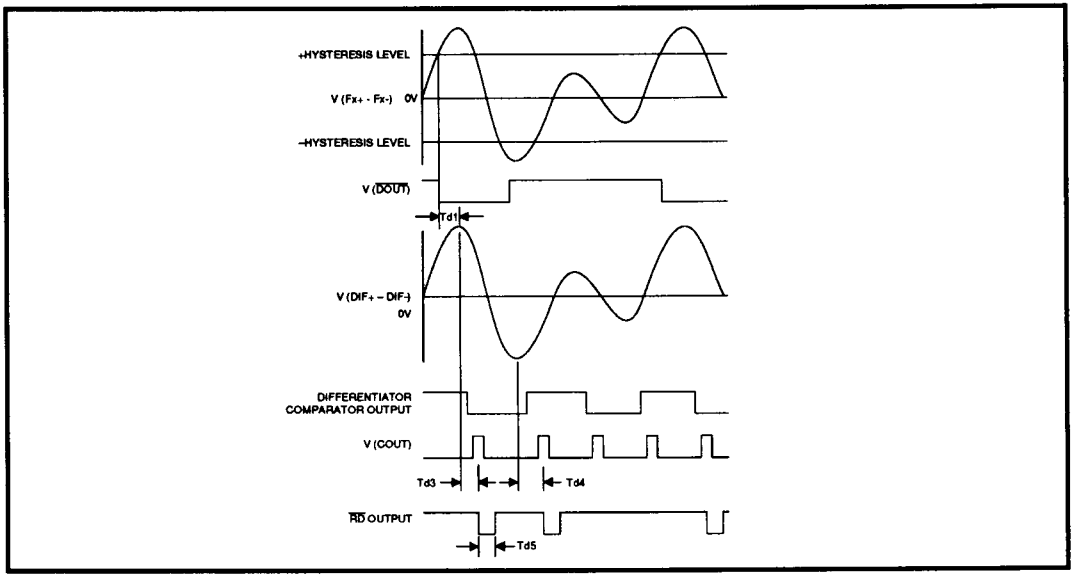


FIGURE 6: Read Mode Digital Section Timing Diagram

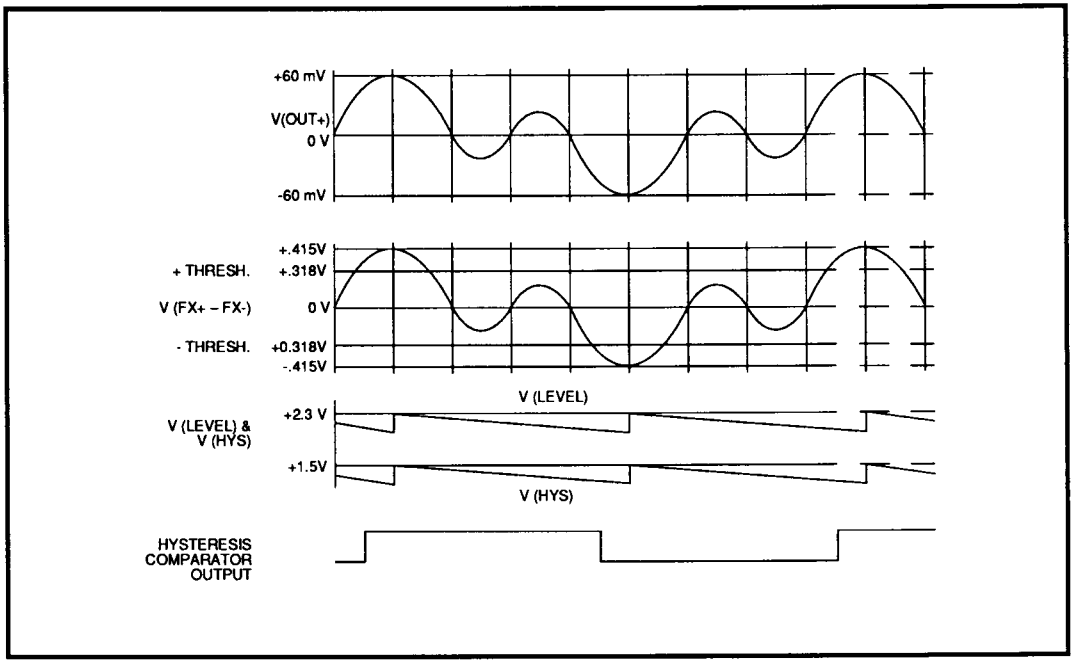


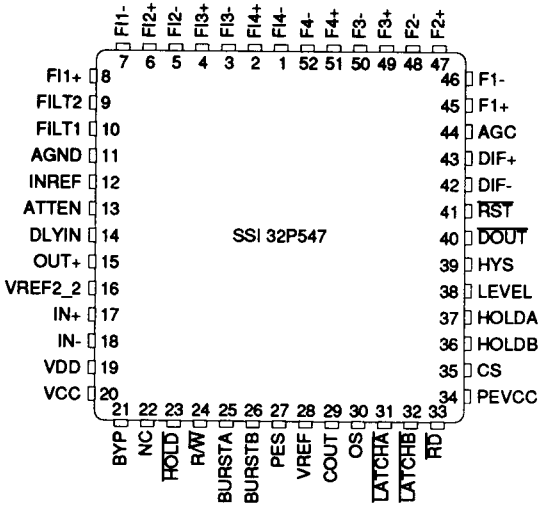
FIGURE 7: Expected Nominal Voltage Levels

PACKAGE PIN DESIGNATIONS

(Top View)

Thermal Characteristics: θjA

52-lead PLCC	55° C/W



52-Lead PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P547 52-Lead PLCC	32P547-CH	32P547-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914