M65843P,FP

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

The M65843 is a CMOS IC for generating echo to be added to the voice through a "karaoke" microphone.

It is suitable for application to the echo generator of a radio cassette player, mini component stereo set, TV etc.

Increased master clock frequency assures high-performance short delay, enabling the IC to be used for digital surround.

FEATURES

- Fixed delay time of 125msec (with external clock set at 320kHz)
- Built-in A-D, D-A converters, input/output low-pass filter, and 10K bit delay memory
- High sound quality is assured by simple system construction, due to A-D, D-A converters with ADM (Adaptive Delta Modulation) system
  - Output noise voltage : − 80dBV (typ)
  - Total harmonic distortion : 1.7 % (typ)
- Built-in mute circuit

Outline 24P4(P)

2.54mm pitch 600mil DIP
(13.0mm × 31.1mm × 3.8mm)

Outline 24P2W-A(FP)

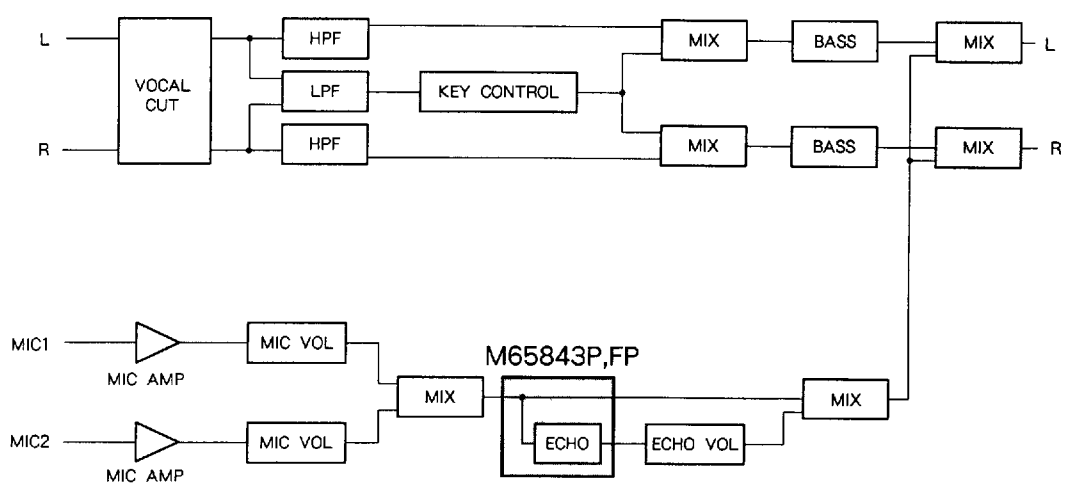
1.27mm pitch 450mil SOP
(8.4mm × 15.0mm × 2.0mm)

RECOMMENDED OPERATING CONDITIONS

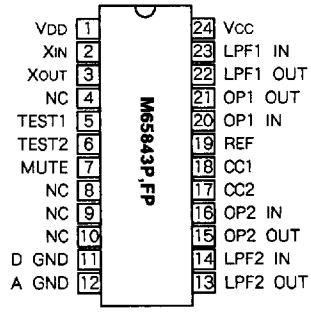
Supply voltage range ..... V_{CC}, V_{DD} = 4.5~5.5V

Rated supply voltage ..... V_{CC}, V_{DD} = 5V

SYSTEM CONFIGURATION



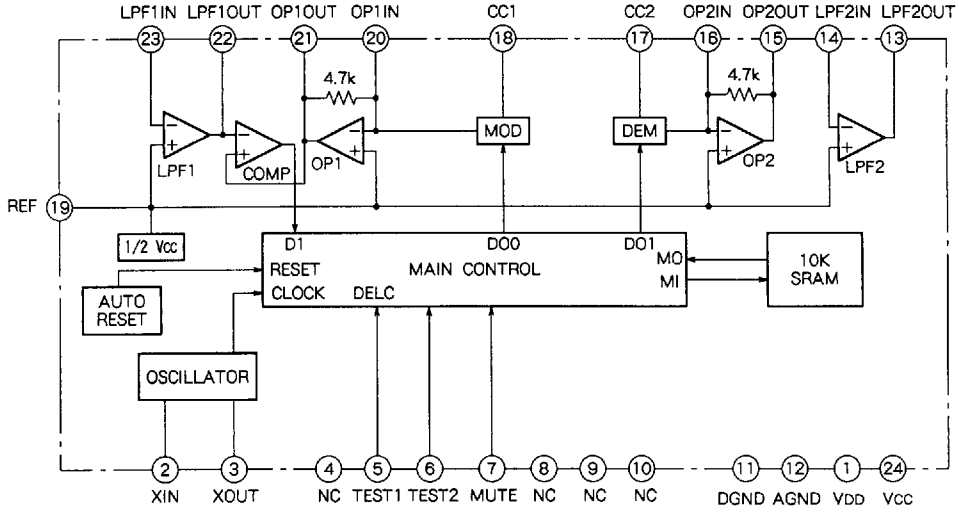
PIN CONFIGURATION



Outline 24P4(P)
24P2W-A(FP)

NC : NO CONNECTION

IC INTERNAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Name	I/O	Function
①	V_{DD}	Digital power supply	–	
②	X_{IN}	Clock generator input	I	To connect 320kHz ceramic oscillator
③	X_{OUT}	Clock generator output	O	Open when external clock is used
④	NC	No connection	–	Connection of external device is inhibited
⑤	TEST1	Test1	I	Fixed at "H"
⑥	TEST2	Test2	I	Fixed at "L"
⑦	MUTE	Mute	I	Mute control, L = Mute mode
⑧	NC	No connection	–	Connection of external device is inhibited
⑨	NC	No connection	–	Connection of external device is inhibited
⑩	NC	No connection	–	Connection of external device is inhibited
⑪	D GND	Digital GND	–	
⑫	A GND	Analog GND	–	
⑬	LPF2 OUT	Low-pass filter 2 output	O	To form output-side low-pass filter by connecting external capacitor and resistor
⑭	LPF2 IN	Low-pass filter 2 input	I	
⑮	OP2 OUT	Operational amplifier 2 output	O	To form demodulating integrator by connecting external capacitor
⑯	OP2 IN	Operational amplifier 2 input	I	
⑰	CC2	Current control 2	–	ADM control of demodulator
⑱	CC1	Current control 1	–	ADM control of modulator
⑲	REF	Reference	–	Analog reference voltage = 1/2Vcc
⑳	OP1 IN	Operational amplifier 1 input	I	To form modulating integrator by connecting external capacitor and resistor
㉑	OP1 OUT	Operational amplifier 1 output	O	
㉒	LPF1 OUT	Low-pass filter 1 output	O	To form input-side low-pass filter by connecting external capacitor and resistor
㉓	LPF1 IN	Low-pass filter 1 input	I	
㉔	Vcc	Analog power supply	–	

ABSOLUTE MAXIMUM RATINGS (Ta = 25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
Vcc	Supply voltage		6.5	V
Icc	Circuit current		100	mA
Pd	Power dissipation	M65843P	1	W
		M65843FP	0.8	
Topr	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−40∼+125	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Analog supply voltage		4.5	5	5.5	V
V_{DD}	Digital supply voltage		4.5	5	5.5	V
Vcc-V_{DD}	Vcc − V_{DD} potential difference		−0.3	0	0.3	V
fck	Clock frequency		280	320	475	kHz
V_{IH}	Input voltage ("H" level)		0.7V_{DD}	–	V_{DD}	V
V_{IL}	Input voltage ("L" level)		0	–	0.3V_{DD}	V

ELECTRICAL CHARACTERISTICS (Vcc = 5V, f = 1kHz, V_i = 100mVrms, Ta = 25℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit current	No signal input	–	13	35	mA
Gv	I/O voltage gain	R_L = 47kΩ	−2.5	0.5	3.5	dB
V_{Omax}	Max. output voltage	THD = 10%	0.7	1	–	Vrms
THD	Distortion factor	30kHz LPF	–	1.7	3.0	%
No	Output noise voltage	DIN−AUDIO	–	−80	−65	dBV
SVRR	Supply voltage reduction ratio	ΔVcc = −20dBV, f = 100Hz	–	−40	−25	dB

FUNCTION

(1) Sampling frequency fs

The sampling frequency can be calculated by the following equation :

fs = Clock frequency/4(Hz)

For clock frequency (fck) = 320kHz, the calculated sampling frequency is :

fs = 320kHz/4 = 80kHz

(2) Delay time Td

For fck = 320kHz(fs = 80kHz), the calculated delay time is :

T_d = 125msec

(3) Mute

Output can be muted by setting the MUTE terminal(⑦Pin) appropriately

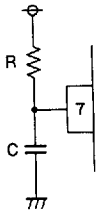
⑦MUTE	Mode
H	Normal mode
L	Mute mode

It is recommended to mute the output, as illustrated on the right, to prevent noise from being generated when power is turned ON. The muting period is determined by the resistor and capacitor connected to : pin, and calculated by the following equation :

Muting period(t mute) ≒ 0.96 × CR(sec)

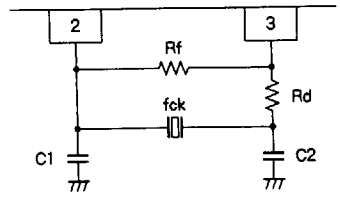
For C = 10 μF, R = 150kΩ, the calculated muting period is about 1.4sec :

t mute ≒ 0.96 × 10 μ × 150k = 1.38(sec)



(4) Clock generator

The M65843P, FP contains an oscillation buffer, so that a clock generator circuit can be formed by connecting a ceramic oscillator, resistors and capacitors as shown below.



For a ceramic oscillator with fck = 320kHz (CSB320D, manufactured by Murata Mfg. Co.), recommended resistance and capacitance values are :

Rf = 1MΩ

Rd = 6.8kΩ

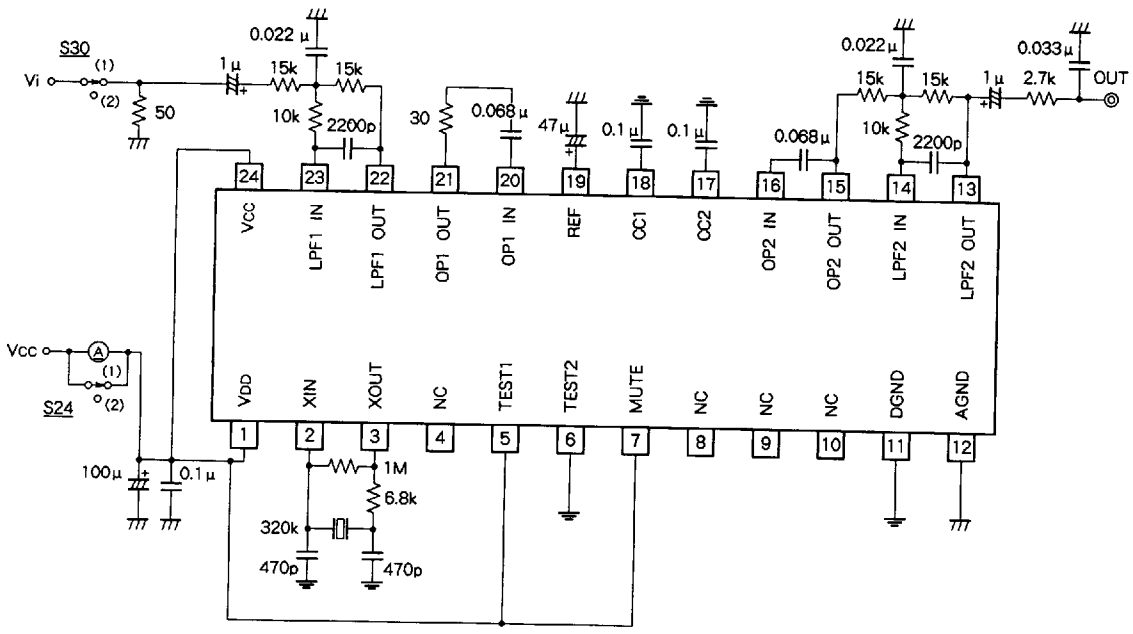
$C_1 = C_2$ = 470pF

Note that the above values vary according to the oscillator used, the oscillation frequency, and the constitutional environment of clock generator circuit (such as the capacity of substrate and wiring).

TEST CONDITIONS

Symbol	Parameter	S24	S30	Remark
Icc	Circuit current	2	2	No signal input
Gv	Voltage gain	1	1	Gv = 20log(Vo/Vi)
Td	Delay time	1	1	
Vomax	Max. output voltage	1	1	30kHzLPF, THD = 10%
THD	Total harmonic distortion factor	1	1	30kHzLPF
No	Output noise voltage	1	2	DIN AUDIO, Vi = 0mVrms
SVRR	Supply voltage reduction ratio	1	2	ΔVcc = − 20dBV, f = 100Hz

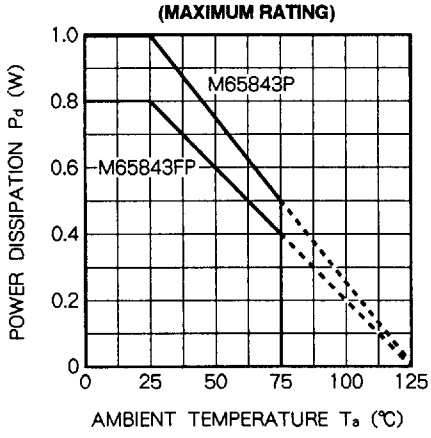
TEST CIRCUIT



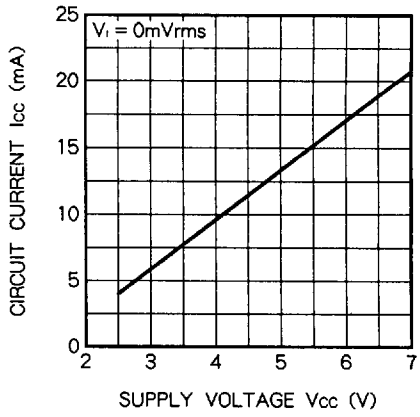
Units Resistance : Ω
Capacitance : F
⏚ : Analog GND
⏚ : Digital GND

TYPICAL CHARACTERISTICS

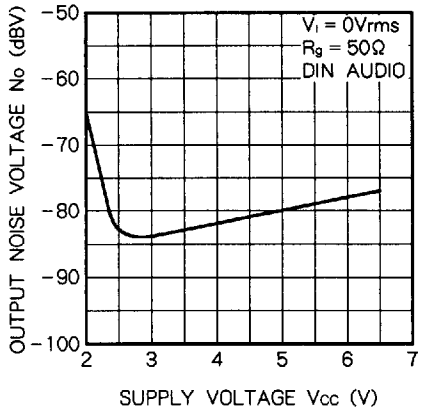
THERMAL DERATING (MAXIMUM RATING)



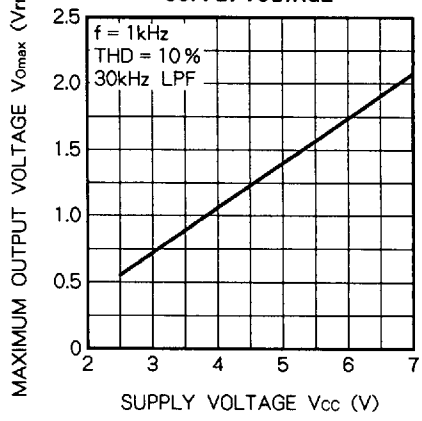
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



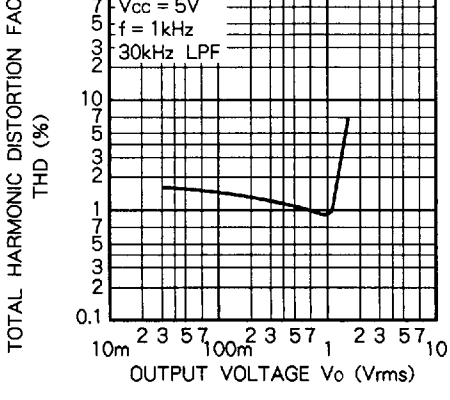
OUTPUT NOISE VOLTAGE VS. SUPPLY VOLTAGE



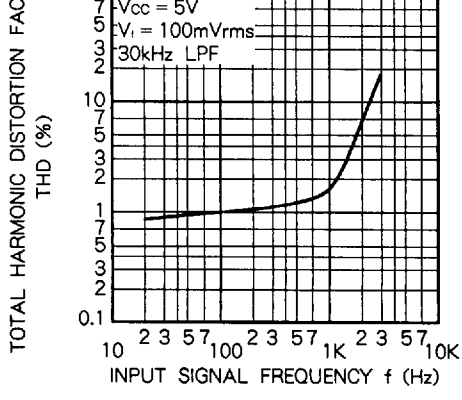
MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



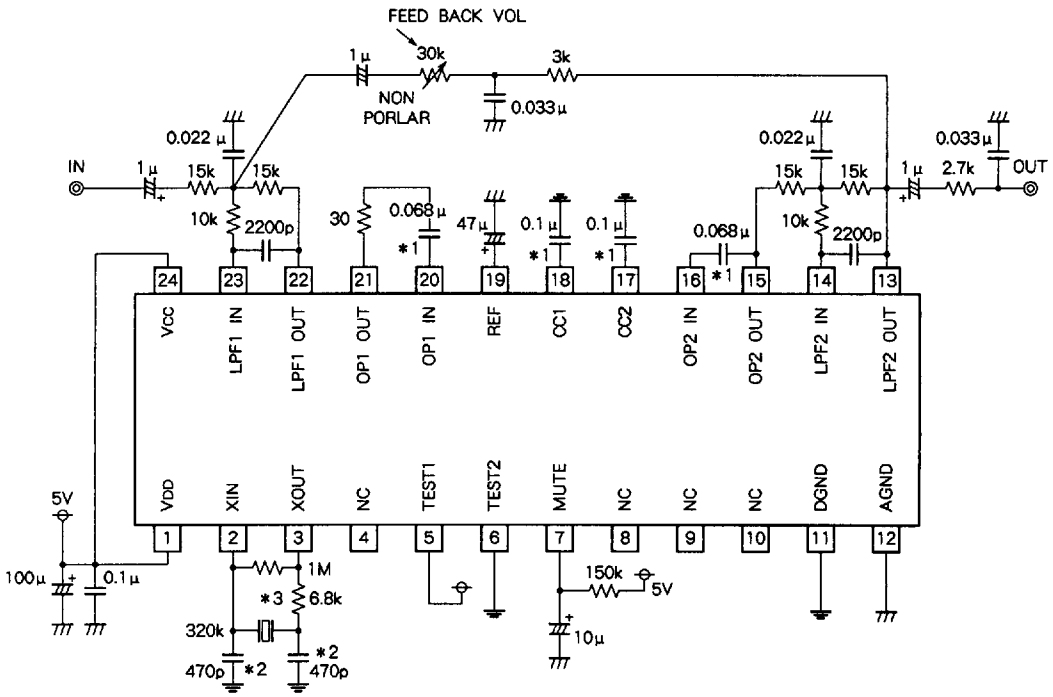
TOTAL HARMONIC DISTORTION FACTOR VS. OUTPUT VOLTAGE



TOTAL HARMONIC DISTORTION FACTOR VS. INPUT SIGNAL FREQUENCY



APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F
⏚ : Analog GND
⏚ : Digital GND

The capacitance marked * 1 shall have a relative accuracy within ± 5 %.

Note that the capacitance marked * 2 and resistance marked * 3 vary according to the oscillation frequency of ceramic oscillator, and the constitutional environment of the clock generator.