

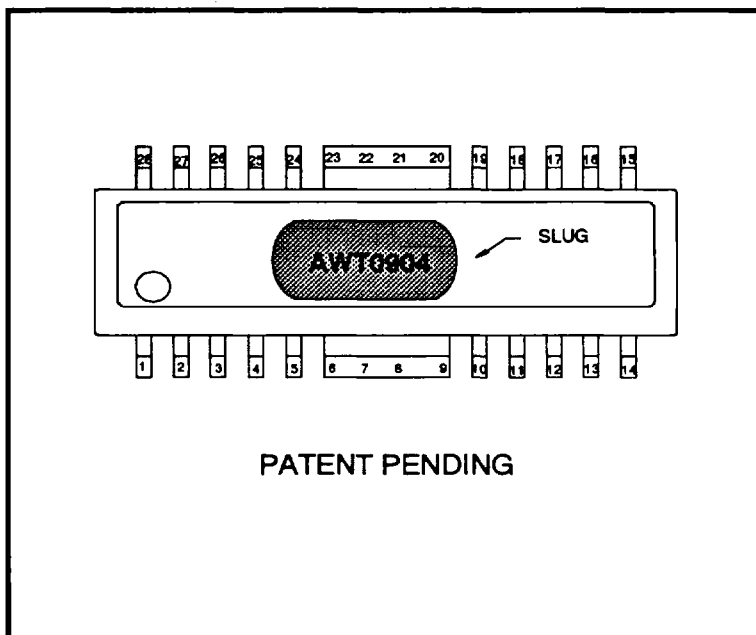
900 MHz Band GSM GaAs Power Amplifier IC

DESCRIPTION

The AWT0904X is a monolithic Power Amplifier IC suited for GSM cellular telephone Applications

FEATURES

- Single Supply
- High Output Power
- High Efficiency
- Low Harmonics
- Built-in Pulse Shaping
- Small Size
- 28 Pin SSOP Plastic Package.
- Surface Mount Package
- 50Ω Input Impedance
- Low Cost



1. Maximum Ratings

Static sensitive electronic devices. Do not operate or store near strong electrostatic, fields. Take proper ESD precautions.

Pin	Rating	Notes
Pin 2 - RFIN	+ 10 dBm max., +/- 7.5 max.	
Pin 3 - VREF	+ 5V max., 0V min.	If VREF is kept high and not pulsed, the amplifier may draw very high currents and permanent damage may occur.
Pin 4 - VDB	+7.5V max., 0V min.	
Pin 5 - VSS_IN	N/A	Do not apply voltage to this pin. If VSS_IN is not between -3V and -5V (with VGEN=4.8V), the amplifier may not work properly.

This data sheet contains technical information about product ANADIGICS is planning to introduce. The data and product specifications are subject to change prior to formal introduction. Please note : This device is NOT to be used for device qualification or production.

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Pin	Rating	Notes
Pin 11, Pin 12	N/A	Do not apply voltage to these pins.
Pin 13 - VGEN	+7.5V max., 0V min.	VGEN must be turned on before any of the drain supplies.
Pin 16 - D2	+7.5V max., 0V min.	
Pin 19 - D3B	+7.5V max., 0V min.	
Pin 24- D3A	+7.5V max., 0V min.	
Pin 27 - D1	+7.5V max., 0V min.	

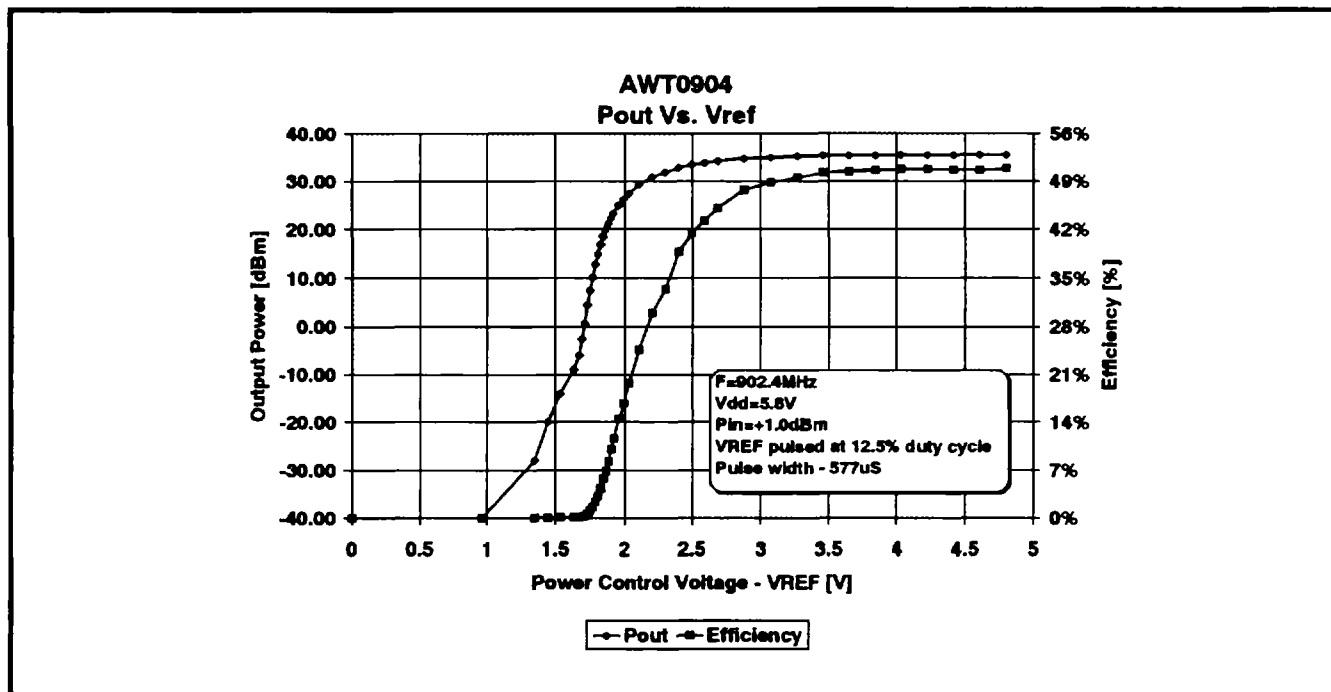
2. ELECTRICAL CHARACTERISTICS:

(Pin = 1dBm, Vds = + 5.8Vdc, Vgen = + 4.8 Vdc, Pulsed @ 577 μ S/12.5% Duty Cycle, Tc = 25°C, 50 Ω Input & 50 Ω external output match)

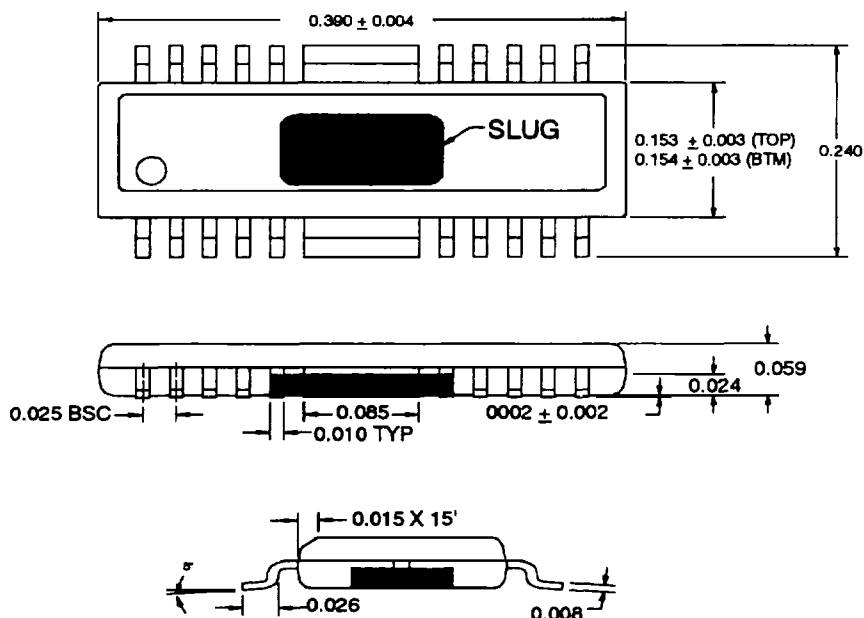
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	PARAMETER
Frequency	fo	890		915	MHz
Power Output	Pout		35		dBm
Power Added Efficiency	PAE		50		%
Gain			33		dB
Harmonics (@ 35dBm)	2fo - 4fo		- 35		dBc
Stability: -80 dBc, all spurious outputs relative to desired signal			6:1		VSWR load, all phase angles, (Pout <= 35dBm) Vds = +5.8.0V, Zs = 50 Ω
Input Return Loss	Rtn _{in}		12		dB
Operating Range	Tc	- 20		+ 70	°C
DC/DC Converter Current	Igen		3		mA
Pulse Control	I _{ref}		3		mA

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3. DATA



4. Case Outline and Pin Description



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Pin	Signal	Description
1	GND	RF and DC Ground
2	RFIN	RF power input,DC blocked
3	VREF	Output Power control,Should be set to level that corresponds to the desired output power . Pulse control voltage (Vref, 0 to 4V)
4	VDB	Bias circuit Supply (+5.8V, 2-3 ma)
5	VSS_IN	Negative Supply (-4V) generated by the dc/dc converter
6,7,8,9	GND	RF and DC Ground (The "Batwing")
10	VSS_OUT	The output of the dc/dc converter providing the negative voltage
11,12		Pump capacitor (C5) which is part of the dc/dc converter circuit.
13	V GEN	DC/DC converter positive supply
14	VGENGND	AC and DC ground for the dc/dc converter .If possible should be grounded through a separate via hole .
15	GND	RFandDC ground.
16	D2	The open drain of the second amplifier stage
17	GND	RF and DC Ground
18	N/C	Not Connected
19	D3B	3rd stage drain supply (5.8V) and RF out
20,21,22,23	GND	RF and DC ground (the "BATWING")
24	D3A	3rd stage drain supply (5.8V) and RF out
25	N/C	Not Connected
26	GND	RF and DC ground
27	D1	1st stage drain supply (5.8V)
28	GND	RF and DC Ground

5. Recommended Operating Procedure on the Evaluation Board

Power Up

- A. Begin by setting all power supplies to zero volts, and input power to zero dBm.
- B. Make sure that the input RF power is turned off.
- C. Turn on VGEN (Pin 13) to + 4.8V
- D. Check the voltage @ VSS_IN (pin 5) to see if it is between -5v and -3v if voltage is not check the pin alignment.
- E. Turn on VD1(Pin 27), VD2(Pin 16), VD3(Pins 19 and 24) and VDB (Pin 4) which are tied together on the fixture, and set to +5.8V. Little drain current should be flowing at this time (I_{dd} < 5 mA).
- F. Turn RF on and adjust input power to 1.0 dBm.

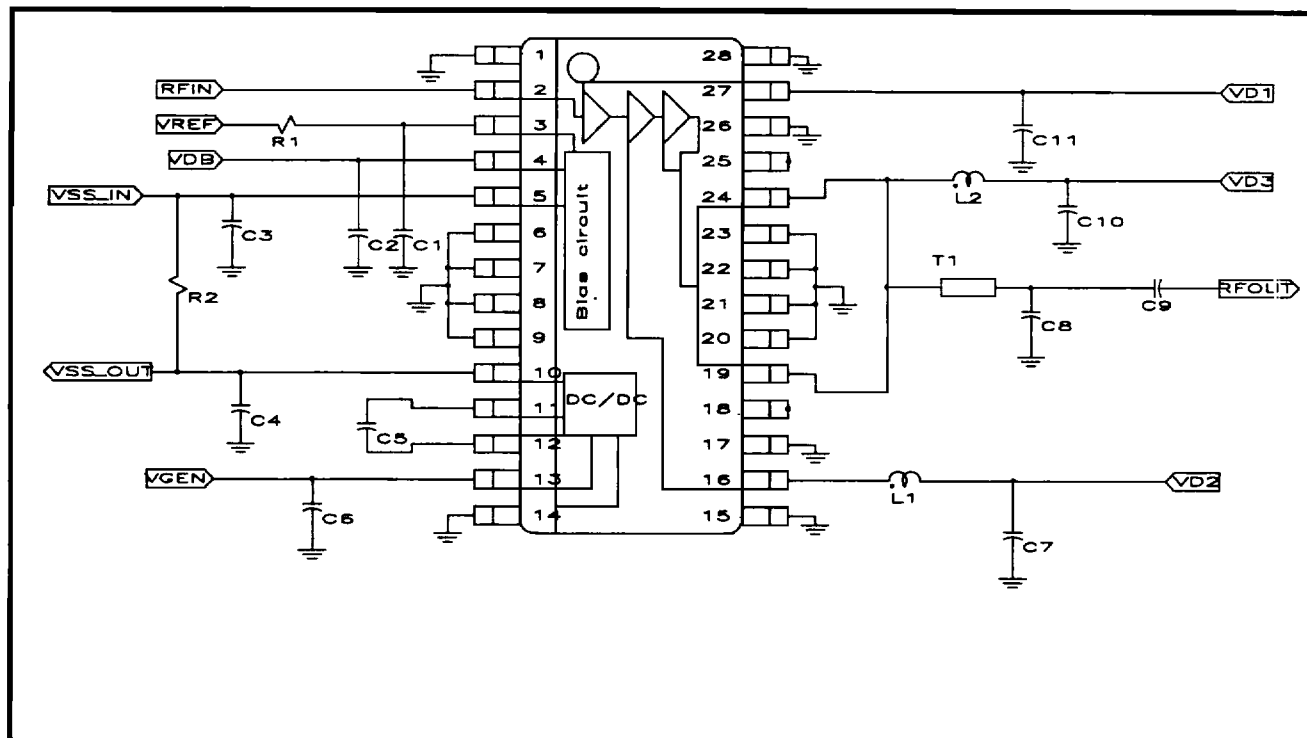
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- G. Turn VREF on using the pulsed scheme of GSM. Adjust Pulse VREF to desired output power (<=35 dBm). No lower than 0V and no higher than +4V. Use an oscilloscope to measure VREF on the VREF package pin (3) rather than using the display of the pulse generator. The reason being the pulse generator may have a 50Ω output impedance while the impedance of VREF pin is high. This causes the voltage on VREF pin to be almost twice as high as the readout on the pulse generator.

Power Down

To power down the device follow the above procedure in reverse order .

6. AWT0904 TEST CIRCUIT



Component	Value	Type
C1	Not Used	
C2	33nF	0402
C3, C4, C6	1uF	0805
C5	100nF	0805
C7, C10, C11	470pF	0402
C8	7pF	0805
C9	470pF	0805
L1	6.8n	0603
L2	18n	Coil Craft 1008
R1	200	0603
R2	10	0603
T1	Z0=25Ω	Microstrip