

NEC

MOS INTEGRATED CIRCUIT

μ PD42S16400L, 4216400L, 42S17400L, 4217400L

3.3 V OPERATION 16 M-BIT DYNAMIC RAM 4 M-WORD BY 4-BIT, FAST PAGE MODE

Description

The μ PD42S16400L, 4216400L, 42S17400L, 4217400L are 4,194,304 words by 4 bits CMOS dynamic RAMs. The fast page mode capability realize high speed access and low power consumption.

These differ in refresh cycles and the μ PD42S16400L, 42S17400L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh.

These are packaged in 26-pin plastic TSOP(II) and 26-pin plastic SOJ.

Features

- 4,194,304 words by 4 bits organization
- Fast page mode
- Single +3.3 V \pm 0.3 V power supply
- Fast access and cycle time

| Part number | Power consumption Active (MAX.) | Access time (MAX.) | R/W cycle time (MIN.) | Fast page mode cycle time (MIM.) |
|-------------------------------------|------------------------------------|-----------------------|--------------------------|-------------------------------------|
| μ PD42S16400L-A50, 4216400L-A50 | 550 mW | 50 ns | 90 ns | 35 ns |
| μ PD42S17400L-A50, 4217400L-A50 | 660 mW | | | |
| μ PD42S16400L-A60, 4216400L-A60 | 288 mW | 60 ns | 110 ns | 40 ns |
| μ PD42S17400L-A60, 4217400L-A60 | 360 mW | | | |
| μ PD42S16400L-A70, 4216400L-A70 | 252 mW | 70 ns | 130 ns | 45 ns |
| μ PD42S17400L-A70, 4217400L-A70 | 324 mW | | | |
| μ PD42S16400L-A80, 4216400L-A80 | 216 mW | 80 ns | 150 ns | 50 ns |
| μ PD42S17400L-A80, 4217400L-A80 | 288 mW | | | |

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- The μ PD42S16400L, μ PD42S17400L can execute $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh

| Part number | Refresh cycle | Refresh | Power consumption at standby (MAX.) |
|-------------------|---------------------|---|--|
| μ PD42S16400L | 4,096 cycles/128 ms | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh | 0.54 mW (CMOS level input) |
| μ PD42S17400L | 2,048 cycles/128 ms | | |
| μ PD4216400L | 4,096 cycles/64 ms | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ only refresh, Hidden refresh | 1.8 mW (CMOS level input) |
| μ PD4217400L | 2,048 cycles/32 ms | | |

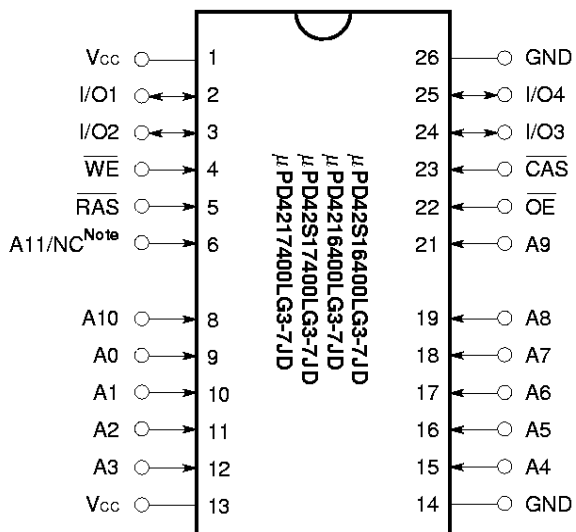
The information in this document is subject to change without notice.

★ Ordering Information

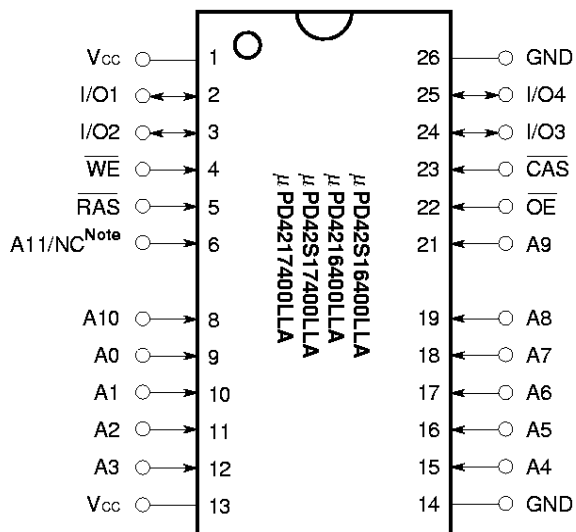
| Part number | Access time (MAX.) | Package | Refresh |
|------------------------|--------------------|---------------------------------------|---|
| μPD42S16400LG3-A50-7JD | 50 ns | 26-pin plastic TSOP (II) (300 mil) | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh |
| μPD42S17400LG3-A50-7JD | | | |
| μPD42S16400LG3-A60-7JD | 60 ns | | |
| μPD42S17400LG3-A60-7JD | | | |
| μPD42S16400LG3-A70-7JD | 70 ns | | |
| μPD42S17400LG3-A70-7JD | | | |
| μPD42S16400LG3-A80-7JD | 80 ns | | |
| μPD42S17400LG3-A80-7JD | | | |
| μPD42S16400LLA-A50 | 50 ns | 26-pin plastic SOJ (300 mil) | |
| μPD42S17400LLA-A50 | | | |
| μPD42S16400LLA-A60 | 60 ns | | |
| μPD42S17400LLA-A60 | | | |
| μPD42S16400LLA-A70 | 70 ns | | |
| μPD42S17400LLA-A70 | | | |
| μPD42S16400LLA-A80 | 80 ns | | |
| μPD42S17400LLA-A80 | | | |
| μPD4216400LG3-A50-7JD | 50 ns | 26-pin plastic TSOP (II) (300 mil) | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh $\overline{\text{RAS}}$ only refresh Hidden refresh |
| μPD4217400LG3-A50-7JD | | | |
| μPD4216400LG3-A60-7JD | 60 ns | | |
| μPD4217400LG3-A60-7JD | | | |
| μPD4216400LG3-A70-7JD | 70 ns | | |
| μPD4217400LG3-A70-7JD | | | |
| μPD4216400LG3-A80-7JD | 80 ns | | |
| μPD4217400LG3-A80-7JD | | | |
| μPD4216400LLA-A50 | 50 ns | 26-pin plastic SOJ (300 mil) | |
| μPD4217400LLA-A50 | | | |
| μPD4216400LLA-A60 | 60 ns | | |
| μPD4217400LLA-A60 | | | |
| μPD4216400LLA-A70 | 70 ns | | |
| μPD4217400LLA-A70 | | | |
| μPD4216400LLA-A80 | 80 ns | | |
| μPD4217400LLA-A80 | | | |

Pin Configurations (Marking Side)

26-pin Plastic TSOP (II) (300 mil)



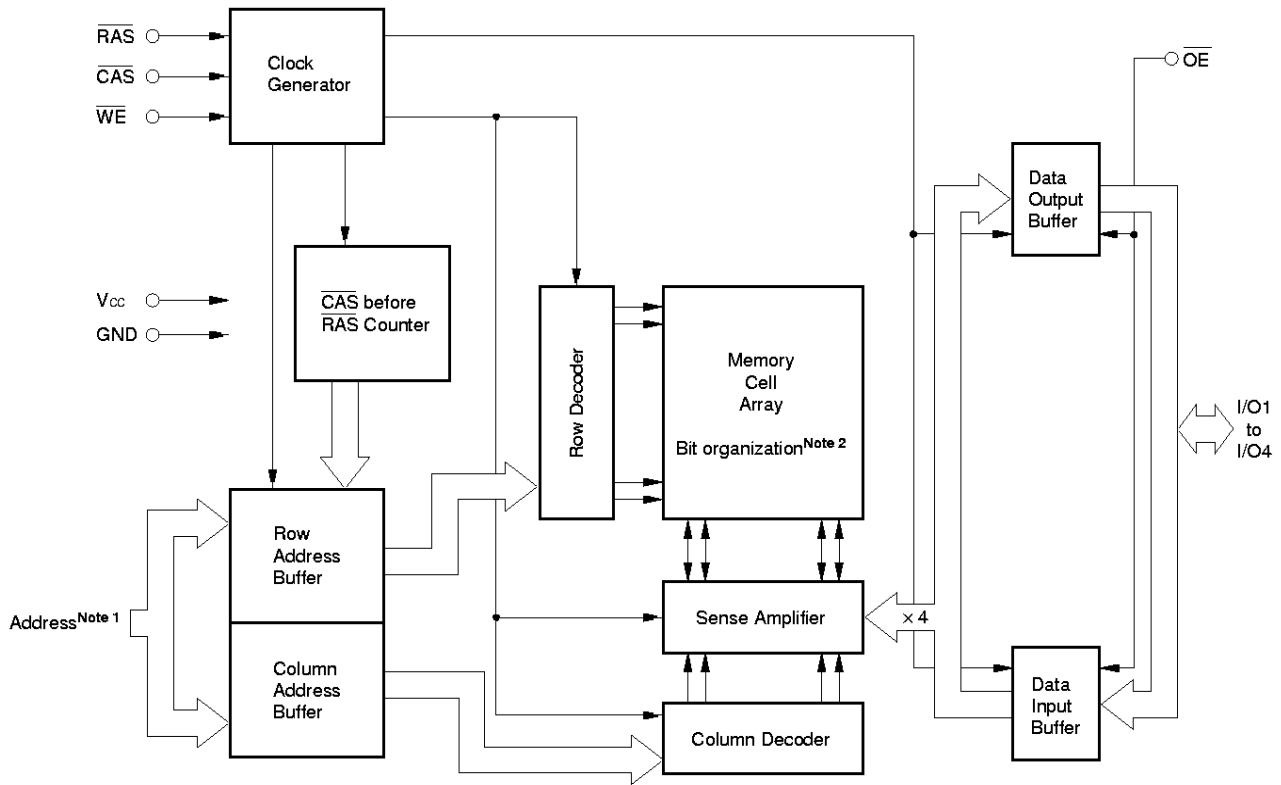
26-pin Plastic SOJ (300 mil)



Note A11 ... μPD42S16400L, 4216400L
 NC ... μPD42S17400L, 4217400L

- A0 to A11 : Address Inputs
- I/O1 to I/O4 : Data Inputs/Outputs
- RAS : Row Address Strobe
- CAS : Column Address Strobe
- WE : Write Enable
- OE : Output Enable
- V_{CC} : Power Supply
- GND : Ground
- NC : No Connection

Block Diagram



Notes 1.

| Part number | Row address | Column address |
|------------------------|-------------|----------------|
| μPD42S16400L, 4216400L | A0 - A11 | A0 - A9 |
| μPD42S17400L, 4217400L | A0 - A10 | A0 - A10 |

2. μPD42S16400L, 4216400L ... 4,096 × 1,024 × 4 μPD42S17400L, 4217400L ... 2,048 × 2,048 × 4

Input/Output Pin Functions

The μPD42S16400L, 4216400L, 42S17400L, 4217400L have input pins \overline{RAS} , \overline{CAS} , \overline{WE} , \overline{OE} , Address^{Note} and input/output pins I/O1 to I/O4.

| Pin name | Input/Output | Function |
|--|--------------|--|
| \overline{RAS} (Row address strobe) | Input | \overline{RAS} activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • \overline{CAS} before \overline{RAS} refresh |
| \overline{CAS} (Column address strobe) | Input | \overline{CAS} activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier. |
| A0 to A _x ^{Note} (Address inputs) | Input | Address bus. Input total 22-bit of address signal, upper bits and lower bits ^{Note} in sequence (address multiplex method). Therefore, one word is selected from 4,194,304-word by 4-bit memory cell array. In actual operation, latch row address by specifying row address and activating \overline{RAS} . Then, switch the address bus to column address and activate \overline{CAS} . Each address is taken into the device when \overline{RAS} and \overline{CAS} are activated. Therefore, the address input setup time (t_{ASR} , t_{ASC}) and hold time (t_{RAH} , t_{CAH}) are specified for the activation of \overline{RAS} and \overline{CAS} . |
| \overline{WE} (Write enable) | Input | Write control signal. Write operation is executed by activating \overline{RAS} , \overline{CAS} and \overline{WE} . |
| \overline{OE} (Output enable) | Input | Read control signal. Read operation can be executed by activating \overline{RAS} , \overline{CAS} and \overline{OE} . If \overline{WE} is activated during read operation, \overline{OE} is to be ineffective in the device. Therefore, read operation cannot be executed. |
| I/O1 to I/O4 (Data inputs/outputs) | Input/Output | 4-bit data bus. I/O1 to I/O4 are used to input/output data. |

Note

| Part number | Address inputs | Upper bits | Lower bits |
|------------------------|----------------|------------|------------|
| μPD42S16400L, 4216400L | A0 - A11 | 12 bits | 10 bits |
| μPD42S17400L, 4217400L | A0 - A10 | 11 bits | 11 bits |

Electrical Specifications

- All voltages are referenced to GND.
- After power up ($V_{CC} \geq V_{CC(MIN)}$), wait more than 100 μs (\overline{RAS} , \overline{CAS} inactive) and then, execute eight \overline{CAS} before \overline{RAS} or \overline{RAS} only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|------------------------------------|-----------|-----------|--------------|------|
| Voltage on any pin relative to GND | V_T | | -0.5 to +4.6 | V |
| Supply voltage | V_{CC} | | -0.5 to +4.6 | V |
| Output current | I_o | | 20 | mA |
| Power dissipation | P_D | | 1 | W |
| Operating ambient temperature | T_A | | 0 to +70 | °C |
| Storage temperature | T_{stg} | | -55 to +125 | °C |

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|-------------------------------|----------|-----------|------|------|----------------|------|
| Supply voltage | V_{CC} | | 3.0 | 3.3 | 3.6 | V |
| High level input voltage | V_{IH} | | 2.0 | | $V_{CC} + 0.3$ | V |
| Low level input voltage | V_{IL} | | -0.3 | | +0.8 | V |
| Operating ambient temperature | T_A | | 0 | | 70 | °C |

Capacitance ($T_A = 25\text{ °C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Test condition | MIN. | TYP. | MAX. | Unit |
|-------------------------------|-----------|---|------|------|------|------|
| Input capacitance | C_{I1} | Address | | | 5 | pF |
| | C_{I2} | \overline{RAS} , \overline{CAS} , \overline{WE} , \overline{OE} | | | 7 | |
| Data input/output capacitance | $C_{I/O}$ | I/O | | | 7 | pF |

★ DC Characteristics (Recommended operating conditions unless otherwise noted)
[μPD42S16400L, 4216400L]

| Parameter | | Symbol | Test condition | MIN. | MAX. | Unit | Notes |
|--|--------------|-------------------|---|--------------------------------------|------|------|------------|
| Operating current | | I _{CC1} | $\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | 100 | mA | 1, 2, 3 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | 80 | | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | 70 | | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | 60 | | |
| Standby current | μPD42S16400L | I _{CC2} | $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_{\text{O}} = 0 \text{ mA}$ | | 0.5 | mA | |
| | | | | | 0.15 | | |
| | μPD4216400L | | | | 2.0 | | |
| | | | | | 0.5 | | |
| RAS only refresh current | | I _{CC3} | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}(\text{MIN.})$ $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | 100 | mA | 1, 2, 3, 4 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | 80 | | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | 70 | | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | 60 | | |
| Operating current (Fast page mode) | | I _{CC4} | $\overline{\text{RAS}} \leq V_{\text{IL}}(\text{MAX.}), \overline{\text{CAS}}$ cycling $t_{\text{PC}} = t_{\text{PC}}(\text{MIN.}), I_{\text{O}} = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | 80 | mA | 1, 2, 5 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | 70 | | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | 60 | | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | 50 | | |
| CAS before RAS refresh current | | I _{CC5} | $\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}}(\text{MIN.})$ $I_{\text{O}} = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | 100 | mA | 1, 2 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | 80 | | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | 70 | | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | 60 | | |
| CAS before RAS long refresh current (4,096 cycles / 128 ms, only for the μPD42S16400L) | | I _{CC6} | $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh : $t_{\text{RC}} = 31.3 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ $I_{\text{O}} = 0 \text{ mA}$ | $t_{\text{RAS}} \leq 300 \text{ ns}$ | 450 | μA | 1, 2 |
| | | | | $t_{\text{RAS}} \leq 1 \mu\text{s}$ | 500 | μA | 1, 2 |
| CAS before RAS self refresh current (only for the μPD42S16400L) | | I _{CC7} | $\overline{\text{RAS}}, \overline{\text{CAS}}$: $t_{\text{RAS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}}(\text{MAX.})$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_{\text{O}} = 0 \text{ mA}$ | | 200 | μA | 2 |
| Input leakage current | | I _{I(L)} | $V_{\text{I}} = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V | -5 | +5 | μA | |
| Output leakage current | | I _{O(L)} | $V_{\text{O}} = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z) | -5 | +5 | μA | |
| High level output voltage | | V _{OH} | $I_{\text{O}} = -2.0 \text{ mA}$ | 2.4 | | V | |
| Low level output voltage | | V _{OL} | $I_{\text{O}} = +2.0 \text{ mA}$ | | 0.4 | V | |

[μ PD42S17400L, 4217400L]

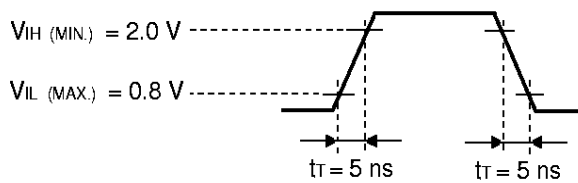
| Parameter | | Symbol | Test condition | MIN. | MAX. | Unit | Notes |
|---|-------------------|-------------------|---|--------------------------------------|------|---------------|-----------------------|
| Operating current | | I _{CC1} | $\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN})}$ $I_o = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | | 120 | mA 1, 2, 3 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | | 100 | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | | 90 | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | | 80 | |
| Standby current | μ PD42S17400L | I _{CC2} | $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN})}, I_o = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN})}, I_o = 0 \text{ mA}$ $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}, I_o = 0 \text{ mA}$ | | | 0.5 | mA |
| | μ PD4217400L | | | | | 0.15 | |
| | | | | | | 2.0 | |
| | | | | | | 0.5 | |
| RAS only refresh current | | I _{CC3} | $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} \geq V_{\text{IH}(\text{MIN})}$ $t_{\text{RC}} = t_{\text{RC}(\text{MIN})}, I_o = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | | 120 | mA 1, 2, 3, 4 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | | 100 | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | | 90 | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | | 80 | |
| Operating current (Fast page mode) | | I _{CC4} | $\overline{\text{RAS}} \leq V_{\text{IL}(\text{MAX})}, \overline{\text{CAS}}$ cycling $t_{\text{PC}} = t_{\text{PC}(\text{MIN})}, I_o = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | | 80 | mA 1, 2, 5 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | | 70 | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | | 60 | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | | 50 | |
| CAS before RAS refresh current | | I _{CC5} | $\overline{\text{RAS}}$ cycling $t_{\text{RC}} = t_{\text{RC}(\text{MIN})}$ $I_o = 0 \text{ mA}$ | $t_{\text{RAC}} = 50 \text{ ns}$ | | 120 | mA 1, 2 |
| | | | | $t_{\text{RAC}} = 60 \text{ ns}$ | | 100 | |
| | | | | $t_{\text{RAC}} = 70 \text{ ns}$ | | 90 | |
| | | | | $t_{\text{RAC}} = 80 \text{ ns}$ | | 80 | |
| CAS before RAS long refresh current (2,048 cycles / 128 ms, only for the μ PD42S17400L) | | I _{CC6} | CAS before RAS refresh : $t_{\text{RC}} = 62.5 \mu\text{s}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$: $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ Standby : $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{\text{CC}} - 0.2 \text{ V}$ Address : V_{IH} or V_{IL} $\overline{\text{WE}}, \overline{\text{OE}}: V_{\text{IH}}$ $I_o = 0 \text{ mA}$ | $t_{\text{RAS}} \leq 300 \text{ ns}$ | | 400 | μA 1, 2 |
| | | | | $t_{\text{RAS}} \leq 1 \mu\text{s}$ | | 450 | μA 1, 2 |
| CAS before RAS self refresh current (only for the μ PD42S17400L) | | I _{CC7} | $\overline{\text{RAS}}, \overline{\text{CAS}}$: $t_{\text{RASS}} = 5 \text{ ms}$ $V_{\text{CC}} - 0.2 \text{ V} \leq V_{\text{IH}} \leq V_{\text{IH}(\text{MAX})}$ $0 \text{ V} \leq V_{\text{IL}} \leq 0.2 \text{ V}$ $I_o = 0 \text{ mA}$ | | | 200 | μA 2 |
| Input leakage current | | I _{I(L)} | $V_i = 0 \text{ to } 3.6 \text{ V}$ All other pins not under test = 0 V | -5 | +5 | μA | |
| Output leakage current | | I _{O(L)} | $V_o = 0 \text{ to } 3.6 \text{ V}$ Output is disabled (Hi-Z) | -5 | +5 | μA | |
| High level output voltage | | V _{OH} | $I_o = -2.0 \text{ mA}$ | 2.4 | | V | |
| Low level output voltage | | V _{OL} | $I_o = +2.0 \text{ mA}$ | | 0.4 | V | |

- Notes**
1. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC5} and I_{CC6} depend on cycle rates (t_{RC} and t_{PC}).
 2. Specified values are obtained with outputs unloaded.
 3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS} \leq V_{IL(MAX.)}$ and $\overline{CAS} \geq V_{IH(MIN.)}$.
 4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
 5. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast page cycle.

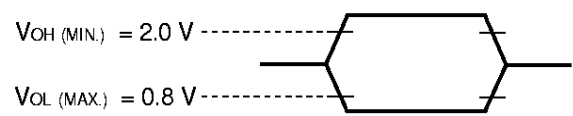
★ **AC Characteristics (Recommended Operating Conditions unless otherwise noted)**

AC Characteristics Test Conditions

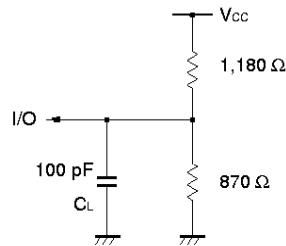
(1) Input timing specification



(2) Output timing specification



(3) Output load condition



Common to Read, Write, Read Modify Write Cycle

| Parameter | Symbol | t _{RAC} = 50 ns | | t _{RAC} = 60 ns | | t _{RAC} = 70 ns | | t _{RAC} = 80 ns | | Unit | Notes | |
|--|-------------------------|--------------------------|--------|--------------------------|--------|--------------------------|--------|--------------------------|--------|------|-------|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | | |
| Read / Write cycle time | t _{RC} | 90 | – | 110 | – | 130 | – | 150 | – | ns | | |
| $\overline{\text{RAS}}$ precharge time | t _{RP} | 30 | – | 40 | – | 50 | – | 60 | – | ns | | |
| $\overline{\text{CAS}}$ precharge time | t _{CPN} | 8 | – | 10 | – | 10 | – | 10 | – | ns | | |
| $\overline{\text{RAS}}$ pulse width | t _{RAS} | 50 | 10,000 | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | ns | 1 | |
| $\overline{\text{CAS}}$ pulse width | t _{CAS} | 13 | 10,000 | 15 | 10,000 | 18 | 10,000 | 20 | 10,000 | ns | | |
| $\overline{\text{RAS}}$ hold time | t _{RSH} | 13 | – | 15 | – | 18 | – | 20 | – | ns | | |
| $\overline{\text{CAS}}$ hold time | t _{CSH} | 50 | – | 60 | – | 70 | – | 80 | – | ns | | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | t _{RCD} | 18 | 37 | 20 | 45 | 20 | 52 | 25 | 60 | ns | 2 | |
| $\overline{\text{RAS}}$ to column address delay time | t _{RAD} | 13 | 25 | 15 | 30 | 15 | 35 | 17 | 40 | ns | 2 | |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | t _{CRP} | 5 | – | 5 | – | 5 | – | 5 | – | ns | 3 | |
| Row address setup time | t _{ASR} | 0 | – | 0 | – | 0 | – | 0 | – | ns | | |
| Row address hold time | t _{RAH} | 8 | – | 10 | – | 10 | – | 12 | – | ns | | |
| Column address setup time | t _{ASC} | 0 | – | 0 | – | 0 | – | 0 | – | ns | | |
| Column address hold time | t _{CAH} | 13 | – | 15 | – | 15 | – | 15 | – | ns | | |
| $\overline{\text{OE}}$ lead time referenced to $\overline{\text{RAS}}$ | t _{OES} | 0 | – | 0 | – | 0 | – | 0 | – | ns | | |
| $\overline{\text{CAS}}$ to data setup time | t _{CLZ} | 0 | – | 0 | – | 0 | – | 0 | – | ns | | |
| $\overline{\text{OE}}$ to data setup time | t _{OLZ} | 0 | – | 0 | – | 0 | – | 0 | – | ns | | |
| $\overline{\text{OE}}$ to data delay time | t _{OED} | 10 | – | 15 | – | 15 | – | 20 | – | ns | | |
| Transition time (rise and fall) | t _r | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 50 | ns | | |
| Refresh time | μPD42S16400L, 42S17400L | t _{REF} | – | 128 | – | 128 | – | 128 | – | 128 | ms | 4 |
| | μPD4216400L | | – | 64 | – | 64 | – | 64 | – | 64 | | |
| | μPD4217400L | | – | 32 | – | 32 | – | 32 | – | 32 | | |

- Notes**
- In $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, t_{RAS (MAX.)} is 100 μs.
If 10 μs < t_{RAS} < 100 μs, $\overline{\text{RAS}}$ precharge time for $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh (t_{RPS}) is applied.
 - For read cycles, access time is defined as follows:

| Input conditions | Access time | Access time from $\overline{\text{RAS}}$ |
|---|-------------------------|--|
| t _{RAD} ≤ t _{RAD (MAX.)} and t _{RCD} ≤ t _{RCD (MAX.)} | t _{RAC (MAX.)} | t _{RAC (MAX.)} |
| t _{RAD} > t _{RAD (MAX.)} and t _{RCD} ≤ t _{RCD (MAX.)} | t _{AA (MAX.)} | t _{RAD} + t _{AA (MAX.)} |
| t _{RCD} > t _{RCD (MAX.)} | t _{CAC (MAX.)} | t _{RCD} + t _{CAC (MAX.)} |

t_{RAD (MAX.)} and t_{RCD (MAX.)} are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RAD} ≥ t_{RAD (MAX.)} and t_{RCD} ≥ t_{RCD (MAX.)} will not cause any operation problems.

- t_{CRP (MIN.)} requirement is applied to $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycles.
- This specification is applied only to the μPD42S16400L, 42S17400L.

Read Cycle

| Parameter | Symbol | t _{RAC} = 50 ns | | t _{RAC} = 60 ns | | t _{RAC} = 70 ns | | t _{RAC} = 80 ns | | Unit | Notes |
|--|------------------|--------------------------|------|--------------------------|------|--------------------------|------|--------------------------|------|------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Access time from $\overline{\text{RAS}}$ | t _{RAC} | – | 50 | – | 60 | – | 70 | – | 80 | ns | 1 |
| Access time from $\overline{\text{CAS}}$ | t _{CAC} | – | 13 | – | 15 | – | 18 | – | 20 | ns | 1 |
| Access time from column address | t _{AA} | – | 25 | – | 30 | – | 35 | – | 40 | ns | 1 |
| Access time from $\overline{\text{OE}}$ | t _{OEa} | – | 13 | – | 15 | – | 18 | – | 20 | ns | |
| Column address lead time referenced to $\overline{\text{RAS}}$ | t _{RAL} | 25 | – | 30 | – | 35 | – | 40 | – | ns | |
| Read command setup time | t _{RCS} | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Read command hold time referenced to $\overline{\text{RAS}}$ | t _{RRH} | 0 | – | 0 | – | 0 | – | 0 | – | ns | 2 |
| Read command hold time referenced to $\overline{\text{CAS}}$ | t _{RCH} | 0 | – | 0 | – | 0 | – | 0 | – | ns | 2 |
| Output buffer turn-off delay time from $\overline{\text{OE}}$ | t _{OEZ} | 0 | 10 | 0 | 15 | 0 | 15 | 0 | 20 | ns | 3 |
| Output buffer turn-off delay time from $\overline{\text{CAS}}$ | t _{OFF} | 0 | 10 | 0 | 15 | 0 | 15 | 0 | 20 | ns | 3 |

Notes 1. For read cycles, access time is defined as follows:

| Input conditions | Access time | Access time from $\overline{\text{RAS}}$ |
|---|-------------------------|--|
| t _{RAD} ≤ t _{RAD} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.) | t _{RAC} (MAX.) | t _{RAC} (MAX.) |
| t _{RAD} > t _{RAD} (MAX.) and t _{RCD} ≤ t _{RCD} (MAX.) | t _{AA} (MAX.) | t _{RAD} + t _{AA} (MAX.) |
| t _{RCD} > t _{RCD} (MAX.) | t _{CAC} (MAX.) | t _{RCD} + t _{CAC} (MAX.) |

t_{RAD}(MAX.) and t_{RCD}(MAX.) are specified as reference points only; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions t_{RAD} ≥ t_{RAD}(MAX.) and t_{RCD} ≥ t_{RCD}(MAX.) will not cause any operation problems.

2. Either t_{RCH}(MIN.) or t_{RRH}(MIN.) should be met in read cycles.
3. t_{OFF}(MAX.) and t_{OEZ}(MAX.) define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

| Parameter | Symbol | t _{RAC} = 50 ns | | t _{RAC} = 60 ns | | t _{RAC} = 70 ns | | t _{RAC} = 80 ns | | Unit | Notes |
|--|------------------|--------------------------|------|--------------------------|------|--------------------------|------|--------------------------|------|------|-------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| \overline{WE} hold time referenced to \overline{CAS} | t _{WCH} | 8 | – | 10 | – | 10 | – | 15 | – | ns | 1 |
| \overline{WE} pulse width | t _{WP} | 8 | – | 10 | – | 10 | – | 15 | – | ns | 1 |
| \overline{WE} lead time referenced to \overline{RAS} | t _{RWL} | 18 | – | 20 | – | 20 | – | 20 | – | ns | |
| \overline{WE} lead time referenced to \overline{CAS} | t _{CWL} | 13 | – | 15 | – | 15 | – | 15 | – | ns | |
| \overline{WE} setup time | t _{WCS} | 0 | – | 0 | – | 0 | – | 0 | – | ns | 2 |
| \overline{OE} hold time | t _{OEH} | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Data-in setup time | t _{DS} | 0 | – | 0 | – | 0 | – | 0 | – | ns | 3 |
| Data-in hold time | t _{DH} | 10 | – | 10 | – | 15 | – | 15 | – | ns | 3 |

- Notes**
1. t_{WP}(MIN.) is applied to late write cycles or read modify write cycles. In early write cycles, t_{WCH}(MIN.) should be met.
 2. If t_{WCS} ≥ t_{WCS}(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.
 3. t_{DS}(MIN.) and t_{DH}(MIN.) are referenced to the \overline{CAS} falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the \overline{WE} falling edge.

Read Modify Write Cycle

| Parameter | Symbol | t _{RAC} = 50 ns | | t _{RAC} = 60 ns | | t _{RAC} = 70 ns | | t _{RAC} = 80 ns | | Unit | Note |
|--|------------------|--------------------------|------|--------------------------|------|--------------------------|------|--------------------------|------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read modify write cycle time | t _{RWC} | 133 | – | 160 | – | 180 | – | 205 | – | ns | |
| \overline{RAS} to \overline{WE} delay time | t _{RWD} | 70 | – | 85 | – | 95 | – | 110 | – | ns | 1 |
| \overline{CAS} to \overline{WE} delay time | t _{CWD} | 33 | – | 40 | – | 43 | – | 50 | – | ns | 1 |
| Column address to \overline{WE} delay time | t _{AWD} | 45 | – | 55 | – | 60 | – | 70 | – | ns | 1 |

- Note**
1. If t_{WCS} ≥ t_{WCS}(MIN.), the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If t_{RWD} ≥ t_{RWD}(MIN.), t_{CWD} ≥ t_{CWD}(MIN.), t_{AWD} ≥ t_{AWD}(MIN.) and t_{CPWD} ≥ t_{CPWD}(MIN.), the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Fast Page Mode

| Parameter | Symbol | t _{RAC} = 50 ns | | t _{RAC} = 60 ns | | t _{RAC} = 70 ns | | t _{RAC} = 80 ns | | Unit | Note |
|--|-------------------|--------------------------|---------|--------------------------|---------|--------------------------|---------|--------------------------|---------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Fast page mode cycle time | t _{PC} | 35 | – | 40 | – | 45 | – | 50 | – | ns | |
| Access time from $\overline{\text{CAS}}$ precharge | t _{ACP} | – | 30 | – | 35 | – | 40 | – | 45 | ns | |
| $\overline{\text{RAS}}$ pulse width | t _{RASP} | 50 | 125,000 | 60 | 125,000 | 70 | 125,000 | 80 | 125,000 | ns | |
| $\overline{\text{CAS}}$ precharge time | t _{CP} | 8 | – | 10 | – | 10 | – | 10 | – | ns | |
| $\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge | t _{RHCP} | 30 | – | 35 | – | 40 | – | 45 | – | ns | |
| Read modify write cycle time | t _{PRWC} | 73 | – | 83 | – | 90 | – | 95 | – | ns | |
| $\overline{\text{CAS}}$ precharge to $\overline{\text{WE}}$ delay time | t _{CPWD} | 50 | – | 58 | – | 65 | – | 70 | – | ns | 1 |

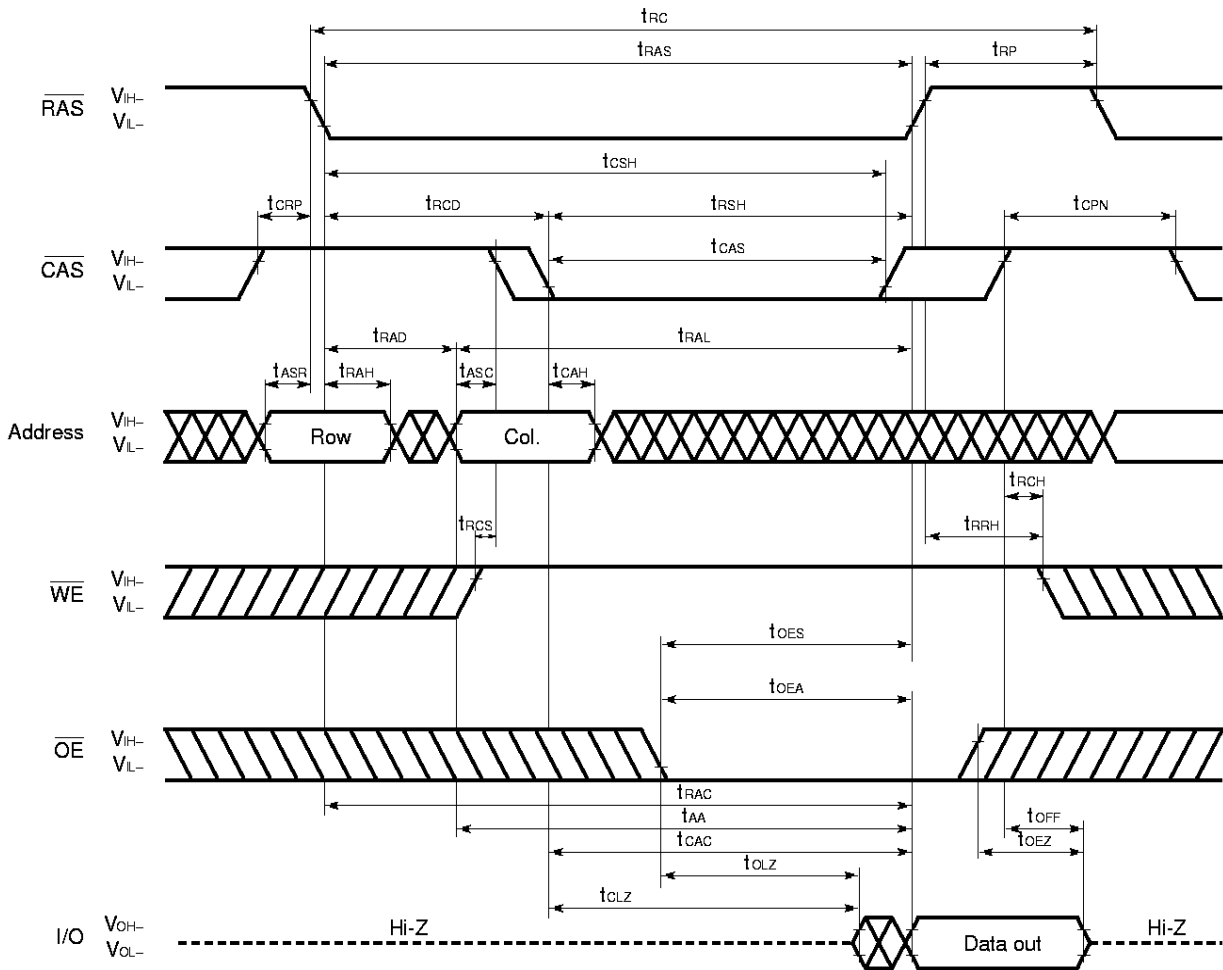
Note 1. If $t_{\text{WCS}} \geq t_{\text{WCS(MIN.)}}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{\text{RW}} \geq t_{\text{RW(MIN.)}}$, $t_{\text{CWD}} \geq t_{\text{CWD(MIN.)}}$, $t_{\text{AWD}} \geq t_{\text{AWD(MIN.)}}$ and $t_{\text{CPWD}} \geq t_{\text{CPWD(MIN.)}}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Refresh Cycle

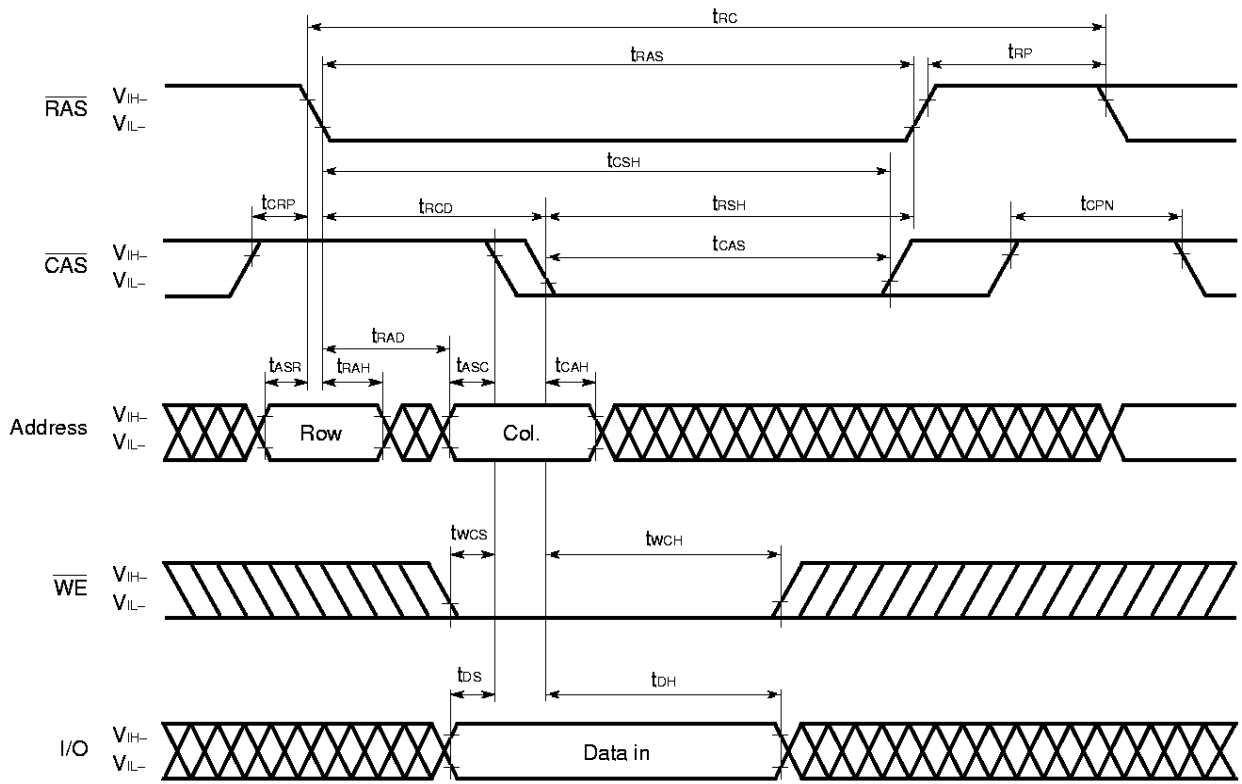
| Parameter | Symbol | t _{RAC} = 50 ns | | t _{RAC} = 60 ns | | t _{RAC} = 70 ns | | t _{RAC} = 80 ns | | Unit | Note |
|---|-------------------|--------------------------|------|--------------------------|------|--------------------------|------|--------------------------|------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| $\overline{\text{CAS}}$ setup time | t _{CSR} | 5 | – | 5 | – | 5 | – | 5 | – | ns | |
| $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) | t _{CHR} | 10 | – | 10 | – | 10 | – | 10 | – | ns | |
| $\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time | t _{RPC} | 5 | – | 5 | – | 5 | – | 5 | – | ns | |
| $\overline{\text{RAS}}$ pulse width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh) | t _{RASS} | 100 | – | 100 | – | 100 | – | 100 | – | μs | 1 |
| $\overline{\text{RAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh) | t _{RPS} | 90 | – | 110 | – | 130 | – | 150 | – | ns | 1 |
| $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ self refresh) | t _{CHS} | –50 | – | –50 | – | –50 | – | –50 | – | ns | 1 |
| $\overline{\text{WE}}$ setup time | t _{WSR} | 10 | – | 10 | – | 10 | – | 10 | – | ns | |
| $\overline{\text{WE}}$ hold time | t _{WHR} | 15 | – | 15 | – | 15 | – | 15 | – | ns | |

Note 1. This specification is applied only to the μPD42S16400L, 42S17400L.

Read Cycle

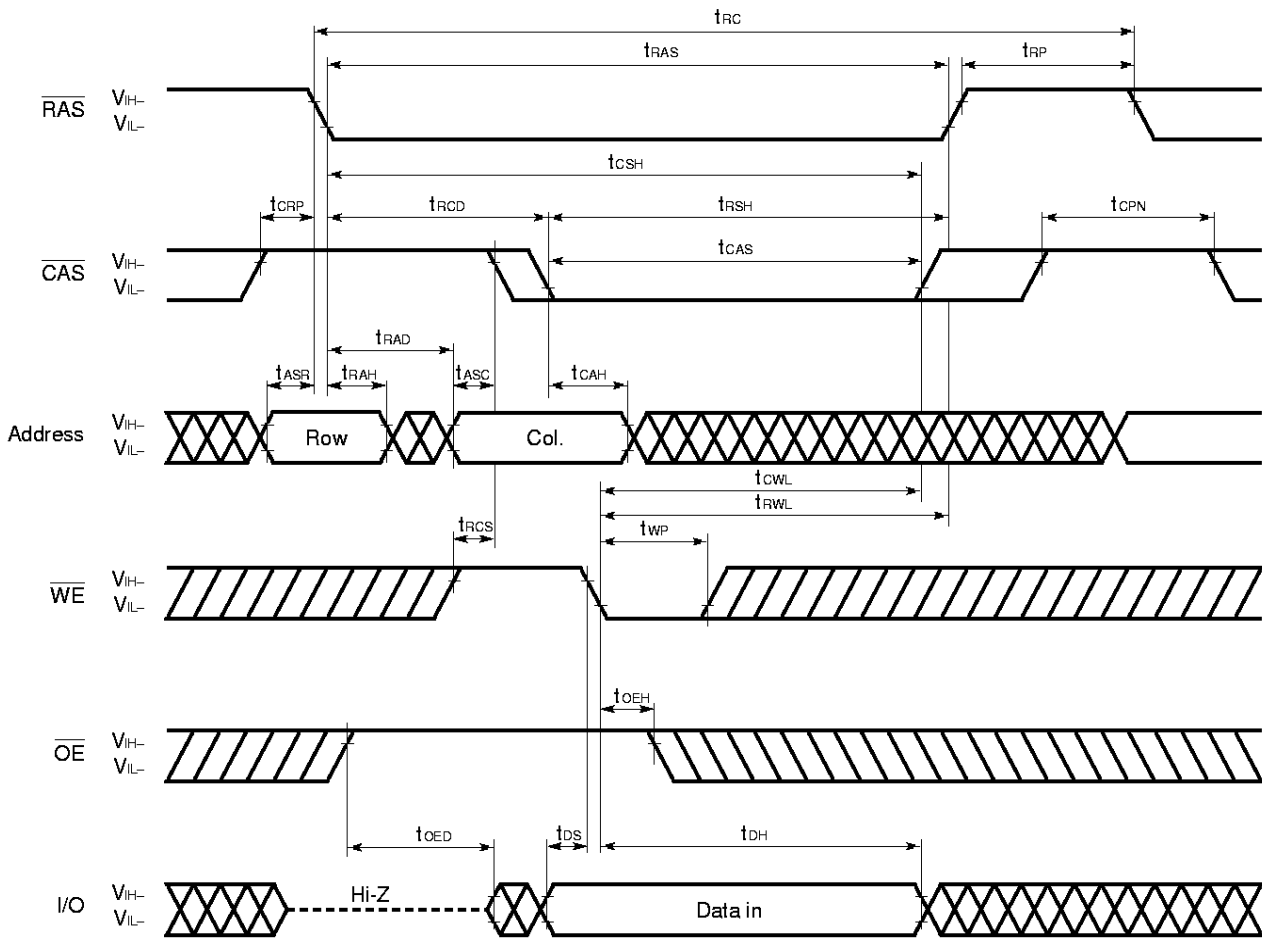


Early Write Cycle

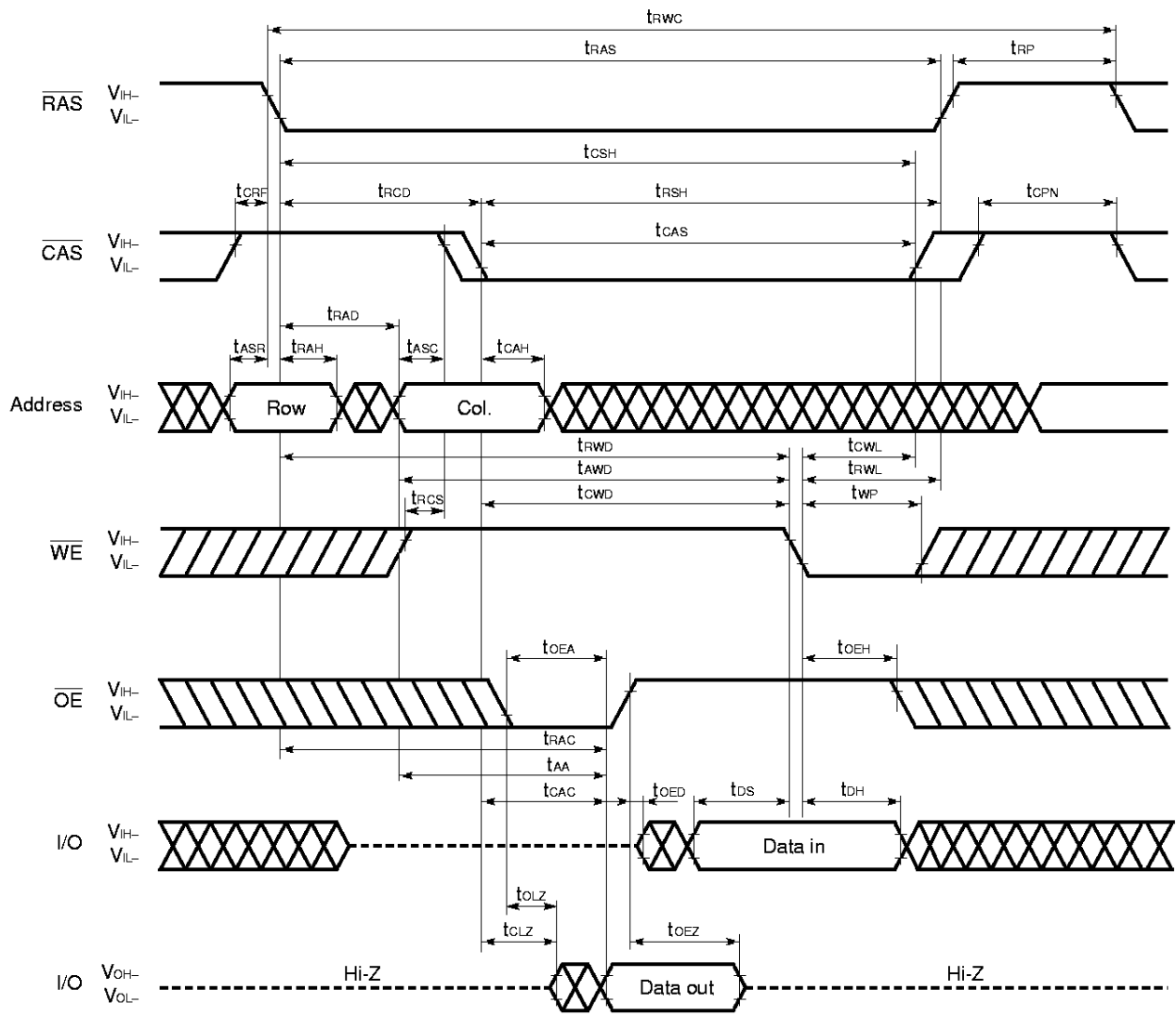


Remark \overline{OE} : Don't care

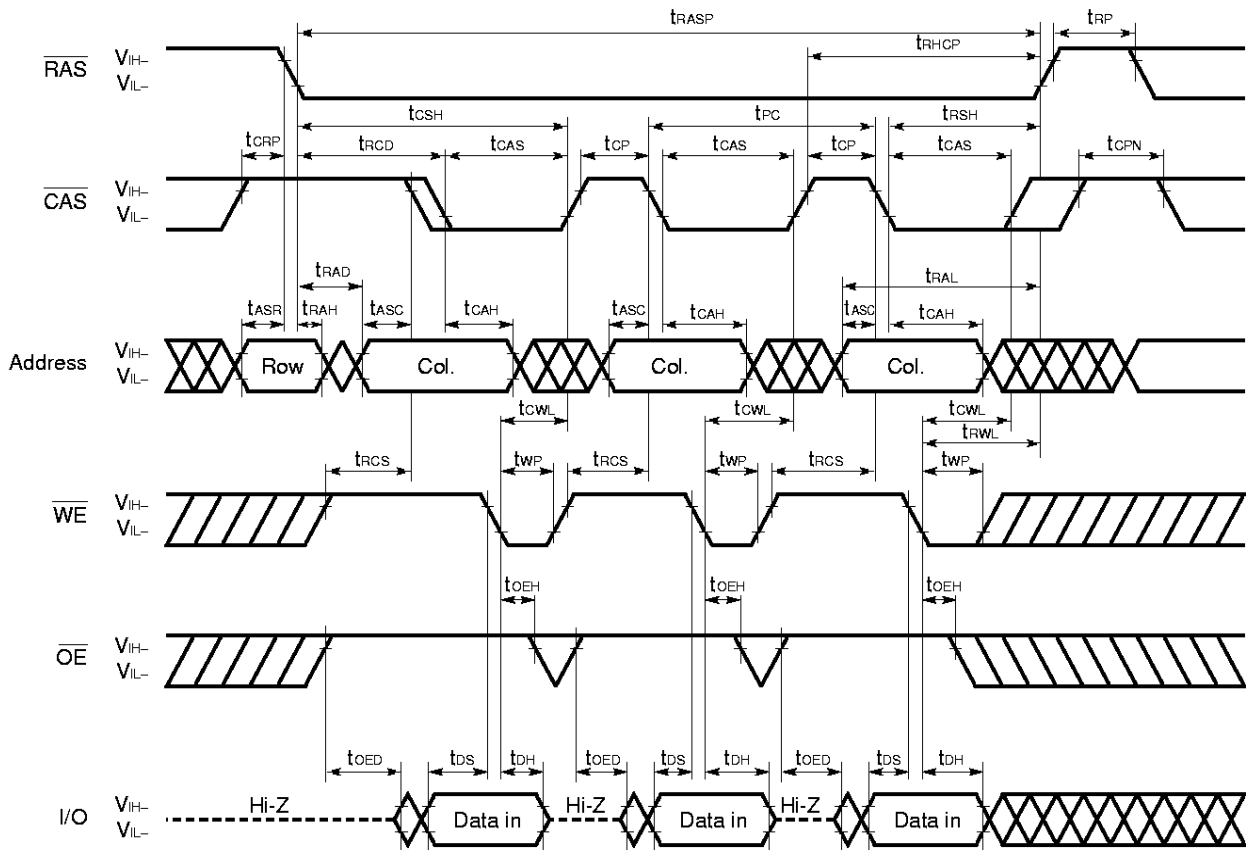
Late Write Cycle



Read Modify Write Cycle

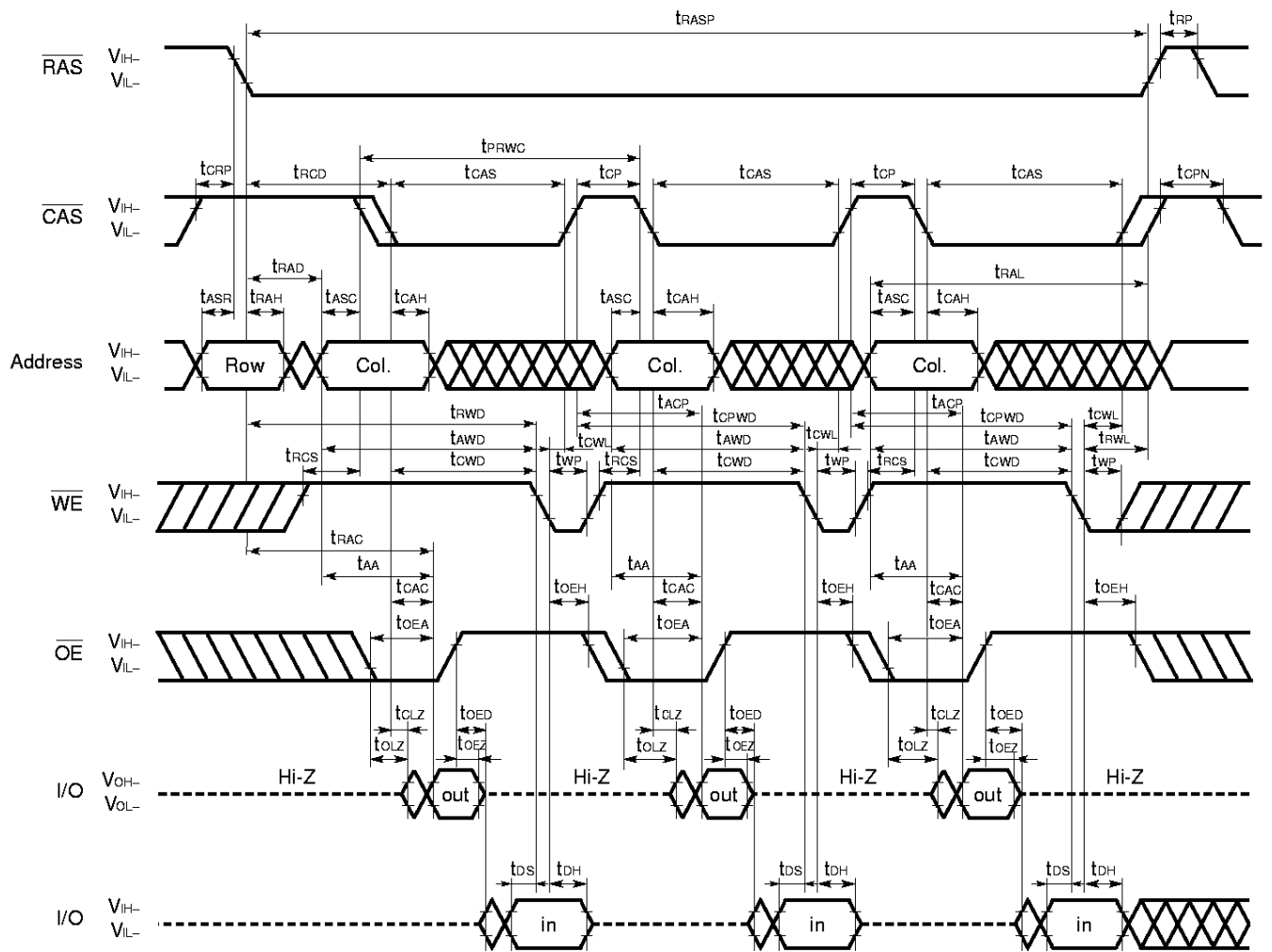


Fast Page Mode Late Write Cycle



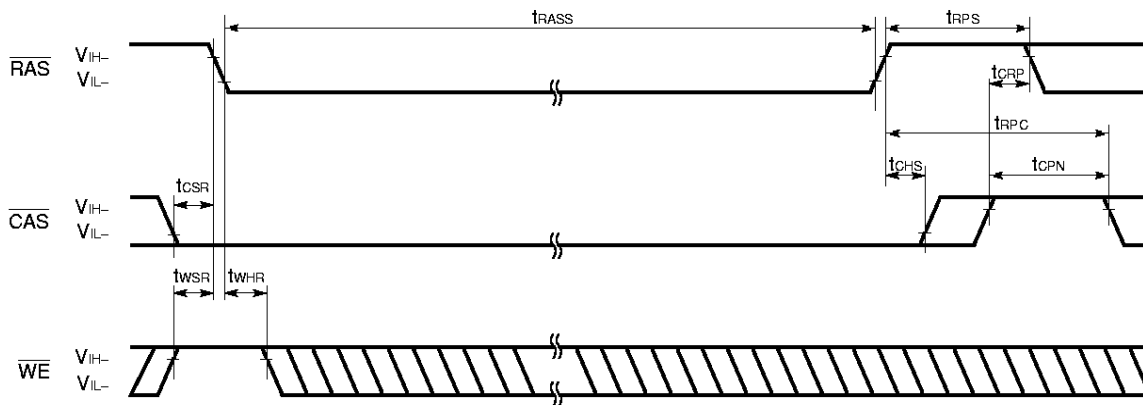
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

Fast Page Mode Read Modify Write Cycle



Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{\text{CAS}}$ cycles within the same $\overline{\text{RAS}}$ cycle.

CAS Before RAS Self Refresh Cycle (Only for the μ PD42S16400L, 42S17400L)



Remark Address, \overline{OE} : Don't care I/O : Hi-Z

Cautions on Use of CAS Before RAS Self Refresh

CAS before RAS self refresh can be used independently when used in combination with distributed CAS before RAS long refresh; However, when used in combination with burst CAS before RAS long refresh or with long RAS only refresh (both distributed and burst), the following cautions must be observed.

(1) Normal Combined Use of CAS Before RAS Self Refresh and Burst CAS Before RAS Long Refresh

When CAS before RAS self refresh and burst CAS before RAS long refresh are used in combination, please perform CAS before RAS refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16400L : 4,096 times within a 64 ms interval

μ PD42S17400L : 2,048 times within a 32 ms interval

(2) Normal Combined Use of CAS Before RAS Self Refresh and Long RAS Only Refresh

When CAS before RAS self refresh and RAS only refresh are used in combination, please perform RAS only refresh as follows just before and after setting CAS before RAS self refresh.

μ PD42S16400L : 4,096 times within a 64 ms interval

μ PD42S17400L : 2,048 times within a 32 ms interval

(3) If $t_{RASS(MIN.)}$ is not satisfied at the beginning of CAS before RAS self refresh cycles ($t_{RAS} < 100 \mu s$), CAS before RAS refresh cycles will be executed one time.

If $10 \mu s < t_{RAS} < 100 \mu s$, RAS precharge time for CAS before RAS self refresh (t_{RPS}) is applied.

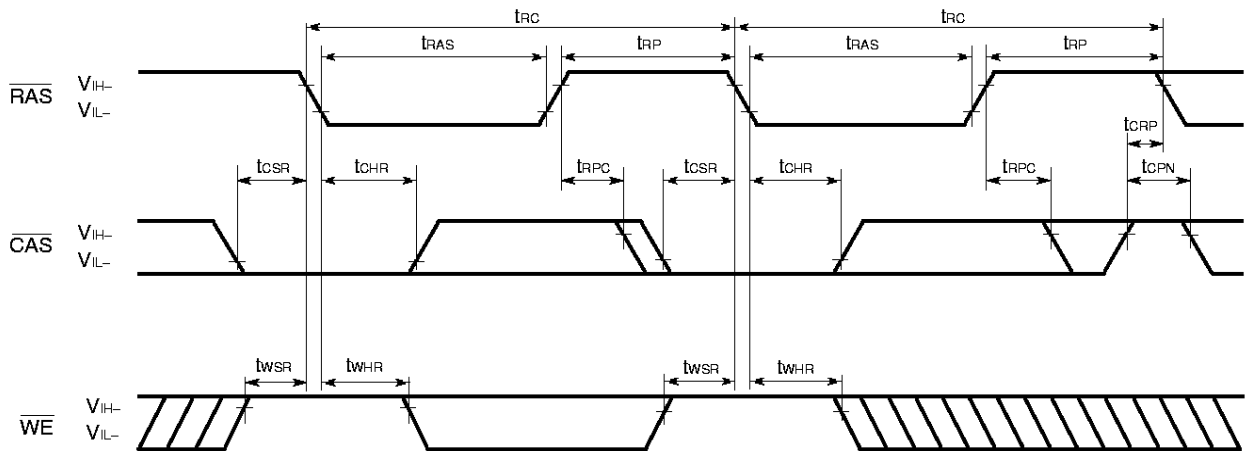
And refresh cycles as follows should be met.

μ PD42S16400L : 4,096 times within a 128 ms interval

μ PD42S17400L : 2,048 times within a 128 ms interval

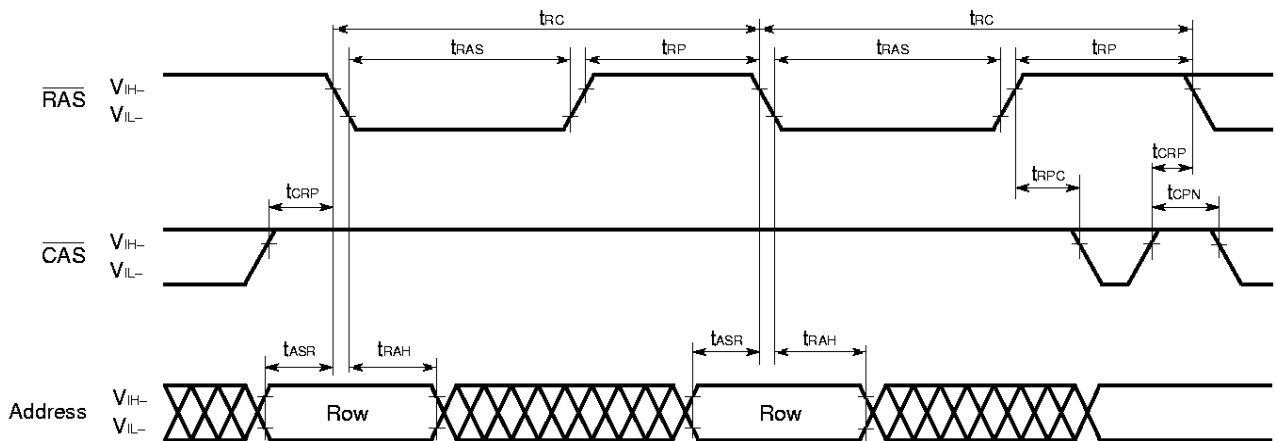
For details, please refer to **How to use DRAM** User's Manual.

CAS Before RAS Refresh Cycle



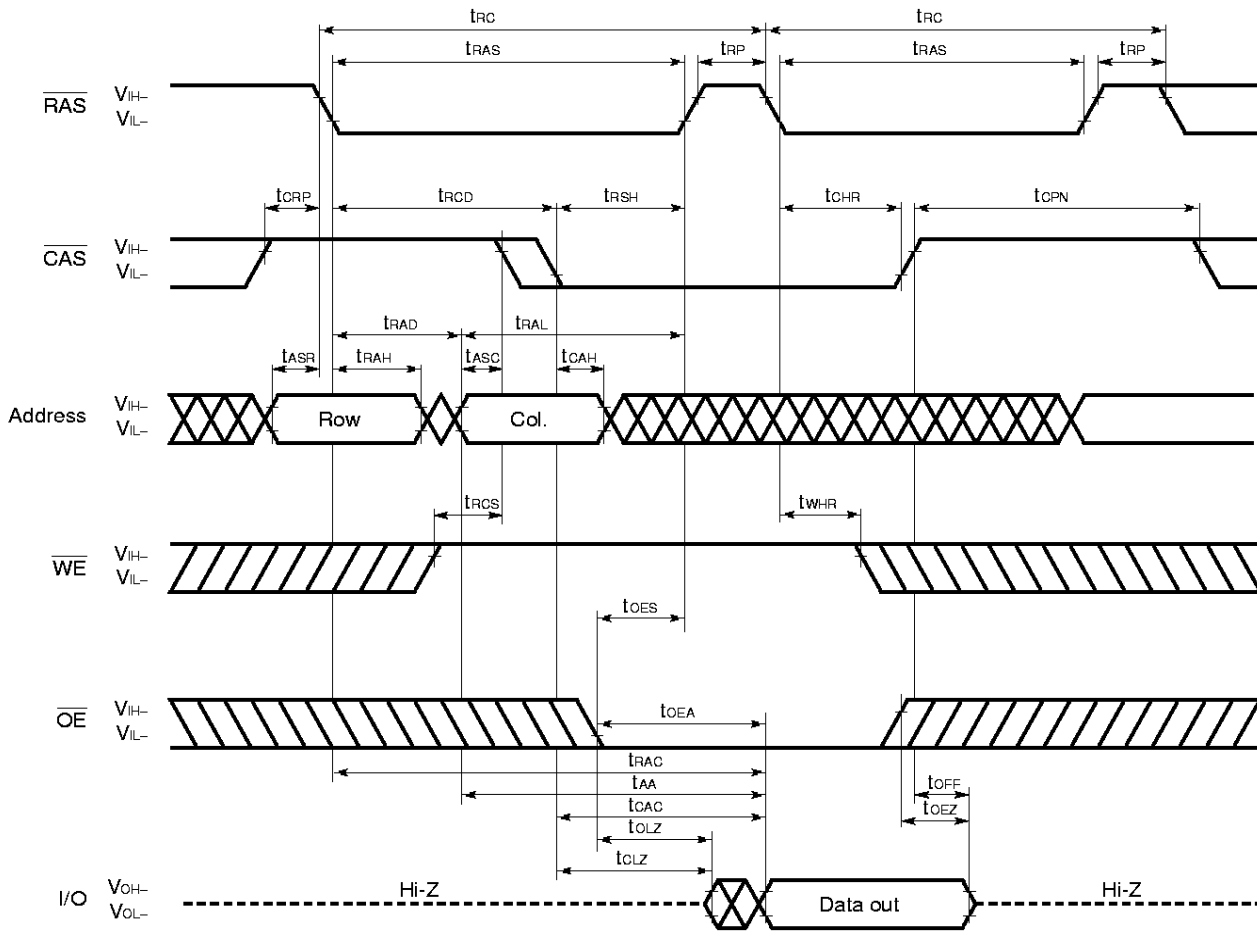
Remark Address, \overline{OE} : Don't care I/O: Hi-Z

RAS Only Refresh Cycle

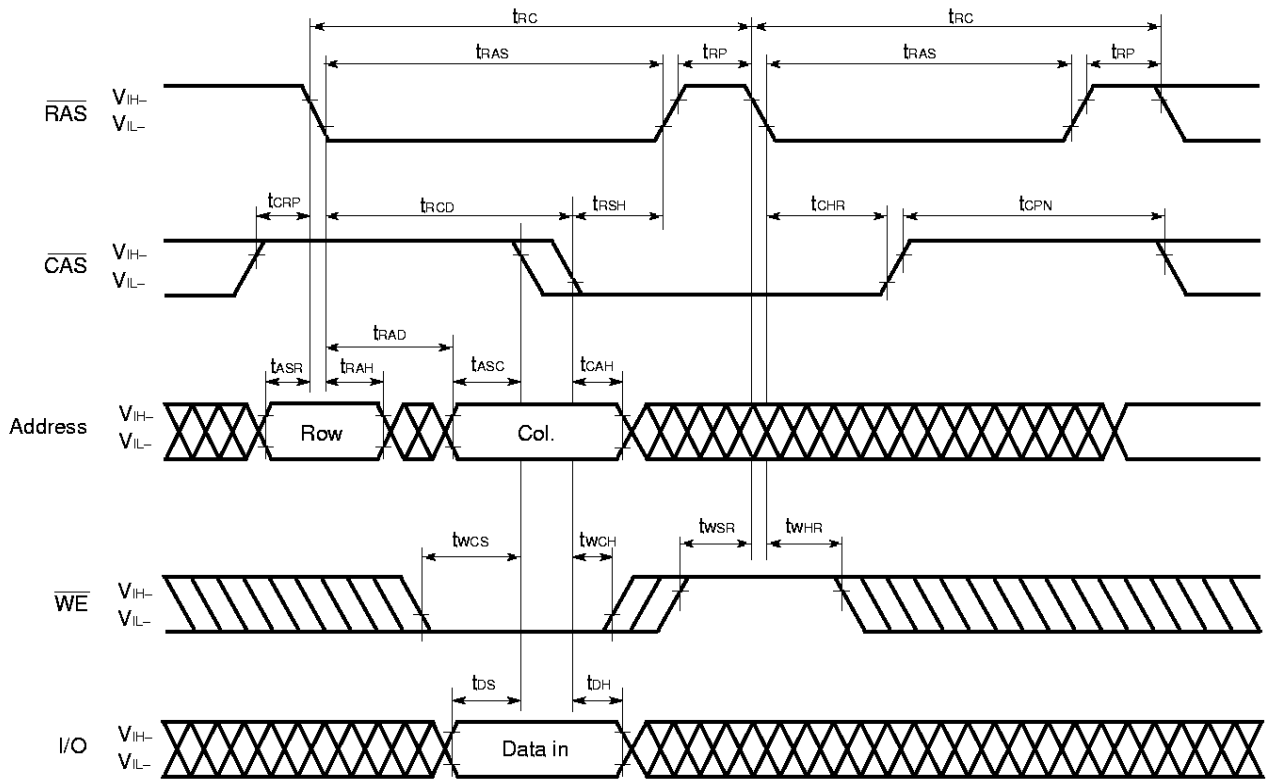


Remark \overline{WE} , \overline{OE} : Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)

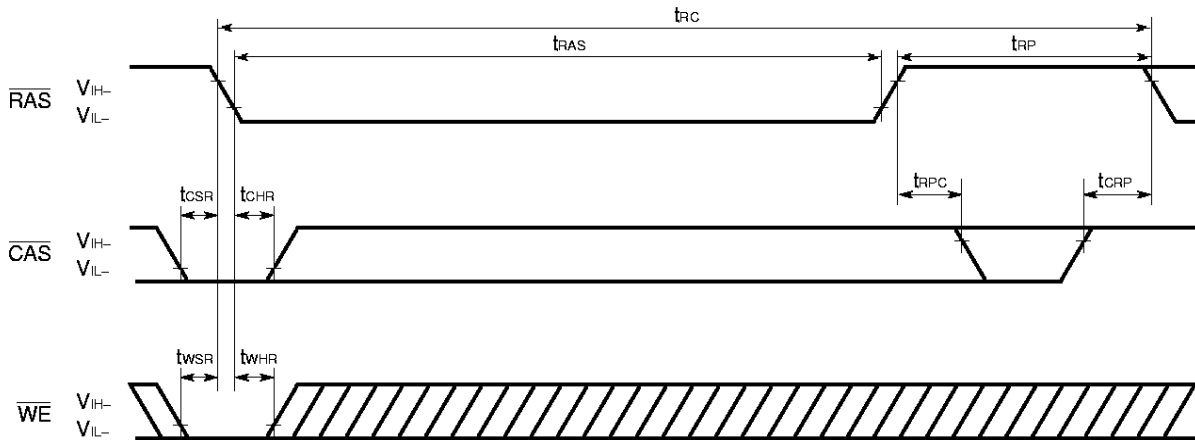


Hidden Refresh Cycle (Write)



Remark \overline{OE} : Don't care

Test Mode Set Cycle (\overline{WE} , \overline{CAS} Before \overline{RAS} Refresh Cycle)



Remark Address, \overline{OE} : Don't care I/O: Hi-Z

Test Mode

By using the test mode, the test time can be reduced. The reason for this is that, the memory emulates the $\times 16$ -bit organization during test mode. Don't care about the input levels of the \overline{CAS} input A0, A1.

(1) Setting the mode

Executing the test mode cycle (\overline{WE} , \overline{CAS} before \overline{RAS} refresh cycle) sets the test mode.

(2) Write/read operation

When either a "0" or a "1" is written to the input pin in test mode, this data is written to 16 bits of memory cell.

Next, when the data is read from the output pin at the same address, the cell can be checked.

Output = "1": Normal write (all memory cells)

Output = "0": Abnormal write

(3) Refresh

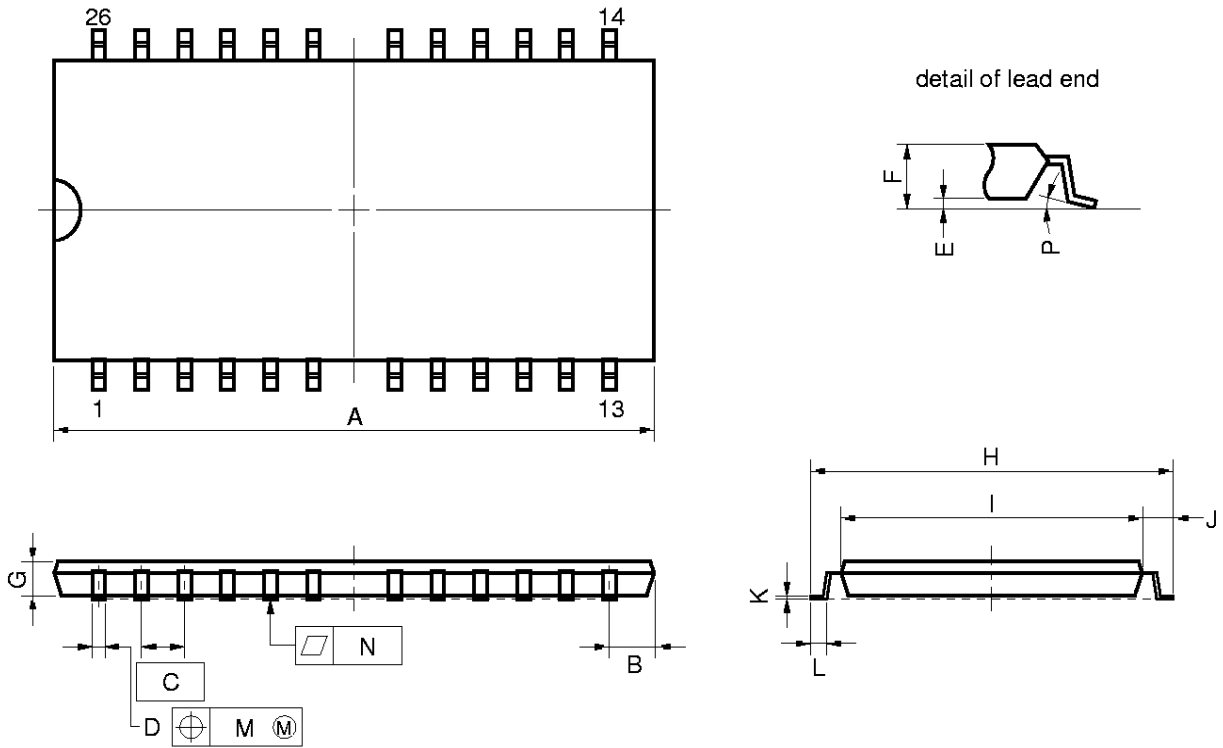
Refresh in the test mode must be performed with the \overline{RAS} / \overline{CAS} cycle or with the \overline{WE} , \overline{CAS} before \overline{RAS} refresh cycle. The \overline{WE} , \overline{CAS} before \overline{RAS} refresh cycle use the same counter as the \overline{CAS} before \overline{RAS} refresh's internal counter.

(4) Mode Cancellation

The test mode is cancelled by executing one cycle of \overline{RAS} only refresh cycle or \overline{CAS} before \overline{RAS} refresh cycle.

Package Drawings

26PIN PLASTIC TSOP(II) (300 mil)



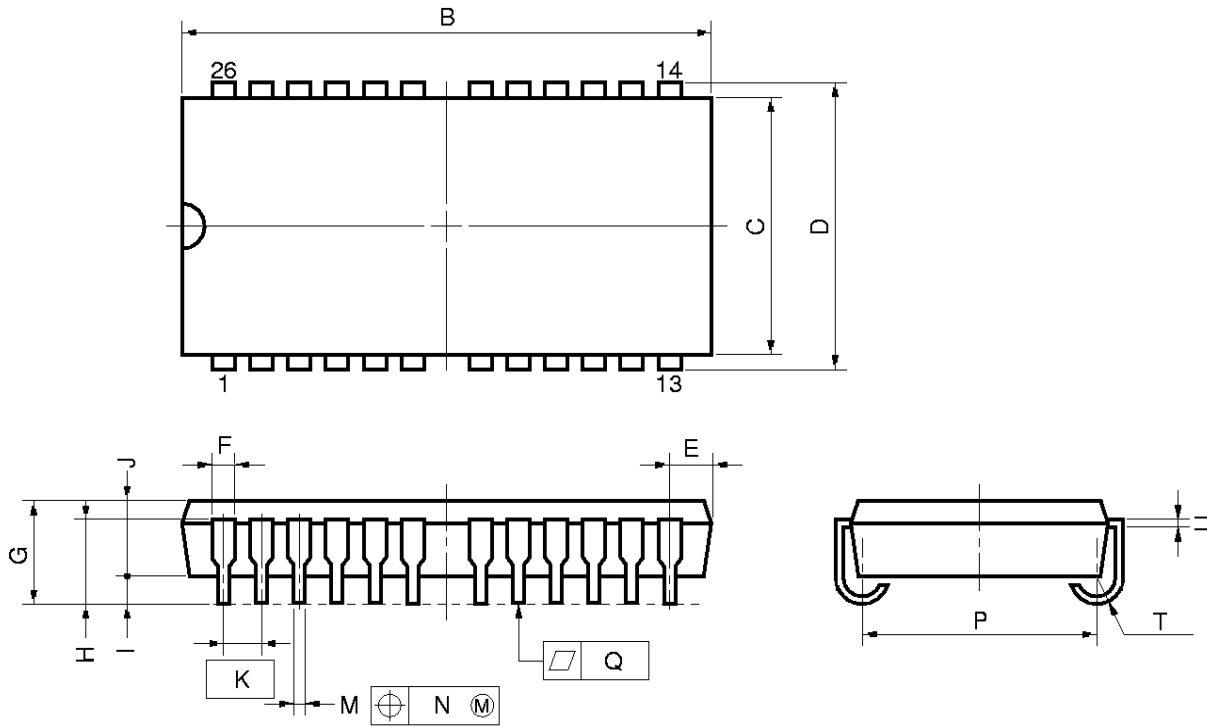
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 17.36 MAX. | 0.684 MAX. |
| B | 1.06 MAX. | 0.042 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.42 ^{+0.08} _{-0.07} | 0.017±0.003 |
| E | 0.1±0.05 | 0.004±0.002 |
| F | 1.2 MAX. | 0.048 MAX. |
| G | 0.97 | 0.038 |
| H | 9.22±0.2 | 0.363±0.008 |
| I | 7.62±0.1 | 0.300±0.004 |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.145 ^{+0.025} _{-0.015} | 0.006±0.001 |
| L | 0.5±0.1 | 0.020 ^{+0.004} _{-0.005} |
| M | 0.21 | 0.009 |
| N | 0.10 | 0.004 |
| P | 3°+7° -3° | 3°+7° -3° |

S26G3-50-7JD1

26 PIN PLASTIC SOJ (300 mil)



NOTE
 Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| B | 17.3 ^{+0.20} _{-0.25} | 0.681 ^{+0.008} _{-0.010} |
| C | 7.62 | 0.300 |
| D | 8.47±0.2 | 0.333 ^{+0.009} _{-0.008} |
| E | 1.03±0.15 | 0.041 ^{+0.006} _{-0.007} |
| F | 0.74 | 0.029 |
| G | 3.5±0.2 | 0.138±0.008 |
| H | 2.545±0.2 | 0.100±0.008 |
| I | 0.8 MIN. | 0.031 MIN. |
| J | 2.6 | 0.102 |
| K | 1.27 (T.P.) | 0.050 (T.P.) |
| M | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| N | 0.12 | 0.005 |
| P | 6.73±0.2 | 0.265±0.008 |
| Q | 0.10 | 0.004 |
| T | R0.85 | R0.033 |
| U | 0.20 ^{+0.10} _{-0.05} | 0.008 ^{+0.004} _{-0.002} |

S26LA-300A-1

★ **Recommended Soldering Conditions**

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD42S16400L, 4216400L, 42S17400L, 4217400L.

For more details, refer to our document “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Types of Surface Mount Device

μPD42S16400LG3-7JD, 4216400LG3-7JD, 42S17400LG3-7JD, 4217400LG3-7JD: 26-pin plastic TSOP (II) (300 mil)

| Soldering process | Soldering conditions | Symbol |
|------------------------|--|------------|
| Infrared ray reflow | Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) | IR35-107-3 |
| VPS | Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limi: 7 days ^{Note} (10 hours pre-baking is required at 125 °C afterwards) | VP15-107-3 |
| Partial heating method | Terminal temperature: 300 °C or lower, Time: 3 seconds or lower (Per side of the package). | ————— |

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

μPD42S16400LLA, 4216400LLA, 42S17400LLA, 4217400LLA: 26-pin plastic SOJ (300 mil)

| Soldering process | Soldering conditions | Symbol |
|------------------------|--|------------|
| Infrared ray reflow | Peak temperature of package surface: 235 °C or lower, Reflow time: 30 seconds or less (210 °C or higher), Number of reflow processes: MAX. 3 Exposure limit: 7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards) | IR35-207-3 |
| VPS | Peak temperature of package: 215 °C or lower, Reflow time: 40 seconds or less (200 °C or higher), Number of reflow processes: MAX. 3 Exposure limit :7 days ^{Note} (20 hours pre-baking is required at 125 °C afterwards) | VP15-207-3 |
| Partial heating method | Terminal temperature: 300 °C or lower, Time: 3 seconds or less (Per side of the package). | ———— |

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for “Partial heating method”.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.