STARTECH

ST37C65

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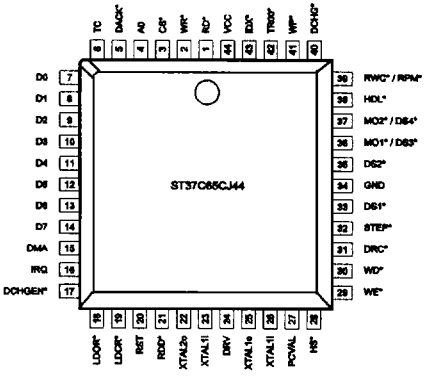
FLOPPY DISK SUBSYSTEM CONTROLLER

DESCRIPTION

The ST37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "super-chip" integrates the following functions: formatter / controller, data separation, write precompensation, data rate selection (to a maximum of 1Mbit per second), and clock generation. It also provides interface drivers and receivers for the floppy drive.

The ST37C65 is functionally compatible pin-for-pin with the WD37C65C. In addition the ST37C65 Supports a power down mode for laptop and portable systems.

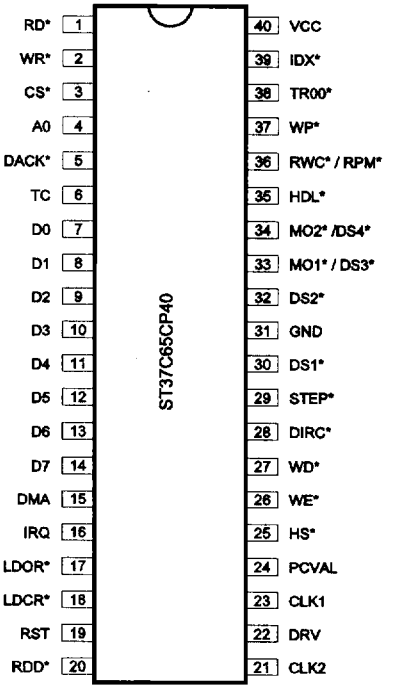
PLCC Package



FEATURES

- IBM* PC AT* compatible format (single and double density)
- BIOS compatible, supports dual speed spindle drives
- Address mark detection circuitry (internal to floppy disk controller)
- Multi-sector and multi-track transfer capability
- Direct floppy disk drive interface (no buffers needed)
- 48 mA sink output drivers
- Automatic write pre-compensation Disable option, Pin selectable inner track values of 125 or 187 nanoseconds
- Integrated high-performance DPLL data separator, industry standard error rates of <10E-9
- Data rates of 125, 250, 300, 500 Kbits/second and 1 Mbit/second
- User programmable track stepping rate and head load/unload times
- Supports four floppy drives

DIP Package



ORDERING INFORMATION

Part number	Package	Operating temperature
ST37C65CJ44	PLCC	0° C to + 70° C
ST37C65CP40	Plastic-Dip	0° C to + 70° C

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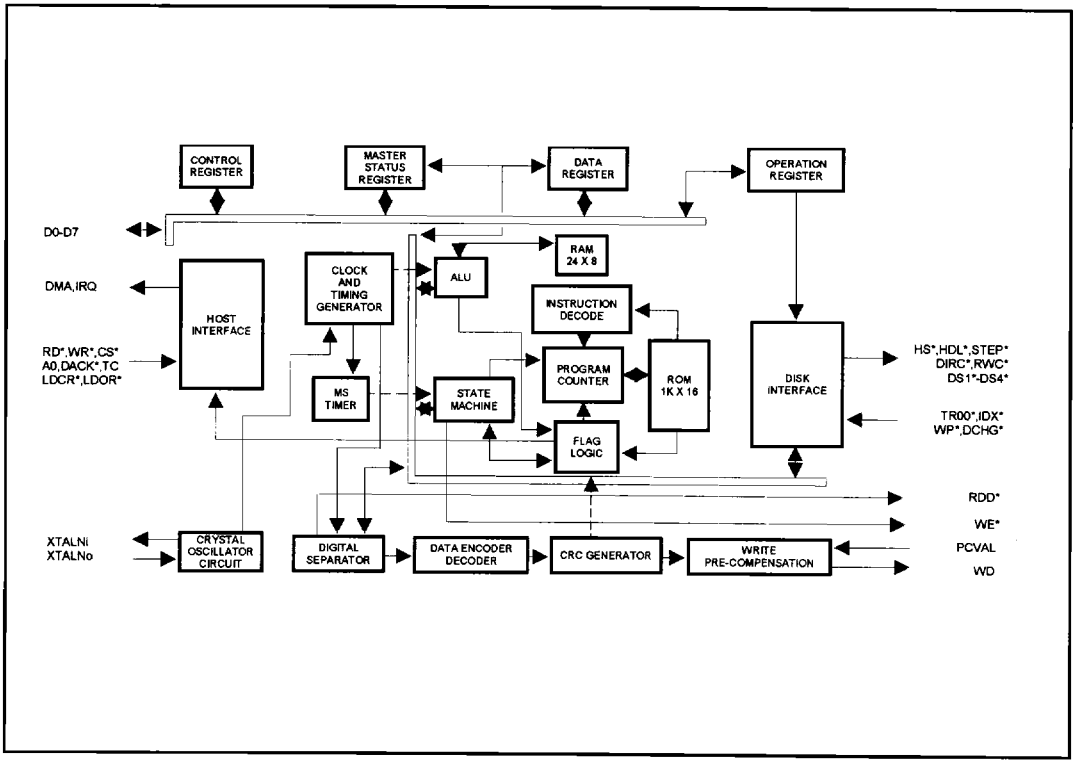
BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
RD*	1	I	Read signal (active low). Control signal for transfer of data or status onto the data bus by the ST37C65.
WR*	2	I	Write signal (active low). Control signal for latching data from the bus into the ST37C65 buffer register.
CS*	3	I	Chip select (active low). Selected when low allowing RD* or WR* operation from the host.
A0	4	I	Address line 1. Address line selecting data or status information.
DACK*	5	I	DMA ACKNOWLEDGE (active low). Used by DMA controller to transfer data from the ST37C65 onto the bus. AT/EISA mode, this signal is qualified by DMAEN from the Operation Register.
TC	6	I	Terminal Count (active high). This signal indicates to ST37C65 that data transfer is complete. If DMA operation mode is selected for command execution, TC will be qualified by DACK*, but not in the programmed I/O execution. In AT/EISA or Special mode, qualification by DACK* requires the Operation Register signal DMAEN to be logically true. Note also AT/EISA mode, TC will be qualified by DACK*, whether in DMA or non-DMA host operation. Programmed I/O in AT/EISA mode will cause an abnormal termination error at the completion of a command.
DB0-DB7	7-14	I/O	Data bus. 8 bit, bi-directional, three state, data bus. DB0 id the least significant bit and DB7 is the most significant bit.
DMA	15	O	Direct Memory Access (three state, active high). DMA request for byte transfers of data. In Special or AT/EISA mode, this pin is three stated, enabled by the DMAEN signal from the Operation Register. This pin is driven in the Base mode.
IRQ	16	O	Interrupt (three state, active high). Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in Base

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			mode. In Special AT/EISA mode, this pin is three stated, enabled by DMAEN signal from the Operation Register.
DCHGEN*	17	I	Disk Change Enable (active low). This input must be at logic "0" to enable DCHG* input status at pin 40 to be placed on bit-7 of the data bus during RD* of LDCR*. It has internal pull-up.
LDOR*	18	I	Load Operations Register (active low). Address decode which enables the loading of the Operation Register. Internally gated with WR* creates the strobe which latches the data bus into the Operations Register.
LDCR*	19	I	Load Control Register (active low). Address decode which enablesloading of the Control Register. Internally gated with WR* create the strobe which latches the two LSBs from the data bus into the Control Register.
RST	20	I	Reset (active high). Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
RDD*	21	I	Read Disk Data. This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of encoded data.
*CLK2	21	I	Clock-2. TTL level clock input used for non-standard data rates; is 9.6 MHz for 300 kb/s, and can only be selected from the Control Register.
XTAL2o	22	O	Crystal oscillator drive output. A crystal oscillator is connected from this pin to XTAL2i pin. This pin should be left floating if TTL inputs used at pin XTAL2i.
XTAL2i	23	I	Crystal oscillator or External clock input pin. Used for non-standard data rates.
DRV	24	I	Drive Type. This input indicates to the device that a two speed spindle motor is used if logic is "0". In that case, the second clock input will never be selected and must be grounded.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
*CLK1	23	I	Clock1. TTL level clock input is used to generate all internal timing for standard data rates. Frequency must be 16 MHz ±0.1% or 32 MHz ±0.1%, and may have 40/60 or 60/40 duty cycle.
XTAL1o	25	O	Crystal oscillator drive output. A crystal oscillator is connected from this pin to XTAL1i pin. This pin should be left floating if TTL inputs used at pin XTAL1i.
XTAL1i	26	I	Crystal oscillator or External clock input pin. Requires 16 MHz or 32 MHz crystal. This oscillator is used for all standard data rates, and may be driven with TTL level signal.
PCVAL	27	I	Pre-Compensation Value. This pin determines the amount of write pre-compensation used on the inner tracks of the diskette. Logic "1" = 125 ns, logic "0" = 187 ns. If the data defeat option is used, PCVAL is unimportant and pre-compensation is disabled.
HS*	28	O	Head Select (active low). High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic "1" = side 0.
WE*	29	O	Write Enable (active low). The output becomes true, just prior to writing on the diskette. This allows current to flow through the write head.
WD*	30	O	Write Data. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
DIRC*	31	O	Direction (active low). DIRC* determines the direction of the head stepper motor. Logic "1" = outward motion.
STEP*	32	O	Step Pulse (active low). STEP* output issues an active low pulse for each track to track movement of the hrad.
DS1*	33	O	Drive Select-1 (active low). It enables the interface to this disk drive. This signal comes from the Operation Register. In Base mode, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			syntax.
GND	34	O	Supply ground.
DS2*	35	O	Drive Select-2 (active low). It enables the interface to this disk drive. This signal comes from the Operation Register. In Base mode, or Special mode, this output is #2 of the four decoded Unit Selects, as specified in the device command syntax.
MO1*, DS3*	36	O	Motor On enable for disk drive #1 (active low). This signal comes from the Operation Register. In Base mode, or Special mode, this output is #3 of the four decoded Unit Selects, as specified in the device command syntax.
MO2*, DS4*	37	O	Motor On enable for disk drive #2 (active low). This signal comes from the Operation Register. In Base mode, or Special mode, this output is #4 of the four decoded Unit Selects, as specified in the device command syntax.
HDL*	38	O	Head Load (active low). When HDL* is low, causes the head to be loaded againt the media in the selected drive.
RWC*, RPM*	39	O	Readuced Write Current / Revolutions Per Minute (active low). When low, causes a Reduced Write Current when bit density is increased toward the inner tracks, becoming active when tracks >28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write pre-compensation is necessary. In the AT/EISA mode, this signal will be active when CR0=1.
DCHG*	40	I	Disk Change (active low). This input senses status from the drive. Active low indicates that drive door is open or that the diskette has possibly changed since the last drive selection. It has internal pull-up.
WP*	41	I	Write Protected (active low). This input senses status from disk drive, indicating active low when a diskette is Write Protected.
TR00*	42	I	Track Zero (active low). This input senses status from disk

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			drive, indicating active low when the head is positioned over the outermost track, Track 00.
IDX*	43	I	Index (active low) This input senses status from disk drive, indicating active low when the head is positioned over the begining of a track marked by an index hole.
VCC	44	I	Positive supply input.

* 40 Pin package only

FUNCTIONAL DESCRIPTION

ST37C65 includes data separation designed to address high performance error rate on floppy disk drives. It contains all the necessary Logic to achieve classical 2nd order, type 2, phase locked-loop performance. Write pre-compensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with 48 mA drivers which meet the ANSI specification.

The host interface supports an 8 or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers. Output drive capability is 20 LS-TTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC, PC AT and EISA applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the ST37C65, these functions are latched into registers addressed within the I/O mapping of the system. The ST37C65 has eight internal registers. The eight bit main status register contains status information about the ST37C65 and may be accessed any time. Another four status registers under system control also give various status and error information. The. Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the ST37C65.

CLOCK GENERATION

SCLK - Sampling Clock, WCLK- Write Clock, and MCLK - Master Clock, are included in the ST37C65. XTAL oscillator circuits provide the necessary signals for internal liming when using the 44 pin PLCC. If the 40 pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the ST37C65. The first at 32 MHz that handles all standard data rates (1Mb/sec, 500, 250, and 125 kb/sec or 16 MHz to handle 500, 250, and 125 Kb/sec.). The second oscillator is at 9.6 MHz to support the 300 kb/sec data rate used in PC AT designs.
Some AT compatibles use two-speed disk drives. If a two speed disk drive is used, the DRV input should be grounded along with the CLK2 input.

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ARCHITECTURE

The ST37C65 Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "super-chip" integrates formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or AT/EISA modes IRQ and DMA request are three-stated and qualified by DMA enable which is provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LS-TTL loading. Inputs are Schmitt Trigger receivers and can be hooked up to a bus or back plane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU waits for 12μs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of The command word may be written into the ST37C65. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the ST37C65. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register.

Note that this reading of the Main Status Register before each byte transfer to the ST37C65 is required only in the Command and Result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12μs.

During the Execution phase, the Main Status Register need not be read. If the ST37C65 is in the non-DMA Mode, then the receipt of each data byte (ST37C65 is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal (RD*=0) clears the interrupt and sends the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the WR* signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the ST37C65 is in the DMA mode, no interrupt signals are generated during the Execution phase. The ST37C65 generates DMA's (DMA Requests) when each byte of data is available The DMA Controller responds to this request with both DACK*= 0 (DMA Acknowledge) and an RD*=0 (Read signal). When the DMA Acknowledge signal goes low (DACK*= 0), the DMA Request is cleared DMA= 0) If a Write Command has been issued, then a WR* signal will appear instead of RD*. After the Execution phase has been completed (Terminal Count has occurred) The EOT sector read/written, then an Interrupt will occur (IRQ=1) this signifies the begining of the result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (IRQ=0). Note that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the ST37C65 will successfully complete commands, but will at ways give abnormal termination error status since TC is qualified by an inactive DACK*. The RD* or WD* signals should be asserted while DACK* is true The CS* signal is used in conjunction with RD* and WR* as gating function during programmed I/O operations. CS* has no effect during DMA operations. It the non-DMA mode is chosen, the DACK signal should be pulled up to VCC.

Note that during the Result phase all bytes shown in the Command Table must be read.

The Read Data Command, for example has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The ST37C65 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during

the Result phase. The ST37C65 contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the ST37C65 to form the command phase, and are read out of the ST37C65 in the result phase, must occur in the order shown in the Command table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the command phase is sent to the ST37C65, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the result phase, the command is automatically ended and the ST37C65 is ready for a new command.

CONTROL REGISTER

The Control Register is a write only register that is used to set the data transfer rate and disable write precompensation. It provides support logic that latches the two LSBs of the data bus upon receiving LDCR* and WR*. CS* should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switch over is internally "deglitched", allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64 times the desired MFM data rate. This implies a maximum data rate of 250 kb/s for a frequency of 16 MHz or a maximum data rate of 500 kb/s for a frequency of 32 MHz, unless the Control Register is used. Switching of this clock must be "glitchess" or the device will need to be reset. Table 1 and Table 2 present the Control Register configuration for 16 MHz and 32 MHz frequencies, respectively.

ST37C65 optionally supports 150 kbits FM data transfer rate. The Control Register configuration is shown in Table 3. The 150 kb/s data rate can be selected by using a 9.6 MHz XTAL or TTL level clock input on pin 26 (44-pin PLCC) or pin 23 (40-pin DIP). Only two data transfer rates can be selected with this configuration 150 kb/s FM and 300 kb/s MFM.

TABLE 1. CONTROL REGISTER CONFIGURATION 16 MHz

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	500 k	MFM	1
0	0	X	250 k	FM	1
0	1	0	250 k	MFM	0
0	1	1	300 k	MFM (9.6 MHz)	0
1	0	X	250 k	MFM, RST Default	1
1	0	X	125 k	FM, RST Default	1
1	1	X	125 k	FM	0

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TABLE 2. CONTROL REGISTER CONFIGURATION 32 MHz

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	1 M	MFM	1
0	0	X	500 k	FM	1
0	1	0	500 k	MFM	0
0	1	1	300 k	MFM (9.6 MHz)	0
1	0	X	500 k	MFM, RST Default	1
1	0	X	250 k	FM, RST Default	1
1	1	X	250 k	FM	0

TABLE 2. CONTROL REGISTER CONFIGURATION - OPTIONS

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA mode)
0	0	X	300 k	MFM	1
0	0	X	150 k	FM	1

In AT/EISA mode, write pre-compensation can be disabled by a logic high on bit-2 of the Control Register. (see table 4.)

TABLE 4. CONTROL REGISTER CONFIGURATION - AT/EISA MODE

BIT	SIGNAL NAME AND FUNCTION	RESET	CLOCK QUALIFIER
0	Data rate	0	None
1	Data rate	0	None
2	No Write Pre-compensation	0	None
3-7	Reserved	None	None

MASTER STATUS REGISTER

The Master Status Register is an eight-bit, read/write register that contains the status information of the FDC. It can be accessed at any time. The ST37C65 provides a write only register, called Master Status Register 1 (MSR1) which is used only to select power down mode. In power down mode the XTAL oscillator, controller circuitry and all linear circuitry are turned off so that the controller draws very low current. Normal operation is restored by asserting reset to the ST37C65 (see Master Status Register 1).

Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and ST37C65. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD* or WR* during a Command or Result phase and the setting of DIO and RQM is 12μs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24μs. If 1 Mb/s is selected, the delay is 6μs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12μs. The maximum time from

the trailing edge of the last RD* in the result phase to when DB4 (FDC busy) goes low is 12µs.

MASTER STATUS REGISTER 1
(MSR1 - Write Only)
The ST37C65 will enter power down mode, when bit of MSR1 is set to logical "1" and the following conditions are met:

1.The RST pin to the FDC is inactive.
2.Bit 2 in the Operations Register is "SRST= 1".
3.The ST37C65 is a waiting a command from the host

The ST37C65 can also be programmed with external logic to automatically enter power down mode a few msec. after the beginning of idle mode.

Normal operation is restored when the RST pin to the FDC is active and the FDC is reset. This in turn resets bit of MSR1 register to logic 0.

TABLE 5. AT/EISA MODE. MASTER STATUS REGISTER 1 CONFIGURATION

BIT	SIGNAL NAME AND FUNCTION	RESET	CLOCK QUALIFIER
0	Power down mode (PDM)	0	None
1-7	Reserved	None	None

TABLE 6. MASTER STATUS REGISTER BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	FDD 0 busy	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D1	FDD 1 busy	D1B	FDD number is 1 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D2	FDD 2 busy	D2B	FDD number is 2 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D3	FDD 3 busy	D3B	FDD number is 3 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE command.
D4	FDC busy	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
D5	Execution mode	EXM	This bit is set only during execution phase in non-DMA mode. When D5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.

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BIT	NAME	SYMBOL	DESCRIPTION
D6	Data input	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, then transfer is from the processor to Data Register.
D7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking function of "ready" and "direction" to the processor.

TABLE 7. STATUS REGISTER 0 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Unit select 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.
D1	Unit select 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D2	Head select	HS	This flag is used to indicate the state of the head at interrupt.
D3	Not ready	NR	Since drive Ready is always presumed true, this will always be a logic "0" (low).
D4	Equipment check	EC	If the Track "0" signal fails to occur after 77 step pulses per Recalibrate Command, then this flag is set.
D5	Seek end	SE	When the FDC completes the SEEK command, this flag is set to "1" (high).
D6	Interrupt code	IC	See D7.
D7	Interrupt code	IC	D7 = 1 and D6 = 0, invalid command issue. Command which was issued was never started.D7 = 0 and D6 = 0, normal termination of command was completed and properly executed. D7 = 0 and D6 = 1, abnormal termination of command, (AT). Execution of command was started but was not successfully completed.

TABLE 8. STATUS REGISTER 1 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Missing address mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.
D1	Not writeable	NW	During execution of Write Data, Write Deleted Data or Format a Track commands, if the FDC detectes a WP* signal from the FDD, then this flag is set.
D2	No data	ND	During execution of Read Data, Write Deleted Data, or Scan command, if the FDC cannot find the sector specified in the IDR (Internal Data Register), this flag is set. During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the Read a Track command, if the starting sector cannot be found, then this flag is set.
D3	Not used		This bit is always set to "0".
D4	Overrun	OR	If the FDC is set not serviced by the host system during data transfers within a certain time interval, this flag is set.
D5	Data error	DE	When the FDC detects a CRC (Cyclic Redundancy Check) error in either the ID field or the data field, this flag is set.
D6	Not used		This bit is always set to "0".
D7	End od cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.

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TABLE 9. STATUS REGISTER 2 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Missing address	MD	Missing address mark in data field. When data is read from the medium, if FDC cannot find a Data Address Mark of Deleted Data Address Mark, then this flag is set.
D1	Bad cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D2	Scan not	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D3	Scan equal	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D4	Wrong cylinder	WC	This bit is related to the ND bit, and when contents of cylinder on the medium is different from that stored in the IDR, this flag is set.
D5	Data error	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D6	Control mark	CM	During execution of the Read Data or Scan Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D7	Not used		This bit is always set to "0".

TABLE 10. STATUS REGISTER 3 BITS

BIT	NAME	SYMBOL	DESCRIPTION
D0	Unit select 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.
D1	Unit select 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D2	Head select	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D3	Write protected	WP*	This bit is used by the ST37C65 to indicate the status of the Write Protected (WP*) signal from FDD.
D4	Track 0	T0	This bit is used to indicated the status of the Track 0 signal from the FDD.
D5	Ready	RY	This bit will always be a logic "1". Drive is presumed to be ready.
D6	Write protected	WP*	This bit is used to indicate the status of the Write Protected (WP*) signal from FDD.
D7	Not used		This bit is always set to "0".

DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out A0, or written into, the Data Register in order to program or obtain the results after a particular command.The relationship between the Master Status Register and the Data Register and the signals RD*, WR*, and A0 are shown in Table 11.

Table 11. MASTER STATUS AND DATA REGISTER

A0	RD*	WR*	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

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OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving LDOR* and WR*. CS* should not be active when this happens. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to selected the desired disk drive. Table 12 represents the Operations Register.

TABLE 12. OPERATIONS REGISTER

OR0	DSEL	Drive Select, if low and MOEN1 = 1, then DS1* is active. If high and MOEN2 = 1, then DS2* is active, but only in the AT/IEISA mode.
OR1	(X)	This must be a logic 0 for DS1* and DS2* to become active.
OR2	SRST*	Soft reset, active low.
OR3	DMAEN	DMA enable, active in Special and AT/EISA modes. Qualifies DMA and IRQ outputs and DACK* input.
OR4	MOEN1	Motor On enable, inverted output M01* is active only in AT/IEISA mode.
OR5	MOEN2	Motor On enable, inverted output M02* Is active only in AT/EISA mode.
OR6	(X)	Has no defined function. A spare.
OR7	(MSEL)	Mode Select. During a soft reset condition, may be used to select between Special mode (1) and AT/IEISA mode (0).

BASE, SPECIAL, AND AT/EISA MODES

Base, Special, PC AT and EISA modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

Base Mode

After a hardware reset, RST active, the ST37C65 will be held in soft reset, SRST* active, with the normally driven signals, DMA request and IRQ request outputs three-stated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying DMAEN and no soft resets. The Drive Select outputs, DS1* to DS4*, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin RWC* represents Reduce Write Current and is indicative of when write pre-compensation is necessary.

Special Mode

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, SRST*. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing SRST* to be active. Then a read of the Control Register address, LDCR* and places the device in Special mode. The DS1*

through DS4* is again offered in this mode, as is RWC*.

AT/EISA Modes

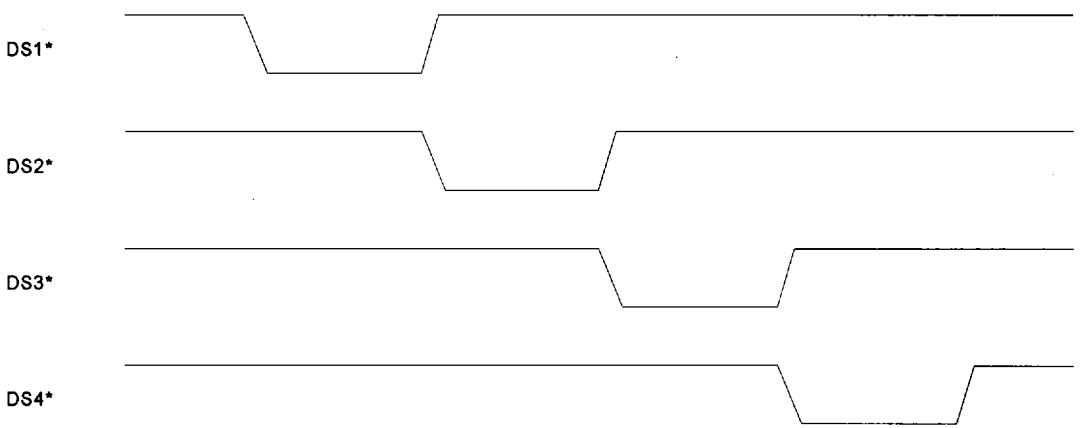
For AT/EISA compatibility, users write to the Operations Register, LDOR* and WR*; this action, performed after a hardware reset, or in the Base mode, initiates AT/EISA mode. AT/EISA mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing SRST* to be active. Then a read of the Control Register address sets the device into AT/EISA mode. The DS* outputs are replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and SRST* are supported and compatible with the current BIOS. RWC* pin function is now RPM* so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low. It can also be used to reduce write current when a slower data rate is selected for a given drive.

POLLING ROUTINE

After any reset the ST37C65, (a hard RST or soft SRST*), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the ST37C65 polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special, AT/EISA modes, if DMAEN is not valid 1ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the ST37C65 occurs continuously between Each drive is polled every 1.024ms, except during the READ/WRITE commands. For mini- floppies, the polling rate is 2.048ms. The drive polling sequence is 1-2-4-3. Note that in the AT/EISA mode, the user will not see the polling at the Drive Select signals. Figure 4 illustrates the Drive Select Polling Timing.

FIGURE 4.

DRIVE SELECT POLLING TIMING



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DEVICE RESETS

The ST37C65 supports both hardware reset (RST pin 19) and a software reset (SRST*) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and selects 250kb MFM (or 125kb FM code dependent) as the data rate (16 MHz input clock) The default data rate for a 32 MHz input clock is 500kb MFM. SRST* will reset the micro controller as did the RST, but will not affect the current data rate selection or the mode RST, when active, will disable the current driver outputs to the disk drive. RST and SRST* will not affect the values set for the internal timers HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 1 illustrates the WD92C32 used as the Data Separator in the ST37C65 system. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

WRITE PRE-COMPENSATION

The ST37C65 maintains the standard first level algorithm to determine when write pre compensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz or 32 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexed gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24)=1, all data will be pre-compensated by ±125ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write pre-compensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ±187ns pre-compensation will be generated. For frequencies other then 16MHz or 32MHz on the CLK1 pin, the pre-compensation values will be two and three clock cycles respectively. When the non-standard 300 kb/s data rate using CLK2 is chosen, the MFM pre-compensation will always be two clock cycles For 9.6 MHz, this is ±208ns. In this case, the PCVAL function is disabled. Write pre-compensation can be disabled by bit-2 of the Control Register for the AT/EISA. The PCVAL input to ST37C65 is ignored if there is no write pre-compensation.

CLOCK GENERATION

This logical block provides all the clocks needed by the ST37C65. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK). SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

MCLK is used by microsequencer. MCLK and MCLK* clock all latches in a two-phase scheme. One micro-instruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 13 presents the Clock Data Rate.

In power down mode the XTAL oscillator and the clok circuitry are turned off.

TABLE 13. CLOCK DATA RATE

DATA RATE	CODE	SCLK	MCLK	WCLK
1Mb/s	MFM	32.0 MHz	8.0 MHz	2.0 MHz
500 kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
500 kb/s	FM	16.0 MHz	8.0 MHz	1.0 MHz
250 kb/s	FM	8.0 MHz	4.0 MHz	500 kHz
250 kb/s	MFM	8.0 MHz	2.0 MHz	500 kHz
125 kb/s	FM	4.0 MHz	2.0 MHz	250 kHz
300 kb/s	MFM	9.6 MHz	2.4 MHz	600 kHz

COMMAND PARAMETERS

The ST37C65 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command phase, Execution phase, and the Result phase.

- Command phase
  The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor.

- Execution phase
  The FDC performs the operation it was instructed to do.

- Result phase
  After completion of the operation, status and other housekeeping information are made available to the processor.

Table 14 lists the 15 ST37C65 commands.

TABLE 14. ST37C65 COMMANDS

- Read Data
- Read Deleted Data
- Write Data
- Write Deleted Data
- Read a Track
- Read ID
- Format a Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Recalibrate
- Sense Interrupt Status
- Specify
- Sense Drive Status
- Seek

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TABLE 15. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

TABLE 16. READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

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TABLE 17. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	0	0	0	1	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

TABLE 18. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	0	0	1	0	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				C					Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
EXECUTION										Data transfer between FDD and main system.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

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TABLE 19. READ TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	0	0	0	1	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				C					Sector ID informatiom prior to command execution. The four bytes are compared against header on floppy disk.
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
EXECUTION										Data transfer between FDD and main system. FDD reads all data fiels from index hole to EOT.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information after command execution.
	R				H					
	R				R					
	R				N					

TABLE 20. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	MF	0	0	1	0	1	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first corrected ID information on the cylinder is stored in Data Register.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					Sector ID information read during Execution Phase from floppy disk.
	R				H					
	R				R					
	R				N					

TABLE 21. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	MF	0	0	1	1	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W				N					Bytes/Sector.
	W				SC					Sectors/Track.
	W				GPL					Gap 3.
	W				D					Filler Byte.
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R				ST0					Status information after command execution.
	R				ST1					
	R				ST2					
	R				C					In this case, the ID information has no meaning.
	R				H					
	R				R					
	R				N					

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TABLE 22. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command code.
	W	X	X	X	X	X	HS	US1	US0	
	W	C								Sector ID informatiom prior to command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
EXECUTION										Data compared between the FDD and main system.
RESULTS	R	ST0								Status information after command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								

TABLE 23. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	1		1	0	0	1	Command code.
	W	X	X	X	X		X	HS	US1	US0	
	W					C					Sector ID informatiom prior to command execution.
	W					H					
	W					R					
	W					N					
	W					EOT					
	W					GPL					
	W					DTL					
EXECUTION											Data compared between FDD and main system.
RESULTS	R					ST0					Status information after command execution.
	R					ST1					
	R					ST2					
	R					C					Sector ID information after command execution.
	R					H					
	R					R					
	R					N					

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TABLE 24. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	DESCRIPTION
COMMAND	W	MT	MF	SK	1		1	1	0	1	Command code.
	W	X	X	X	X		X	HS	US1	US0	
	W					C					Sector ID informatiom prior to command execution.
	W					H					
	W					R					
	W					N					
	W					EOT					
	W					GPL					
	W					STP					
EXECUTION											Data compared between FDD and main system.
RESULTS	R					ST0					Status information after command execution.
	R					ST1					
	R					ST2					
	R					C					Sector ID information after command execution.
	R					H					
	R					R					
	R					N					

TABLE 25. RECALIBRATE

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	1	1	1	Command code.
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 26. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	1	0	0	0	Command code.
	W	X	X	X	X	X	0	US1	US0	
RESULTS	R				ST0					Status information about the FDC at the end of seek operation.
	R				PCN					

TABLE 27. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	0	1	1	Command code.
	W	SRT	SRT	SRT	SRT	HUT	HUT	HUT	HUT	
	W	HLT	HLT	HLT	HLT	HLT	HLT	HLT	ND	

TABLE 28. SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	0	1	0	0	Command code.
	W	X	X	X	X	X	HS	US1	US0	
RESULTS	R				ST3					Status information about FDC.

TABLE 29. SEEK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
COMMAND	W	0	0	0	0	1	1	1	1	Command code.
	W	X	X	X	X	X	0	US1	US0	
	W				NCN					
EXECUTION										Head is positioned over proper cylinder on the diskette.

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TABLE 30. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
A0	Address line 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	Cylinder Number	C stands for the current/selected cylinder (track) number 0 through 255 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D7 - D0	Data Bus	8-bits Data Bus, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the Data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in the ID field.
HLT	Head Load Time	HLT stands for the Head Load Time in FDD (2 to 254 ms in 2 ms increments).
HS	Head Select	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40 pin DIP) or pin 28 (in 44 pin PLCC).
HUT	Head Unload Time	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MultiTrack	If MT is high, a MUTITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the NUMBER of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	Non-DMA Mode	ND stands for operation in the NON-DMA MODE.

TABLE 30. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
PCN	Present Cylinder	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head ar present time.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either READ or WRITE signal.
SC	Sector	SC indicates the number of sectores per cylinder.
SK	Skip	SK stands for SKIP Deleted Data Address Mark.
SRT	Step Rate Time	SRT stabds for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives. In 2's complement format, F (hex)=1 ms, E (hex)=2 ms, etc.
ST0-3	Status 0-3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a SCAN operation, If STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectore are read and compared.
US0-1	Unit Select 0-1	US stands for a selected drive; binary encoded, 1 of 4.

COMMAND DESCRIPTIONS

Read Data

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time Idefined in Ihe Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read of the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the dala bus. After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next seclor is read and output on the data bus. This continuous read function is called a "Multi- sector Read Operation" The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time thal the DACK* for the last byte of data is

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sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes sector). Table 31 lists the Transfer Capacity.

TABLE 31. TRANSFER CAPACITY

Multi-Track MT	MFM/ FM MF	Bytes/ Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3328	26 at side 0
0	1	01	(256) (26) = 6656	or 26 at side 1
1	0	00	(128) (52) = 6656	26 at side 1
1	1	01	(256) (52) = 13312	26 at side 1
0	0	01	(256) (15) = 3840	15 at side 0
0	1	02	(512) (15) = 7680	or 15 at side 1
1	0	01	(256) (30) = 7680	15 at side 1
1	1	02	(512) (30) = 15360	15 at side 1
0	0	02	(512) (8) = 4096	8 at side 0
0	1	03	(1024) (8) = 8192	8 at side 1
1	0	02	(512) (16) = 8192	8 at side 1
1	1	03	(1024) (16) = 16384	8 at side 1

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette. When N=0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexidecimal.

At the completion of the Read Dala command, the head is not unloaded until after Head Unload Time

Interval (specified in the Specity command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 lo 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 6 and set to 0 and 1) respectively.

If Ihe FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit OS in the first Command Word) is not set (SK=0) then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command after reading all the data in the sector. If SK=1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK=1.

During disk data transfers between the FDC and the processor via the data bus, the FDC must be serviced by the processor every 27μs in the FM mode, and every 19μs in the MFM mode or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 32 shows the values for C, H, A, and N, when the processor terminates the command.

TABLE 32. C, H, R, AND N VALUES

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=1	NC
0	1	Less that EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=1	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=1	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=1	NC

Note: NC (No Change): The same value as the one at the begininning of command execution.

Write Datas

A set of nine bytes is required to set the FDC into the Wide Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent complete the data field. If the Terminal Counl signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Wrile Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data

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command for details

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N= 0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data
This command is the same as the Write Data command except a Deleted Data Address mark Is written at the beginning of the data field instead of the normal Data address mark.

Read Deteted Data.
This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK=0) it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK=1, then the FDC skips the sector with the Data Address mark and reads the next sector

Read A Track
This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts leading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to o and 1 respectively.)

Read ID
The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track
The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed inlo N (number ot bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the ST37C65 for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after

each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 33 shows the relationship between N, SC, and GPL for various sector sizes.

TABLE 33. N, SC AND GPL RELATIONSHIP

FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2,3
8" STANDARD FLOPPY					
FM MODE					
	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5 1/4" MINI-FLOPPY					
FM MODE					
	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM MODE					
	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3 1/2" SONY MICRO-FLOPPY					
FM MODE					
	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM MODE					
	256	01	0F	0E	36
	256	02	09	1B	54
	1024	03	05	35	74

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. Ones complement arithmetic is used for comparison (FF=largest number, 00=smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP -8R), and the scan operation is continued. The scan operation continues until one of the following conditions occur the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Regisler 2 is a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and the to terminale the command. Table 34 shows the status of bits SH and SN under various conditions of Scan.

TABLE 34. STATUS OF BITS SH AND SN

STATUS REGISTER 2 COMMAND	BIT-2	BIT-3	COMMENTS
Scan Equal	0	1	DFDD = Dprocessor
	1	0	DFDD ≠ Dprocessor
	0	1	DFDD = Dprocessor
Scan Low or Equal	0	0	DFDD < Dprocessor
	1	0	DFDD > Dprocessor
	0	1	DFDD = Dprocessor
Scan High or Equal	0	0	DFDD > Dprocessor
	1	0	DFDD < Dprocessor

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If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK=0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command If SK=1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK=1), the FDC sets the CM (Conlrol mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors=01, or alternate sectors=02) sectors are read or the MT (Multitrack) is programmed it is necessary to remember that the last sector on tbe track must be read. For example, if STP=02, MT=0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sertor 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27μs (FM mode) or 13μs (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, Ihe SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated At this point FDC interrupt goes high. Bits D0B-D3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operalions may be done on up to four drives at once. No other command can be issued as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be shorter than that set in the Specify command by as much as 1ms.

Recalibrate

Tne function of this command is to retract the Read/Write nead within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated If the Track 0 signal is still low after 255 step pulses have been issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also

applies to the Recalibrate command.

Sense Interrupt Status
An Interrupt signal is generated by the FDC for one of the following reasons:

1 Upon entering the Result phase of
- Read Data command
- Read A Track command
- Read ID command
- Read Deleted Data command
- Write Data command
- Format A Cylinder command
- Write Deleted Data command
- Scan commands

2 Ready Line of FDD changes state
3 End of Seek or Recalibrate command
4 During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor During an Execution phase in non-DMA mode, DBS in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands.

The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued. resets the Interrupt signal and via bits 5, 6, and 7 ot Status Register 0 identifies the cause of the interrupt.

TABLE 35. INTERRUPT CAUSE

BIT-5	BIT-6	BIT-7	CAUSE
0	1	1	Ready line changed state, either polarity.
1	0	0	Normal Termination of Seek or Recalibrate command.
1	1	0	Abnormal Termination of Seek or Recalibrate command.

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the ST37C65 will Set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 7.

The Specify command sets the initial values for each of the three internal timers: The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state This timer is programmable from 16 to 240ms in increments of 16ms (01=16ms, 02=120ms, 0F=240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F=1ms, E=2ms, D=3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/ Write operation starts. This timer is programmable from 2 to 254ms in increments of 2ms (01=2ms, 02=4ms, 03=6ms . . . 7F=254ms).

The time intervals mentioned above are a dirert lunction of tne clock (CLK on pin 23). Times indicated above are for a 16MHz clock; if the clock was reduced to 8MHz, then all time intervals are increased by a factor of 2. If the clock was increased to 32MHz, then all time in tervals are decreased by half.
The choice ot DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-OMA mode is selected; and when ND = 0, the DMA mode is selected.

Sense Drive Status
This command may be used by the processor to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

Invalid
If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set

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to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the ST37C65 is in the Result phase and the contents of Status Register 0 (STD) must be read When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

FIGURE 8. ST37C65 FM MODE FORMAT

GAP (4a) 40x FF	SYNC 6x 00	IAM FC	GAP (1) 26x FF	SYNC 6x 00	IDAM FE	C Y L	H D	S E C	N O	C R C	GAP (2) 11x FF	SYNC 6x 00	DATA AM FB or F8	DATA	C R C	GAP (3)	GAP (4b)

FIGURE 9. ST37C65 MFM MODE FORMAT

GAP (4a) 80x FF	SYNC 12x 00	IAM 3x C2 FC	GAP (1) 50x 4E	SYNC 12x 00	IDAM 3x A1 FE	C Y L	H D	S E C	N O	C R C	GAP (2) 22x 4E	SYNC 12x 00	DATA AM 3x A1 FB F8	DATA	C R C	GAP (3)	GAP (4b)

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T_1	Clock high pulse duration	13.5			ns	
T_2	Clock low pulse duration	13.5			ns	
T_3	Clock rise/fall time			2	ns	
T_4	A0, CS*, DACK* set up time to RD* low	0			ns	
T_5	RD* width	90			ns	
T_6	A0, CS*, DACK* hold time to RD* high	0			ns	
T_8	Data access time from RD* low			90	ns	
T_9	Data bus to float delay from RD* high	10		65	ns	
T_{10}	IRQ reset delay time from RD* high			T_{18}	ns	+150ns
T_{11}	A0, CS*, DACK*, LDCR*, LDOR* set up time to WR* low	0			ns	
T_{12}	WR* width	60			ns	
T_{13}	A0, CS*, DACK*, LDCR*, LDOR* hold time from WR* high	0			ns	
T_{15}	Data set up time to WR* high	80			ns	
T_{16}	Data hold time from WR* high	0			ns	
T_{17}	IRQ reset delay time from WR* high			T_{18}	ns	+150ns
T_{18}	DMA cycle time	52			T_{18}	
T_{19}	DACK* delay time from DMA high	0			ns	
T_{20}	DMA reset delay time from DACK* low			140	ns	
T_{21}	DACK* width	90			ns	
T_{22}	RD* or WR* response from DMA high			48	T_{18}	
T_{23}	RD* delay from DMA	0			ns	
T_{24}	WR* delay from DMA	0			ns	
T_{28}	TC delay from last DMA or IRQ, RD*	0		192	T_{18}	
T_{29}	TC delay from last DMA or IRQ, WR*	0		384	T_{18}	
T_{30}	TC width	60			ns	
T_{31}	Reset width - TTL driven CLK1	60			ns	
T_{32}	Chip access delay from RST low	32			T_{18}	
T_{33}	DIRC* hold & set up to STEP* low	4			T_{18}	
T_{34}	STEP* active time low	24			T_{18}	
T_{35}	DIRC* hold time after STEP*	96			T_{18}	
T_{36}	STEP* cycle time	132			T_{18}	
T_{37}	DSX* hold time from STEP* low	20			T_{18}	
T_{38}	IDX* index pulse width	2			T_{18}	
T_{39}	RDD* active time low	40			ns	
T_{40}	WD* write data width low		1/2		WCLK	

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ABSOLUTE MAXIMUM RATINGS

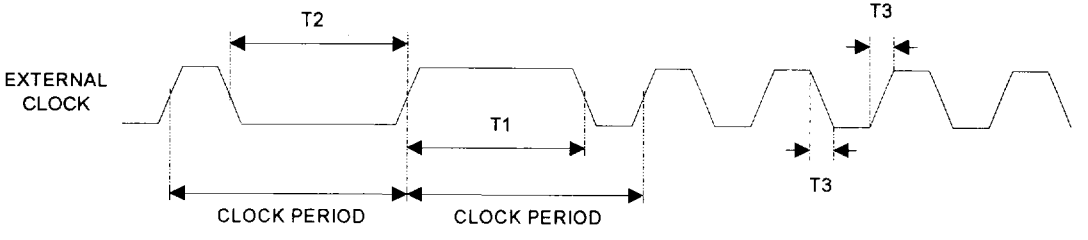
Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level for Dx, IRQ, DMA			0.4	V	I_{OL}= 24 mA
V_{OH}	Output high level for Dx, IRQ, DMA	2.8			V	I_{OH}= -5 mA
V_{OLHC}	Output low-high current open drain			0.4	V	I_{OL}= 24 mA
I_{CC}	Avg. power supply current		5		mA	
I_{CCC}	Power down current		100		µA	
I_{IL}	Input leakage			±10	µA	
V_{ILT}	Input low trashold - "Schmitt"	0.8		1.1	V	
V_{IHT}	Input high trashold - "Schmitt"	1.7		2.0	V	
V_{HYS}	Schmitt trigger hysterisis	0.45			V	

CLOCK TIMING



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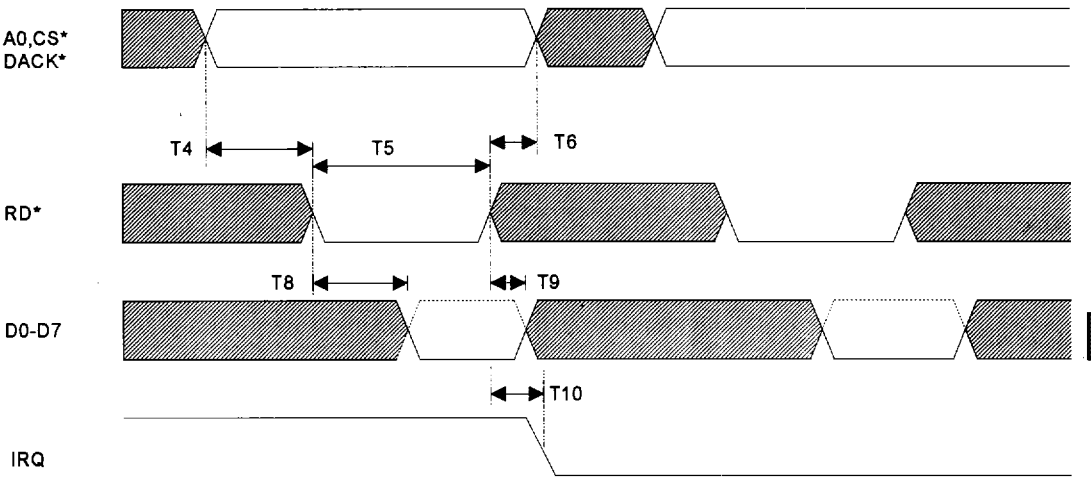
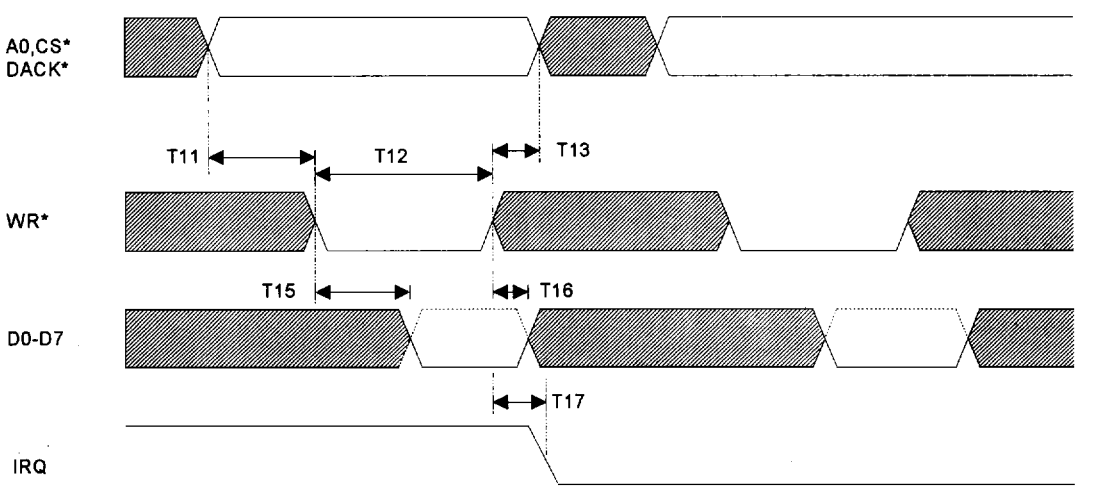
GENERAL READ TIMING



GENERAL WRITE TIMING



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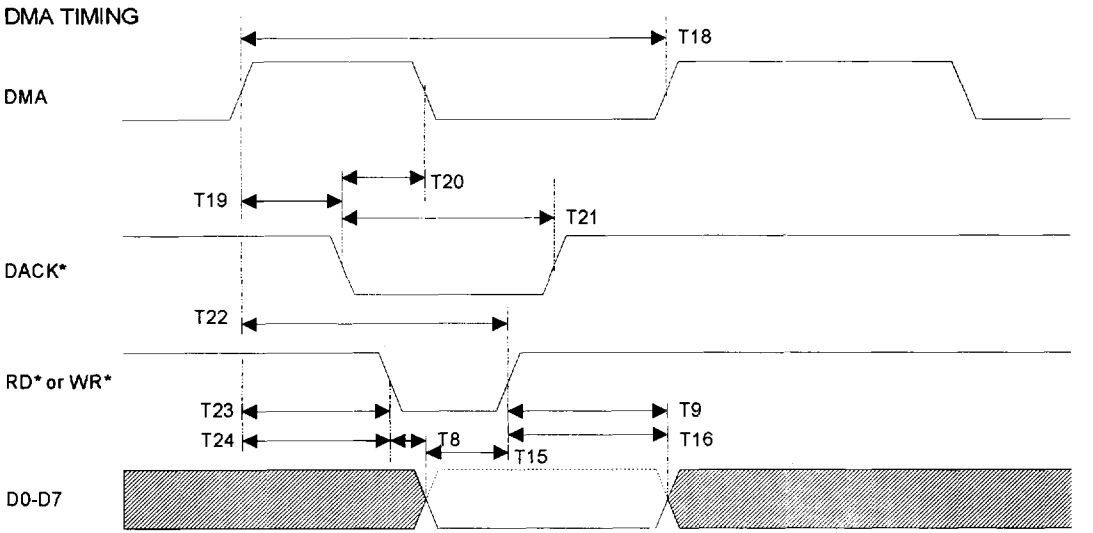
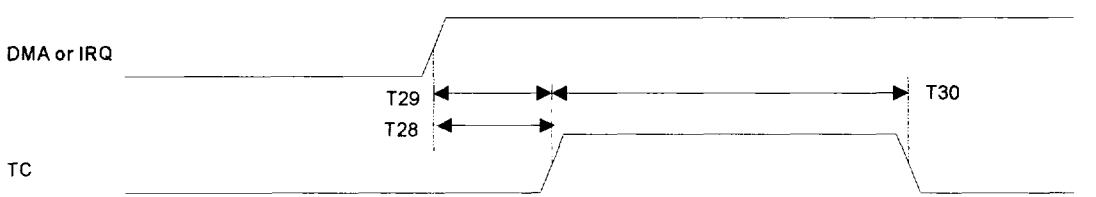
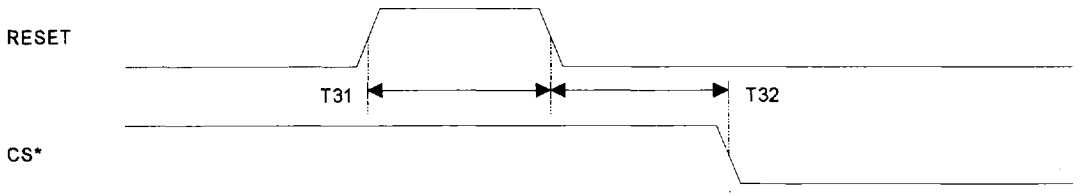
DMA TIMING



TERMINAL COUNT TIMING



RESET TIMING



DISK DRIVE TIMING