16-bit Data Bus One-Time PROM Card

MF4129-F3DAPXX
MF4257-F3DAPXX
MF4513-F3DAPXX
MF41M1-F3DAPXX
MF42M1-F3DAPXX

Connector Type

Two-piece 60-pin

DESCRIPTION

Mitsubishi's One-Time PROM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm × 54mm × 3.4mm). The cards use a 16-bit data bus.
Available in 128K, 256K, 512K, 1 M and 2 M byte capacities, Mitsubishi's One-Time PROM cards are available with either a 60 pin, two-piece connector.

- Buffered interface (without data bus)
- 60-pin connector
- 16-bit data width

FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size.
- Electrostatic discharge protection to 25kV

APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communications
- Industrial
- Consumer

PRODUCT LIST

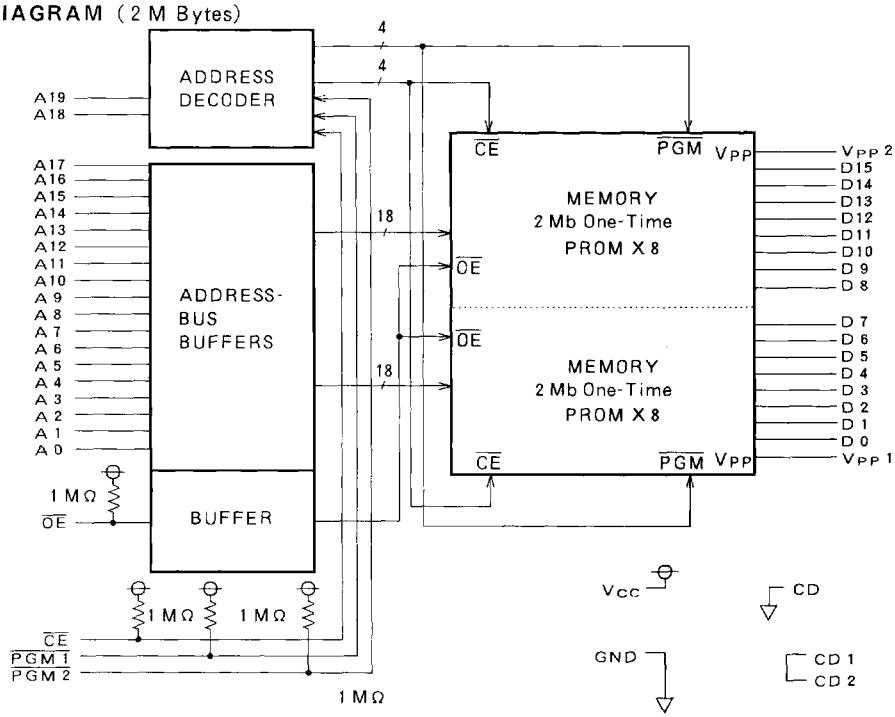
Item / Type name	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF4129-F3DAPXX	128KB	16	200	Two-piece	60	60P-001
MF4257-F3DAPXX	256KB					
MF4513-F3DAPXX	512KB					
MF41M1-F3DAPXX	1 MB					
MF42M1-F3DAPXX	2 MB					

PIN ASSIGNMENT

Two-Piece Type (60-pin) (2 M Bytes)

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	No connection	2	NC	No connection
3	V_{PP} 1	Power supply 1	4	V_{PP} 2	Power supply 2
5	A12	Address input	6	CD 1	Card detect 1
7	A 7		8	A15	Address input
9	A 6		10	A16	NC for ≤128KB types
11	A 5		12	A17	NC for ≤256KB types
13	A 4		14	A18	NC for ≤512KB types
15	A 3		16	A19	NC for ≤ 1 MB types
17	A 2		18	NC	No connection
19	A 1		20	NC	
21	A 0		22	NC	
23	D 0	Data I/O	24	D 8	Data I/O
25	D 1		26	D 9	
27	D 2		28	D10	
29	GND	Ground	30	GND	Ground
31	D 3	Data I/O	32	GND	
33	D 4		34	D11	Data I/O
35	D 5		36	D12	
37	D 6		38	D13	
39	D 7		40	D14	
41	$\overline{CE}$	Card enable	42	D15	
43	A10	Address input	44	NC	No connection
45	$\overline{OE}$	Output enable	46	$\overline{PGM\ 2}$	Program control 2
47	A11	Address input	48	NC	No connection
49	A 9		50	NC	
51	A 8		52	B 0	GND
53	A13		54	B 1	No connection
55	A14		56	B 2	GND
57	$\overline{PGM\ 1}$	Program control 1	58	CD 2	Card detect 2
59	V_{CC}	Power supply	60	V_{CC}	Power supply

BLOCK DIAGRAM (2 M Bytes)



FUNCTION TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (Note 1)	V_{pp} (typ.)	V_{CC} (typ.)	I/O	I_{cc}
Standby	H	X	X	5 V	5 V	High-impedance	Standby
Read	L	L	X	5 V	5 V	Data out	Active
Output disable	L	H	X	5 V	5 V	High-impedance	Active
Word Program	L	H	L	12.5V	6 V	Data in	Active
Program verify	L	L	H	12.5V	6 V	Data out	Active
Page data latch	H	L	H	12.5V	6 V	Data in	Active
Page program	H	H	L	12.5V	6 V	High-impedance	Active
Program inhibit	X	L	L	12.5V	6 V	High-impedance	Active
	X	H	H	12.5V	6 V	High-impedance	Active

Note 1 : $\overline{PGM} = \overline{PGM1} + \overline{PGM2}$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.5~7.0	V
V_{pp}	Supply voltage		−0.5~14.0	V
V_I	Input voltage		−0.5~V_{CC}+0.5 (7.0Max.)	V
V_o	Output voltage		0~V_{CC}	V
T_{opr}	Operating temperature		0~70	℃
T_{stg} 1	Storage temperature 1		−40~80	℃

READ OPERATION

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 50°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} supply voltage		V_{CC}		V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 50°C, V_{CC} = V_{PP} = 4.75 ~ 5.25V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH} = −400 μA		2.4			V
V_{OL}	Low output voltage	I_{OL} = 2.1mA				0.45	V
I_{IH}	High input current	V_I = V_{CC} V				10	μA
I_{IL}	Low input current	V_I = 0V	PGM1 PGM2 CE OE			−20	μA
			Other inputs			−10	
I_{OZH}	High output current in off state	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_O = V_{CC} V				10	μA
I_{OZL}	Low output current in off state	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_O = 0 V				−10	μA
I_{CC} 1・1	Standby V_{CC} supply current	$\overline{CE}$ = V_{IH}, Outputs = open, Other inputs = V_{IH} or V_{IL}	128K			40	mA
			256K			50	
			512K			55	
			1 M			55	
			2 M			55	
I_{CC}1・2	Standby V_{CC} supply current	$\overline{CE}$ ≧ V_{CC} − 0.2V, Outputs = open, Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V	128K			3	mA
			256K				
			512K				
			1 M			5	
			2 M				
I_{CC} 2・1	Active V_{CC} supply current (Minimum cycle)	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, Outputs = open, Other inputs = V_{IH} or V_{IL}	128K			150	mA
			256K			200	
			512K			205	
			1 M			180	
			2 M			180	
I_{CC} 2・2	Active V_{CC} supply current (Minimum cycle)	$\overline{CE}$ = $\overline{OE}$ ≦ 0.2V, Outputs = open, Other inputs ≦ 0.2V or ≧ V_{CC} − 0.2V	128K			110	mA
			256K			160	
			512K				
			1 M			130	
			2 M			130	
I_{PP} 1	Vpp supply current of each V_{PP} pin (V_{PP} 1 or V_{PP} 2)		128K			0.1	mA
			256K				
			512K			0.2	
			1 M			1.0	
			2 M			1.0	

Note 2 : Direction of current flowing into IC is indicated as positive.

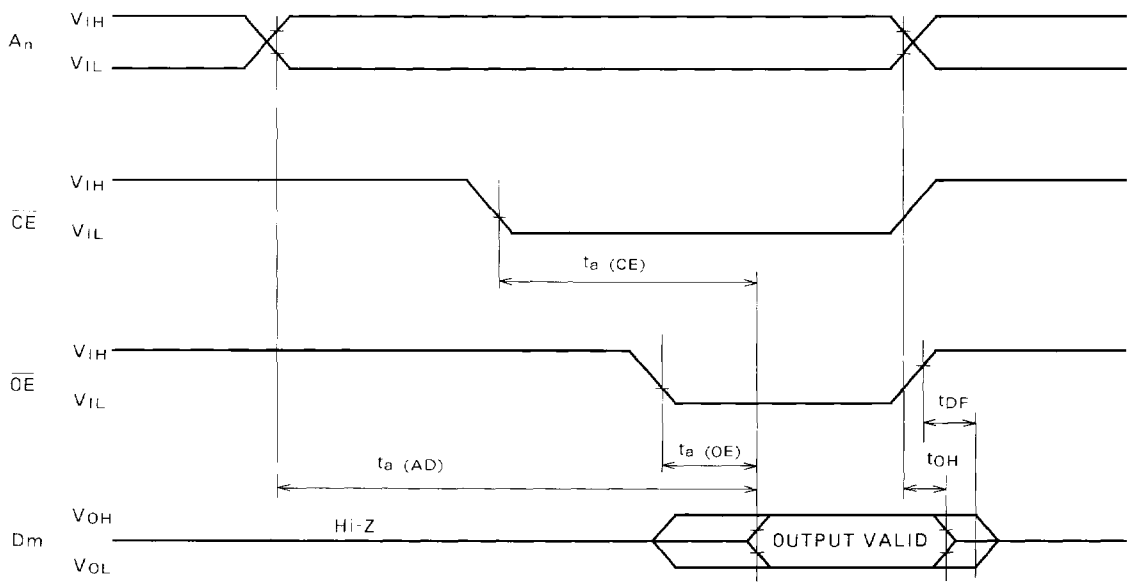
SWITCHING CHARACTERISTICS

Read Cycle (T_a = 0 ~ 50℃, $V_{CC} = V_{PP}$ = 4.75 ~ 5.25V, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(AD)}$	Address access time	$\overline{CE} = \overline{OE} = V_{IL}$			200	ns
$t_{a(CE)}$	Card select access time	$\overline{OE} = V_{IL}$			200	ns
$t_{a(OE)}$	Output enable access time	$\overline{CE} = V_{IL}$			100	ns
t_{DF}	Output disable time (from $\overline{OE}$)	$\overline{CE} = V_{IL}$	0		100	ns
t_{OH}	Data hold time after address change	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note 3 : V_{CC} must be applied simultaneously with V_{PP} and removed simultaneously with V_{PP}.

TIMING DIAGRAM (READ OPERATION)



Note 4 : Test conditions

Input pulse levels		: V_{IL} = 0.45V, V_{IH} = 0.8 × V_{CC} V
Input pulse rise, fall time		: $t_r = t_f$ = 10ns
Reference voltage	input	: V_{IL} = 0.8V, V_{IH} = 0.7 × V_{CC} V
	output	: V_{OL} = 0.8V, V_{OH} = 2.0V
		(t_{DF} is measured when the output voltage is ±500mV from the steady state.)
Load		: 100pF + 1TTL gate (except for measurwent)
		: 5pF + 1TTL gate (for t_{DF} measuring)

PROGRAM OPERATION

RECOMMENDED OPERATING CONDITIONS (T_a=20~30℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} supply voltage	12.2	12.5	12.8	V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V

ELECTRICAL CHARACTERISTICS (T_a=20~30℃, V_{CC}=5.75~6.25V, V_{PP}=12.2~12.8V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH}=−400μA		2.4			V
V_{OL}	Low output voltage	I_{OL}=2.1mA				0.45	V
I_{IH}	High input current	V_I=V_{CC} V	Other inputs			10	μA
I_{IH}	Low input current	V_I=0V	$\overline{CE}$ $\overline{OE}$ $\overline{PGM1}$ $\overline{PGM2}$			−20	μA
			Other inputs			−10	
$I_{CC3 \cdot 1}$	Active V_{CC} supply current	Inputs=V_{IH} or V_{IL}, Outputs=open	128K			150	mA
			256K			210	
			512K			320	
			1 M			250	
			2 M			370	
$I_{CC3 \cdot 2}$	Active V_{CC} supply current	Inputs≦0.2V or ≧V_{CC}−0.2V, Outputs=open	128K			70	mA
			256K			120	
			512K			220	
			1 M			200	
			2 M			320	
$I_{PP2 \cdot 1}$	V_{PP} supply current of each V_{PP} pin (V_{PP1} or V_{PP2})	$\overline{CE}$=V_{IL}<WORD PROGRAM>	128K			70	mA
			256K				
			512K			75	
			1 M			50	
			2 M			60	
$I_{PP2 \cdot 2}$		$\overline{CE}$=V_{IH}<PAGE PROGRAM>	128K			120	mA
			256K				
			512K			125	
			1 M			120	
			2 M			130	

Note 5 : Direction of current flowing into IC : is indicated positive.

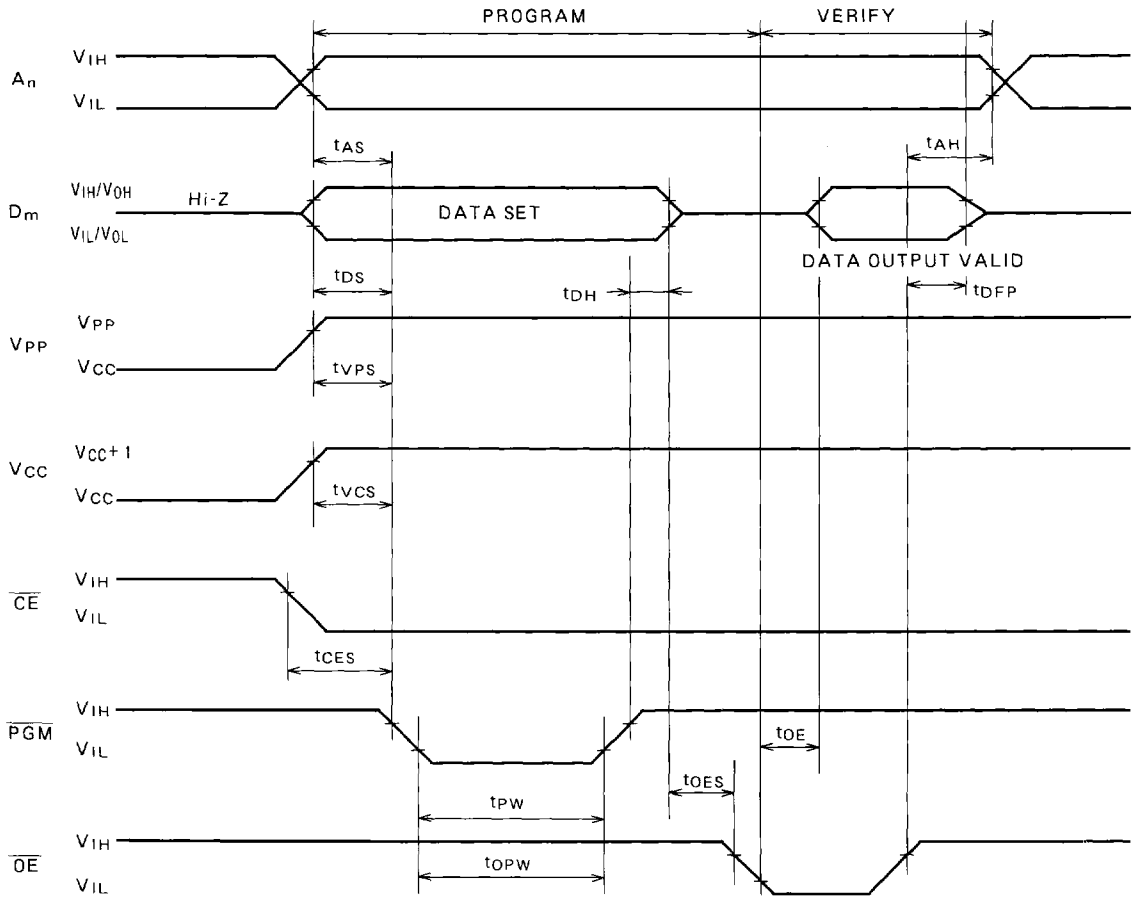
WORD PROGRAM

SWITCHING CHARACTERISTICS (T_a=20~30℃, V_{CC}=5.75~6.25V, V_{PP}=12.2~12.8V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address setup time	2			μs
t_{OES}	$\overline{OE}$ setup time	2			μs
t_{DS}	Data setup time	2			μs
t_{AH}	Address hold time	0			μs
t_{DH}	Data hold time	2			μs
t_{DFP}	Output disable time (from $\overline{OE}$)	0		180	ns
t_{VCS}	V_{CC} setup time	2			μs
t_{VPS}	Vpp setup time	2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width	0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width	0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time	2			μs
t_{OE}	Data valid from $\overline{OE}$			200	ns

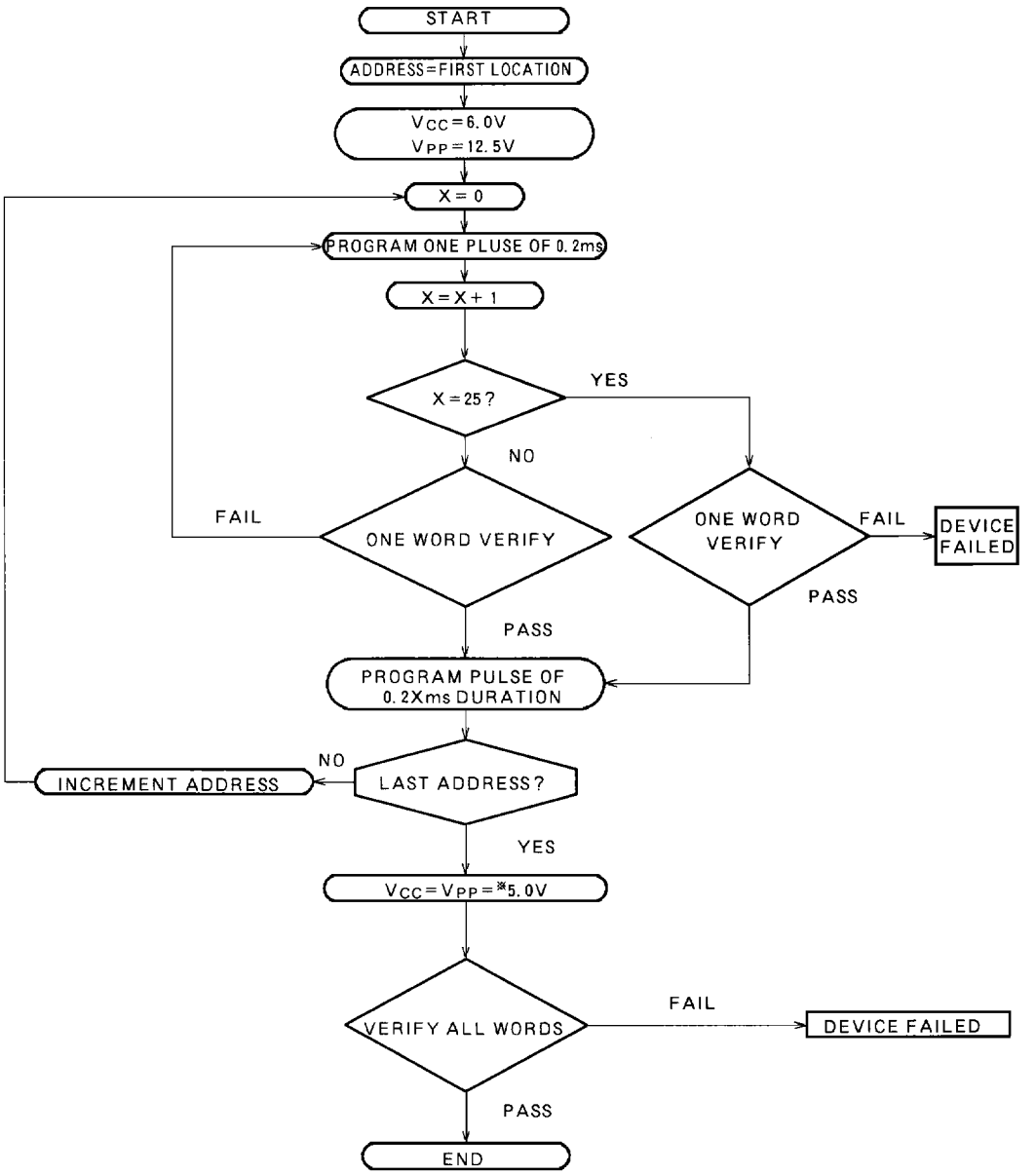
Note 6 : V_{CC} must be applied simultaneously with Vpp and removed simultaneously with V_{PP}.

WORD PROGRAM
TIMING DIAGRAM (PROGRAM OPERATION)



Note 7 : Test conditions
Input pulse levels : $V_{IL}=0.45V$, $V_{IH}=0.8\times V_{CC}$ V
Input pulse rise, fall time : $t_r=t_f=10ns$
Reference voltage input : $V_{IL}=0.8V$, $V_{IH}=0.7\times V_{CC}$ V
output : $V_{OL}=0.8V$, $V_{OH}=2.0V$
(t_{DFP} is measured when the output voltage is ±500mV from the steady state.)

WORD PROGRAMMING ALGORITHM FLOW CHART



※4.75V≦VCC=VPP≦5.25V

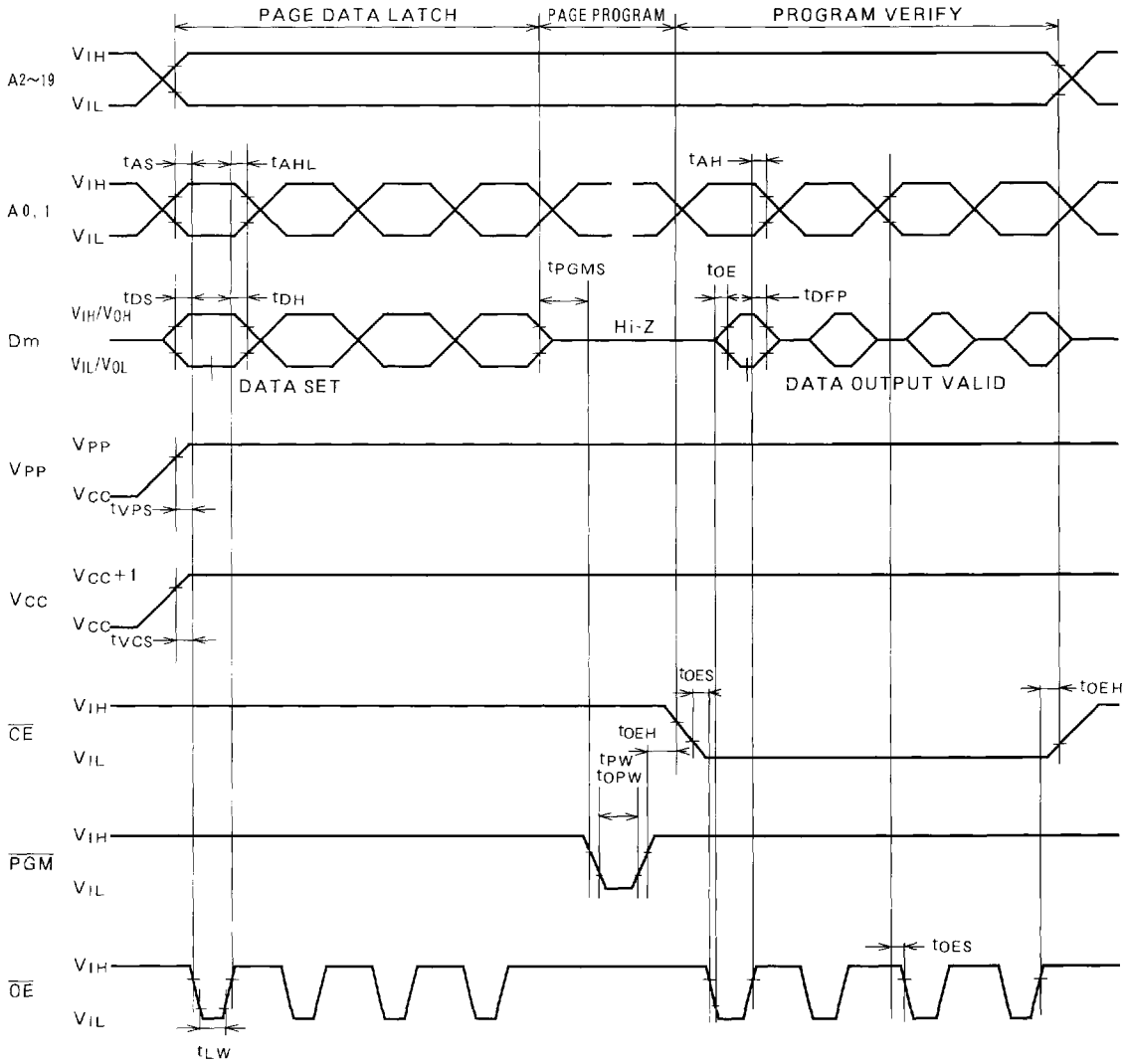
PAGE PROGRAM

SWITCHING CHARACTERISTICS (T_a=20~30℃, V_{CC}=5.25~6.25V, V_{PP}=12.2~12.8V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address setup time	2			μs
t_{OES}	$\overline{OE}$ setup time	2			μs
t_{DS}	Data setup time	2			μs
t_{AH}	Address hold time	0			μs
t_{AHL}		2			μs
t_{DH}	Data hold time	2			μs
t_{DFP}	Output disable time (from $\overline{OE}$)	0		180	ns
t_{VCS}	V_{CC} setup time	2			μs
t_{VPS}	V_{PP} setup time	2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width	0.19	0.20	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width	0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time	2			μs
t_{OE}	Data valid from $\overline{OE}$	0		200	ns
t_{LW}	Data latch time	1			μs
t_{PGMS}	$\overline{PGM}$ setup time	2			μs
t_{CEH}	$\overline{CE}$ hold time	2			μs
t_{OEH}	$\overline{OE}$ hold time	2			μs

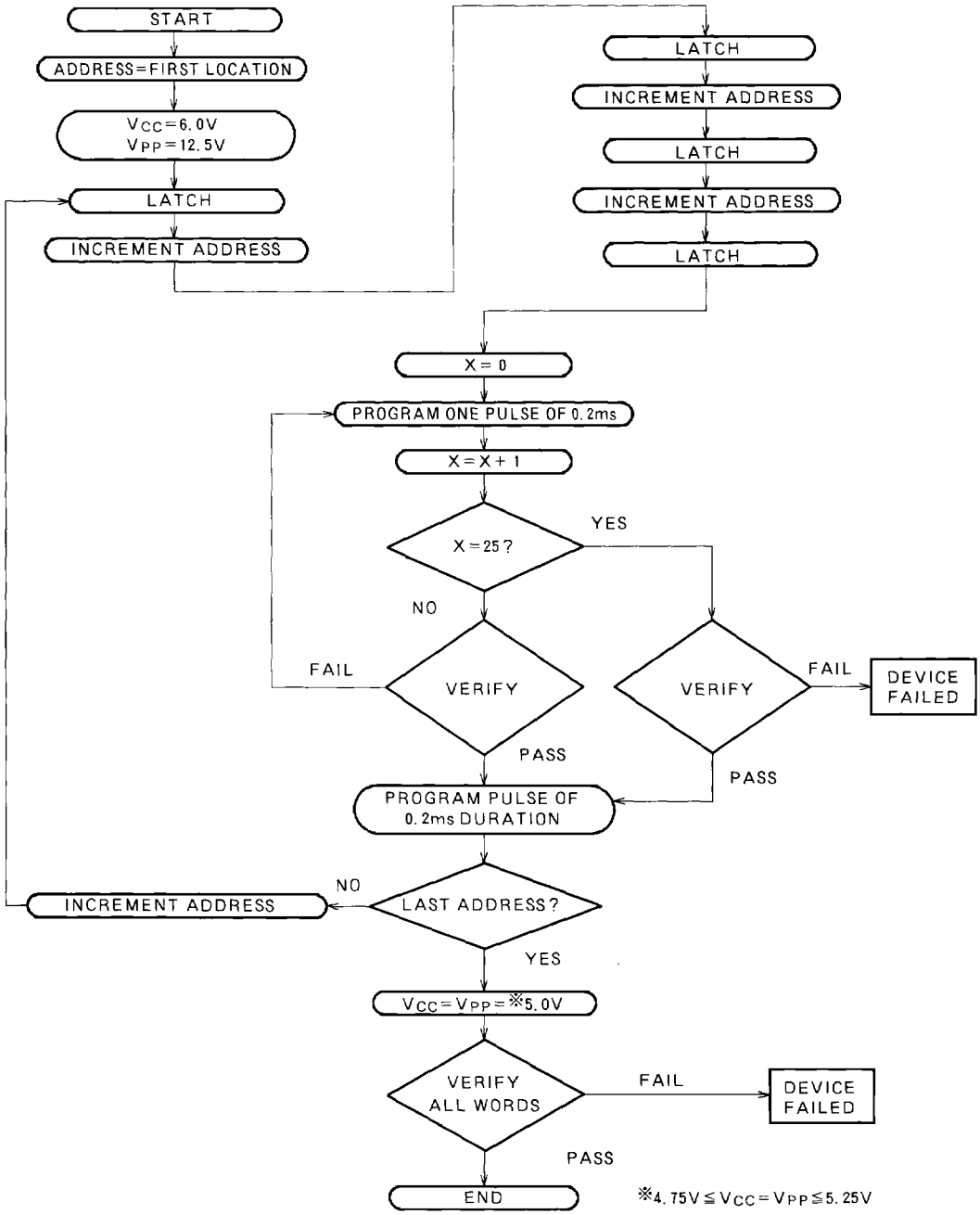
Note 8 : V_{CC} must be applied simultaneously with V_{PP} and removed simultaneously with V_{PP}.

PAGE PROGRAM TIMING DIAGRAM (PROGRAM OPERATION)



Note 9 : Test conditions
Input pulse levels : $V_{IL}=0.45$ V, $V_{IH}=0.8\times V_{CC}$ V
Input pulse rise, fall time : $t_r=t_f=10$ns
Reference voltage input : $V_{IL}=0.8$ V, $V_{IH}=0.7\times V_{CC}$ V (tDFP is measured when the output voltage
output : $V_{IL}=0.8$ V, $V_{IH}=2.0$ V is ±500mV from the steady state.)

PAGE PROGRAMMING ALGORITHM FLOW CHART



CAPACITANCE

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f= 1 MHz, T_a=25℃	128K			30	pF
			256K			40	
			512K			40	
			1 M			40	
			2 M			40	
C_O	Output capacitance	V_O=GND, V_O=25mVrms, f= 1 MHz, T_a=25℃	128K			35	pF
			256K			35	
			512K			50	
			1 M			50	
			2 M			80	

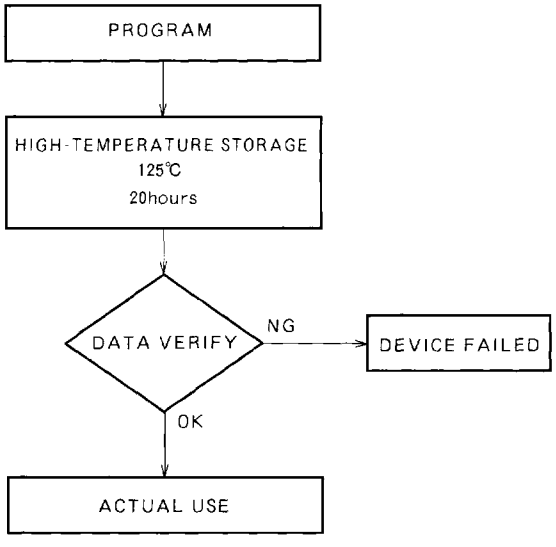
Note 10 : These items are not 100% tested.

DEVICE IDENTIFIER MODE

This card does not support a device identifier mode.
Do not apply voltages exceeding 7 V to pin A 9.

RECOMMENDED SCREENING CONDITIONS

The following screening test is recommended before using a card which you have programmed for evaluation. If you use cards for mass produchion, it is recommended that the manufacturer programs them.



Note 11 : The color of the panels might be affected by high-temperature storage.
After the data-verify test, it is cecommended that you apply labels of you own desigh to the cad parel surfaces.