National Semiconductor

ADVANCED INFORMATION

# 54F/74F395
# 4-Bit Cascadable Shift Register with TRI-STATE® Outputs

## General Description

The 'F395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs ($D_0$–$D_3$) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input ($D_S$) is loaded into the $Q_0$ flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0$-$Q_1$-$Q_2$-$Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

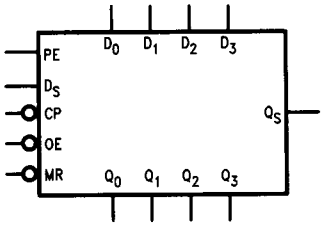
The Master Reset ($\overline{MR}$) is an asynchronous Active LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The TRI-STATE output buffers are designed to drive heavily loaded TRI-STATE buses or large capacitive loads. The Active LOW Output Enable ($\overline{OE}$) controls all four TRI-STATE buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is LOW. The outputs are in the high impedance (OFF) state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output ($Q_S$) is tied to the Serial Data input ($D_S$) of the next device for serial expansion applications. The $Q_S$ output is not affected by the TRI-STATE buffer operation.

## Features

- 4-Bit parallel load shift register
- Independent TRI-STATE buffer outputs
- Separate $Q_S$ output for serial expansion
- Asynchronous master reset

## Logic Symbols

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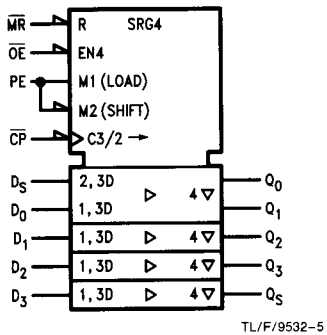
**IEEE/IEC**

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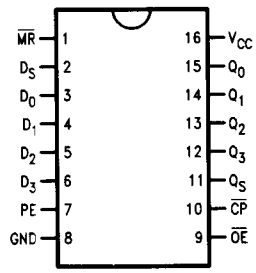
## Connection Diagrams

**Pin Assignment for DIP, SOIC and Flatpak**

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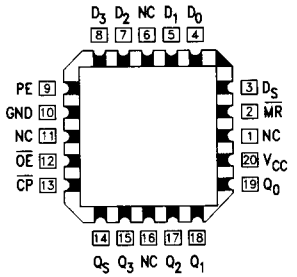
**Pin Assignment for LCC and PCC**

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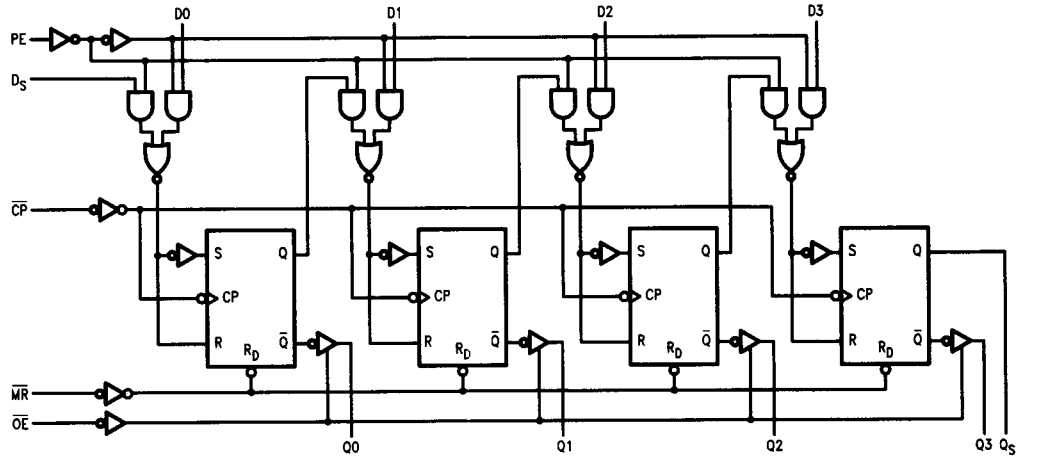
**Mode Select-Function Tables**

| Register Operating Modes | Inputs | | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | $\overline{CP}$ | PE | $D_s$ | $D_n$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
| Reset (clear) | L | X | X | X | X | L | L | L | L |
| Shift Right | H | ⌐ | L | L | X | L | $q_0$ | $q_1$ | $q_2$ |
| | H | ⌐ | L | H | X | H | $q_0$ | $q_1$ | $q_2$ |
| Parallel Load | H | ⌐ | H | X | L | L | L | L | L |
| | H | ⌐ | H | X | H | H | H | H | H |

| TRI-STATE Buffer Operating Modes | Inputs | | Outputs | |
|---|---|---|---|---|
| | $\overline{OE}$ | $Q_n$(Register) | $Q_0, Q_1, Q_2, Q_3$ | $Q_s$ |
| Read | L | L | L | L |
| | L | H | H | H |
| Disable Buffers | H | L | Z | L |
| | H | H | Z | H |

H = HIGH Voltage Level
L = LOW Voltage Level
$q_n$ = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock Transition
X = Immaterial
Z = High Impedance
⌐ = HIGH-to-LOW transition

## Logic Diagram

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.