SED2000

CMOS VFD Driver

Technical Manual

S-MOS Systems, Inc.
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Version 1.0 (Preliminary)

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Table of Contents

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1.0 GENERAL DESCRIPTION

1.1 DESCRIPTION

The SED2000 is a CMOS LSI dot-matrix vacuum fluorescent display anode and grid driver. It has 40 high-voltage anode outputs in 2 × 20 blocks and 20 high-voltage grid outputs.

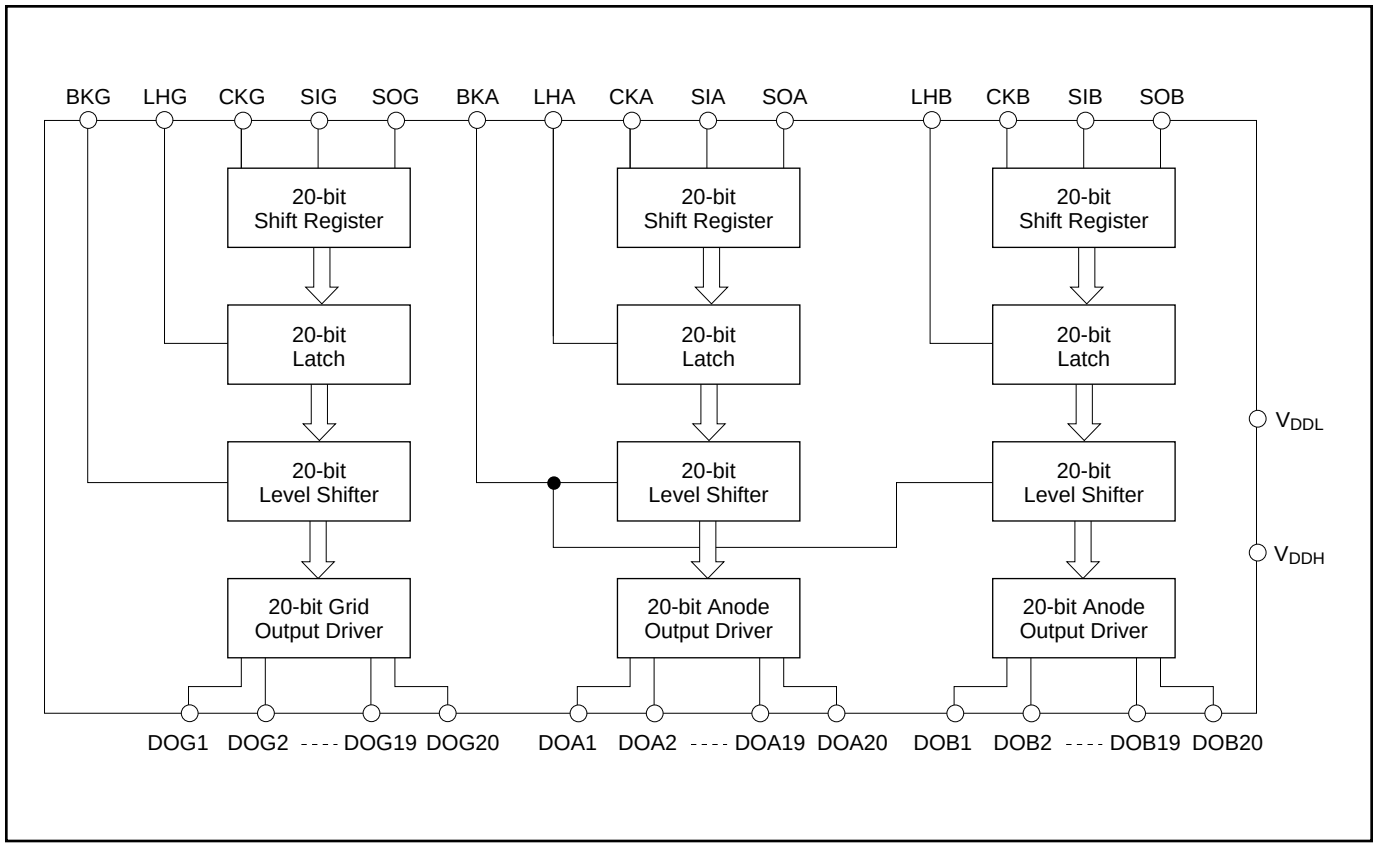
The SED2000 has independent serial inputs and outputs for each 20-element block which feature data transfer rates of up to 4 Mbits/s. The daisy-chain serial data transfer system simplifies controller requirements. An automatic shutdown circuit turns off output drivers when power is removed from the logic circuits, simplifying power supply design.

SED2000 uses a 5V logic supply and a 30 to 70V display supply, and is available in 80-pin plastic flatpacks.

1.2 FEATURES

- 40 anode and 20 grid output drivers
- 70V, 10mA grid drive capability
- 70V, 2mA anode drive capability
- Automatic shutdown circuit
- Up to 4 Mbits/s serial data transfer rate
- Daisy-chain data transfer system for cascaded operation
- Silicon-gate CMOS technology
- 5V logic supply
- 30 to 70V display supply
- 80-pin plastic flatpack (QFP5-80pin)

1.3 BLOCK DIAGRAM



1.4 PIN DESCRIPTION

Pin Name	Pin No.	Function
DO_{A20} – DO_{A1} DO_{B20} – DO_{B1} DO_{G20} – DO_{G1}	23 – 42 3 – 22 43 – 62	CMOS outputs for driving anodes. CMOS outputs for driving anodes. CMOS outputs for driving grids.
SI_A SI_B SI_C	76 65 71	Serial data inputs for shift registers.
SO_A SO_B SO_C	75 66 70	Serial data outputs of shift registers.
BLK_A BLK_C	73 68	Blanking inputs. H level inputs turn all displays off.
LH_A LH_B LH_C	74 79 69	Latch clock inputs. The contents of shift registers are read out at LH = H, and are latched at the falling edge of LH.
CK_A CK_B CK_C	77 80 72	Shift clock inputs. Data inputs from SI are read in at CK = L,_, and data are produced from SO at the rising edge of CK.
V_{DDH} V_{DDL} V_{SS}	1, 64 67 78	Power supply for drivers. (70V) Power supply for logic circuits. (5V) Power supply (0V)

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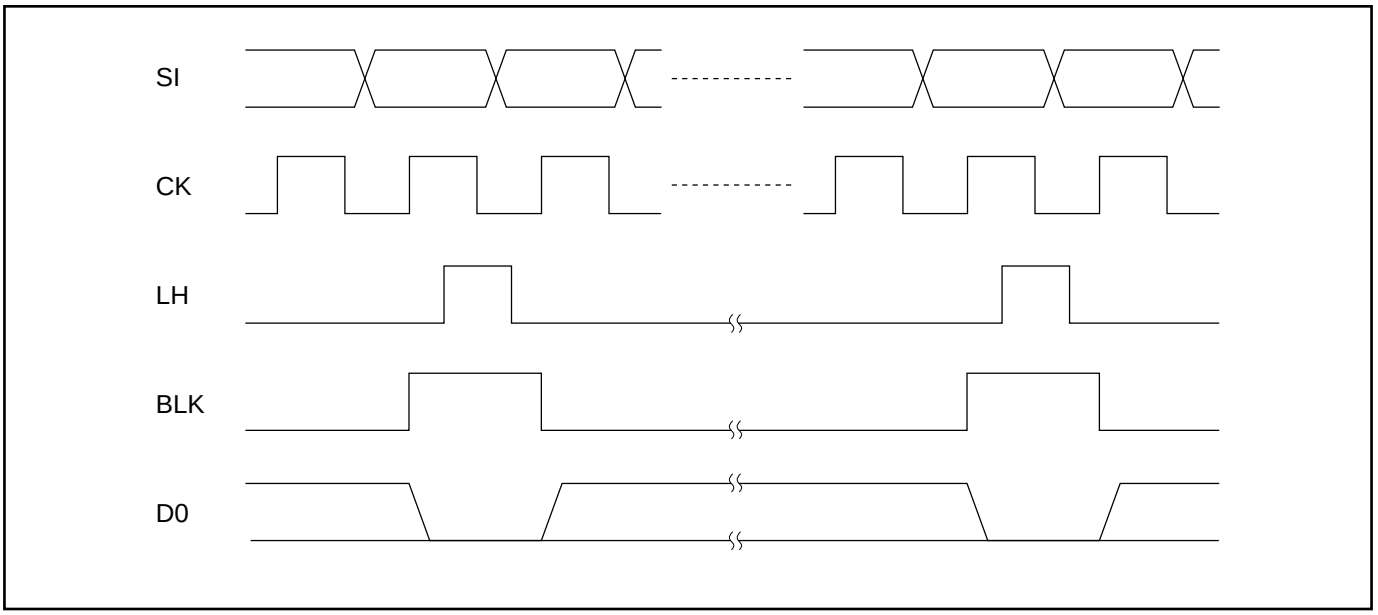
2.0 ELECTRICAL CHARACTERISTICS

2.1 EXAMPLE OF TIMING



Note: Be sure to input a high level to LH pin during BLK = H. If a high level is given to LH pin during BLK = L, the current consumption increases when DO changes the output level from high to low.

2.2 ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V

Parameter		Symbol	Rating	Unit
Supply voltage (1)		V_{DDH}	–0.3 to 70	V
Supply voltage (2)		V_{DDL}	–0.3 to 7.0	V
Driver output voltage		V_{DO}	V_{SS} – 0.3 to V_{DDH} + 0.3	V
Output voltage		V_O	V_{SS} – 0.3 to V_{DDL} + 0.3	V
Input voltage		V_I	V_{SS} – 0.3 to V_{DDL} + 0.3	V
Driver H level all output current	Anode	I_{OHDO}	–5.0 to 0	mA
	Grid		–15.0 to 0	mA
Driver L level all output current		I_{OLDO}	0 to 1.0	mA
Operating temperature		T_{OPR}	–10 to 70	°C
Storage temperature		T_{STG}	–50 to 125	°C
Power dissipation		P_D	0 to 250	mW
Solering temperature/time		T_{SOL}	260°C, 10s (at lead)	—

2.3 RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage (1)	V_{DDH}	—	30	60	70	V
Supply voltage (2)	V_{DDL}	—	4.5	5.0	5.5	V
Input voltage	V_I	—	0	—	V_{DDL}	V
Input logic level	V_{LL}	—	—	1.55*	—	V
H output current	I_{OH}	Grid driver	—	–10	—	mA
		Anode driver	—	–0.5	—	
Clock frequency	f_{CK}	CK, In-cascade	0	—	4	MHz
Clock pulse width	t_{WCK}	CK	125	—	—	ns
Setup time	t_{SU}	—	70	—	—	ns
Hold time	t_H	—	0	—	—	ns
Latch pulse width	t_{WL}	LH	250	—	—	ns

*: TTL input level

2.4 DC ELECTRICAL CHARACTERISTICS

V_{SS} = 0V, V_{DDL} = 5V, V_{DDH} = 60V, Ta = 25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H input voltage	V_{IH}	—	2.4	—	V_{DDL}	V
L input voltage	V_{IL}	—	0	—	0.7	V
H input current	I_{IH}	V_{IH} = 5.0V	—	—	0.1	µA
L input current	I_{IL}	V_{IL} = 0V	10	33	100	µA
H output current (1)	I_{OH1}	V_{OH1} = 4.6V, SO	—	–1.4	–0.44	mA
L output current (1)	I_{OL1}	V_{OL1} = 0.4V, SO	0.5	1.5	—	mA
H output current (2)	I_{OH2}	V_{OH} =55V, DO_{An} (Anode)	—	—	–2	mA
H output current (3)	I_{OH3}	V_{OH} =55V, DO_{Gn} (Grid)	—	—	–10	mA
L output current (2)	I_{OL2}	V_{OL2} = 5.0V, DO	–0.5	1.0	—	mA
Supply current (V_{DDL})	I_{DDL}	f_{CK} = 4MHz	—	—	5	mA
Supply current (V_{DDH})	I_{DDH}	Fixed outputs	—	—	0.1	mA

2.5 SWITCHING CHARACTERISTICS

V_{SS} = 0V, V_{DDL} = 5V, V_{DDH} = 60V, Ta = 25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Set up time for latch	t_{SUL}	—	125	—	—	ns
Hold time for latch	t_{HL}	—	0	—	—	ns
SO rise up time	t_{rSO}	—	—	—	50	ns
SO fall down time	t_{fSO}	—	—	—	50	ns
CK – SO delay time	t_{dSO}	—	—	—	125	ns
DO rise up time	t_{rDO}	—	—	—	0.5	µs
DO fall down time	t_{fDO}	—	—	—	1.0	µs
BLK – DO delay time	t_{dDO}	—	—	—	2.0	µs

2.6 MEASURING CONDITION FOR SWITCHING CHARACTERISTICS

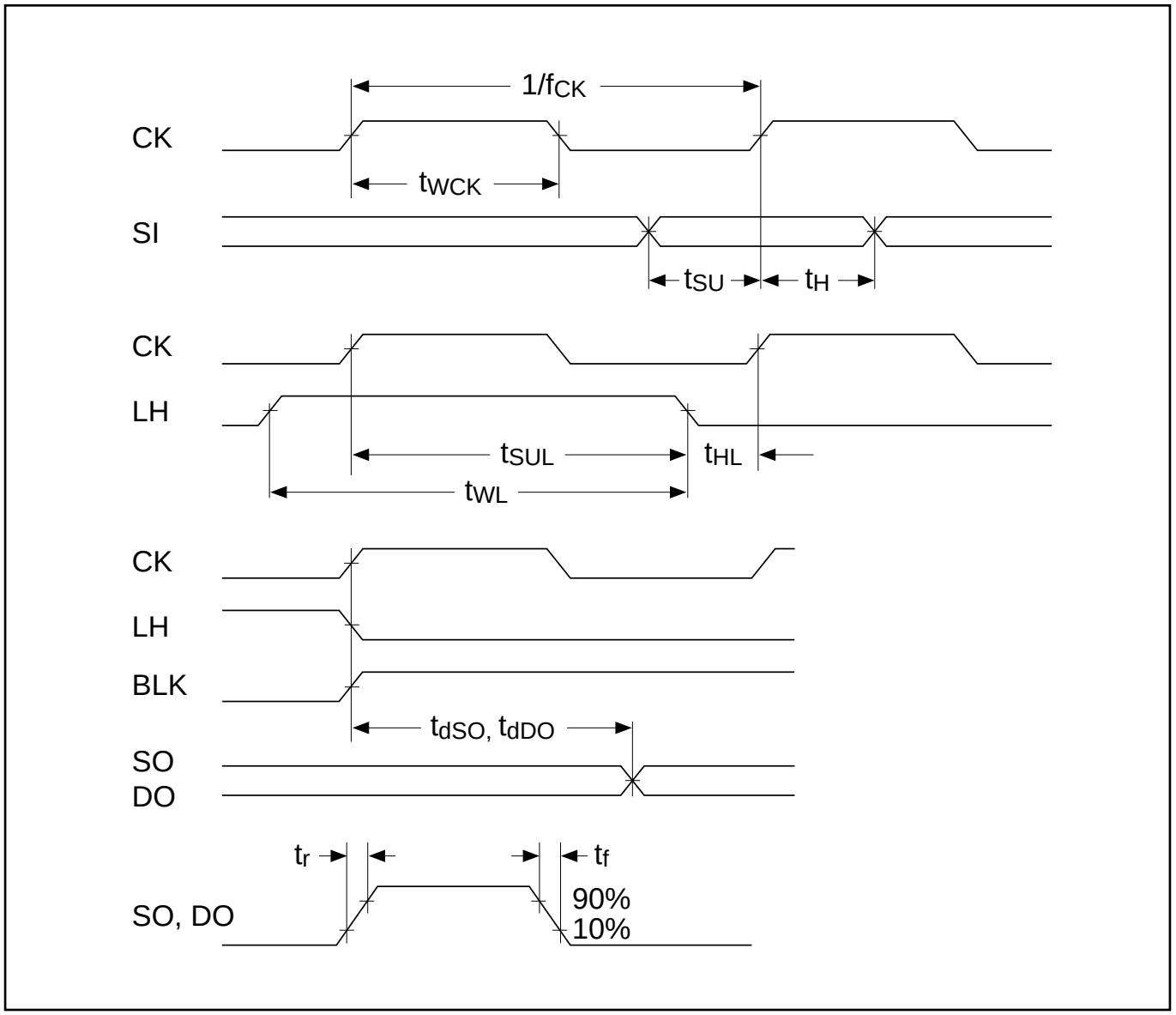
2.6.1 Input Signal

- Amplitude: 0 to 5V
- Rise up time and fall down time: 15ns or less
- Measuring voltage: 2.5V

2.6.2 Output Signal

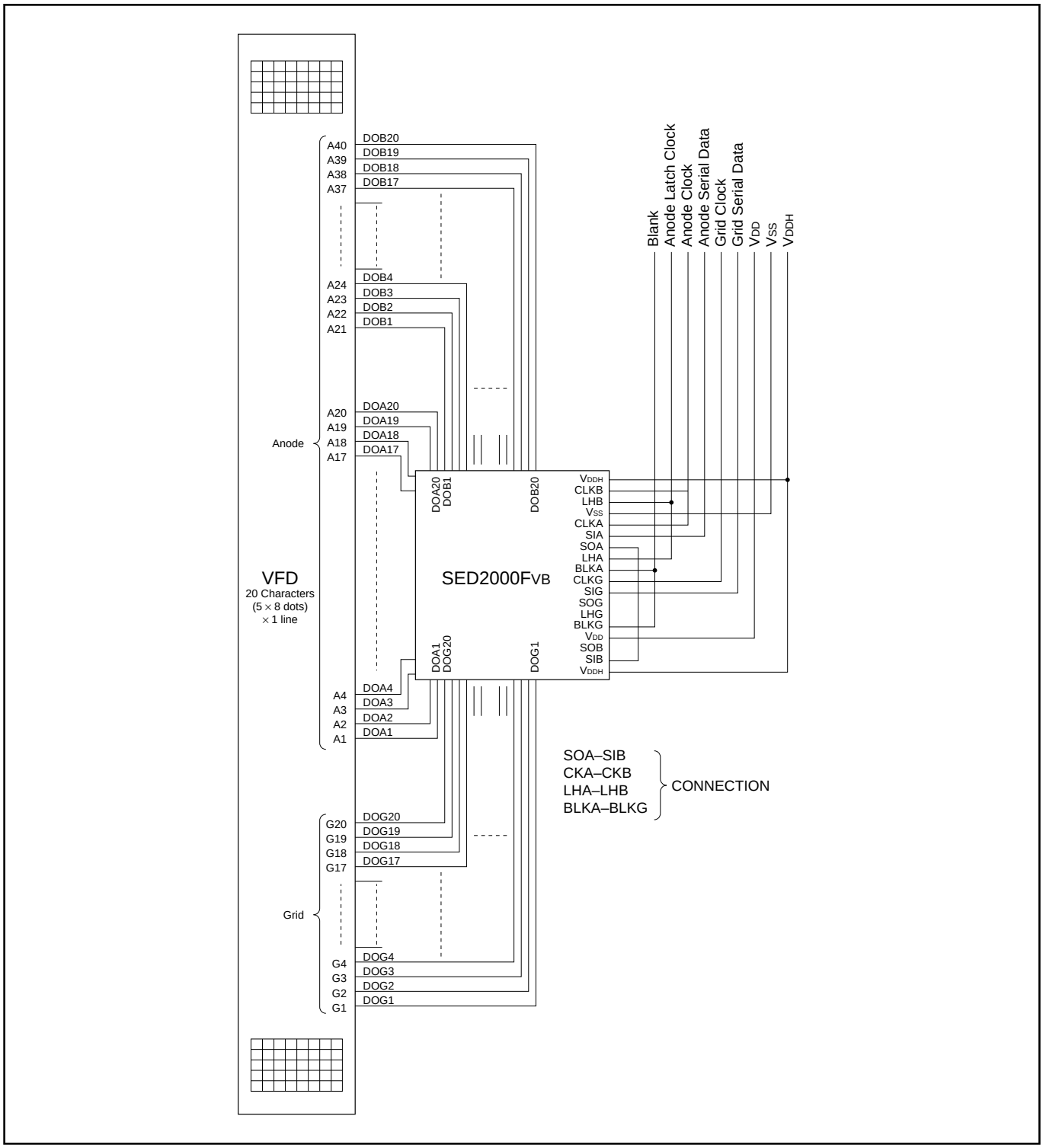
- Nominal load: (13pF, 10MΩ)
- Measuring voltage: 2.5V or 1/2 level of amplitude

2.6.3 Timing Chart

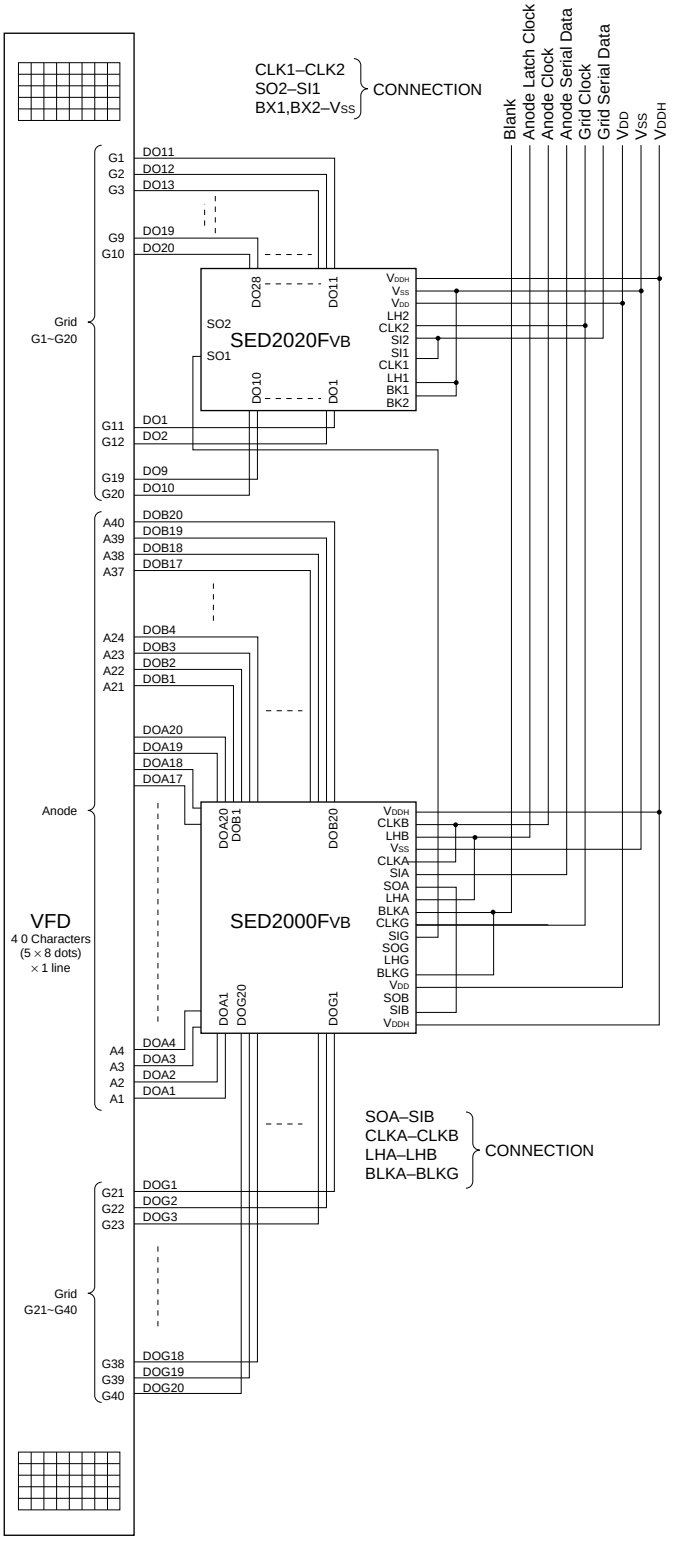


3.0 TYPICAL CONNECTIONS

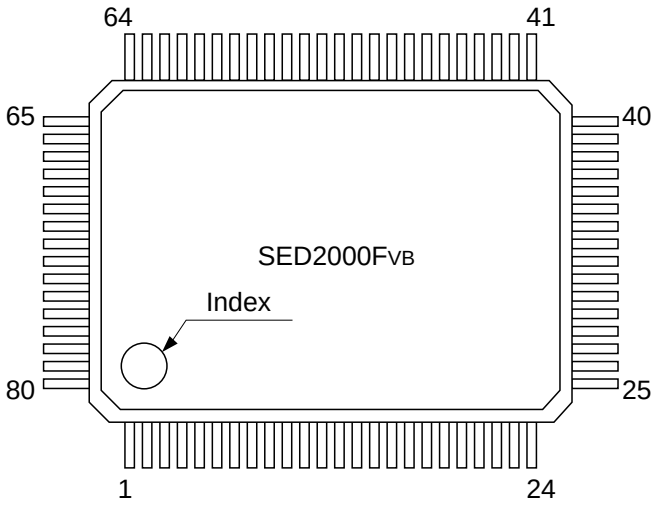
3.1 EXAMPLE OF CONNECTING SED2000F$_{VB}$ TO VFD (1)



3.2 EXAMPLE OF CONNECTING SED2000F$_{VA}$ TO VFD (2)



4.0 PINOUT



Pin		Pin		Pin		Pin	
Number	**Name**	**Number**	**Name**	**Number**	**Name**	**Number**	**Name**
1	V_{DDH}	21	DOB2	41	DOA2	61	DOG2
2	NC	22	DOB1	42	DOA1	62	DOG1
3	DOB20	23	DOA20	43	DOG20	63	NC
4	DOB19	24	DOA19	44	DOG19	64	V_{DDH}
5	DOB18	25	DOA18	45	DOG18	65	SIB
6	DOB17	26	DOA17	46	DOG17	66	SOB
7	DOB16	27	DOA16	47	DOG16	67	V_{DDL}
8	DOB15	28	DOA15	48	DOG15	68	BKG
9	DOB14	29	DOA14	49	DOG14	69	LHG
10	DOB13	30	DOA13	50	DOG13	70	SOG
11	DOB12	31	DOA12	51	DOG12	71	SIG
12	DOB11	32	DOA11	52	DOG11	72	CKG
13	DOB10	33	DOA10	53	DOG10	73	BKA
14	DOB9	34	DOA9	54	DOG9	74	LHA
15	DOB8	35	DOA8	55	DOG8	75	SOA
16	DOB7	36	DOA7	56	DOG7	76	SIA
17	DOB6	37	DOA6	57	DOG6	77	CKA
18	DOB5	38	DOA5	58	DOG5	78	V_{SS}
19	DOB4	39	DOA4	59	DOG4	79	LHB
20	DOB3	40	DOA3	60	DOG3	80	CKB

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