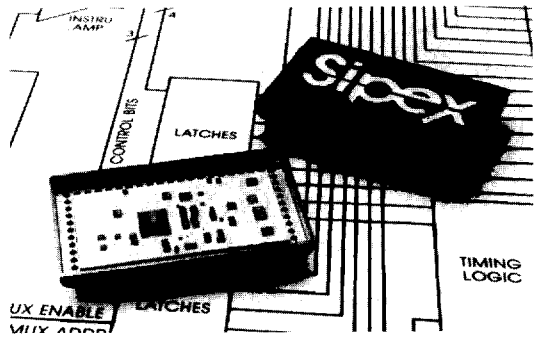
16-BIT
µP CONTROLLED DATA ACQUISITION SYSTEM

FEATURES

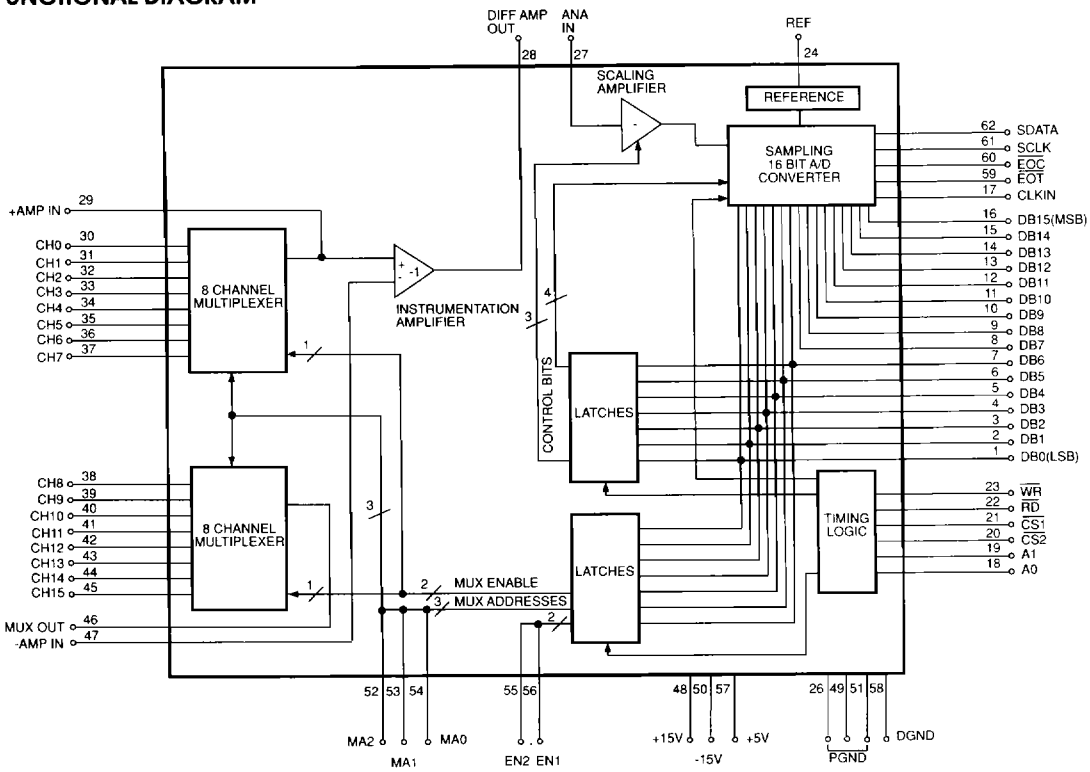
- Integral Linearity - 0.001% FSR
- Differential Linearity - 0.003% FSR
- High CMRR - 80 dB min.
- High Throughput - 50 kHz



DESCRIPTION

The SP9488 provides complete 16-bit data acquisition functionality in a single 62 pin package. It includes user selected 8 differential or 16 single-ended input channel multiplexing, an instrumentation amplifier with gain of 1 and a self calibrating 16-bit sampling A/D converter. Different modes and ranges (bipolar 20V, 10V and 5V; unipolar 10V, 5V and 2.5V) are digitally selectable. The SP9488 is suited for intelligent (microprocessor based) applications. A "shared" 16-bit data bus reads the result of a conversion or the status word of the A/D, writes control bits to the A/D and selects a new input signal. The SP9488 is offered in a 62 pin hermetically sealed package. Temperature ranges available are 0 to 70°C for commercial versions and -55 to +125°C with MIL-STD-883 Rev C screening for military grades.

FUNCTIONAL DIAGRAM



(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	SP9488C	SP9488B
ANALOG INPUTS		
Number of channels	User selectable 16 SE or 8 DI	*
Input Voltage Range[1]		
Unipolar	0 to +2.5V, 0 to +5V, 0 to +10V	*
Bipolar	-10V to +10V, -5V to +5V, -2.5V to +2.5V	*
Common Mode Voltage	±11V min	*
CMRR (1kHz, 20 Vp-p)[8]	80 dB min	*
Multiplexer Crosstalk[8]	80 dB typ	*
Inputs Bias Current[8]	50 nA max	*
Input Offest Voltage[8]	20 nA max	*
Input Impedance	1 mV max	*
Full Power Bandwidth	11 GOhm	*
	25 kHz	*
DIGITAL INPUTS		
High Level Input Voltage	2.0V min	*
Low Level Input Voltage	0.8V max	*
Input Current[8]	10 µA max	*
DIGITAL OUTPUTS		
High Level Output Voltage	3.75V min	*
Low Level Output Voltage	0.4V max	*
Tri-State Leakage Current[8]	±10 µA max	*
Digital Output Pin Capacitance	9 pF typ	*
Output Coding		
Unipolar	Straight Binary	*
Bipolar	Offset Binary	*
Output Drive	8 LSTTL Loads	*
SWITCHING CHARACTERISTICS Refer to the "THEORY OF OPERATION" section for details.		
STATIC PERFORMANCE		
Integral Linearity Error[2]	±0.001% of FSR typ, ±0.002% of FSR max	*
Differential Linearity Error	±0.003% of FSR max	*
Gain Error[3]	±0.03% typ, ±0.1% max	*
Unipolar Offset Error[3]	±0.02% of FSR typ, ±0.05% max	*
Bipolar Offset Error[3]	±0.03% of FSR max, ±0.1% max	*
Noise	0.9 LSB 16 bit RMS typ	*
CONVERSION and THROUGHPUT		
Throughput[4,8]	50 kHz max	*
A/D Conversion Time[5]	16 µs typ	*
S/H Acquisition Time[5]	3 µs typ	*
Front End Acquisition Time[6]	15 µs typ	*
DRIFT CHARACTERISTICS		
Integral Linearity Error (t_{MIN}-t_{MAX})	±0.003% of FSR max	*
Differential Linearity (t_{MIN}-t_{MAX})	No Missing Codes 15-Bits	*
Gain	±15 ppm/°C max	*
Unipolar Offset	±5 ppm of FSR/°C max	*
Bipolar Offset	±10 ppm of FSR/°C max	*
POWER REQUIREMENTS[7]		
Current Drains		
+15V	60mA max	*
-15V	50mA max	*
+5V	10mA max	*
Power Consumption	1.7W max	*
PSRR (All Supplies, Any Range and Mode)	0.001% of FSR/% of Vsupply typ	*
TEMPERATURE RANGE		
Operating	0°C to 70°C	-55°C to +125°C
Storage	-65°C to +150°C	*

*Same as SP9488C

NOTES

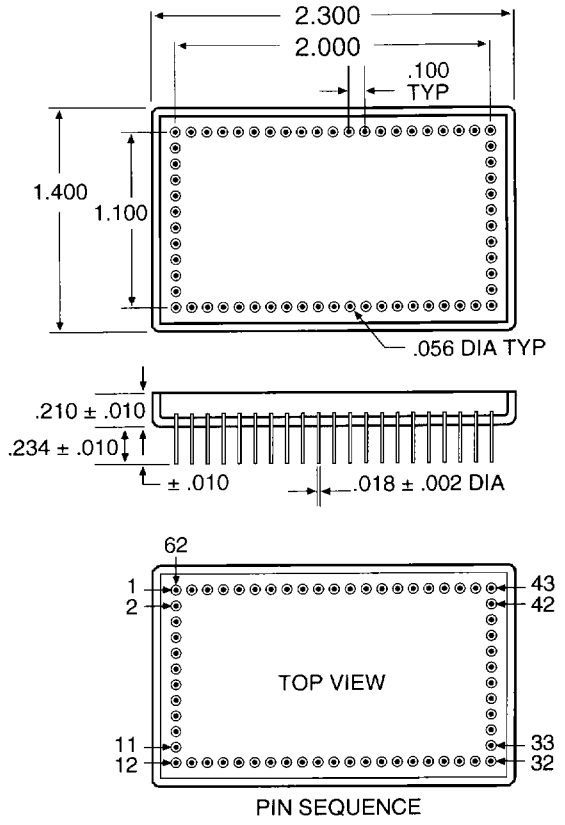
1. Digitally selectable by the user.
2. End point definition.
3. Specification valid for any selectable ranges. Assumption is made that Pins 27 and 28 are tied together.
4. Throughput specified when the pipeline technique is used to acquire the new input signal. A 4 MHz external clock and synchronous sampling are assumed to be used.
5. A 4 MHz external clock and synchronous sampling are assumed to be used. The conversion time is defined as the time between the falling edge on $\overline{WR}$ and the falling edge on $\overline{EOC}$.
6. Includes the settling time of the multiplexers, instrumentation amplifier and scaling amplifier.
7. The +5V supply should not be applied before the ±15V supply. Otherwise, latch up condition may occur.
8. Guaranteed but not tested

PIN ASSIGNMENTS

PIN #	FUNCTION
1	DB0 (LSB)
2	DB1
3	DB2
4	DB3
5	DB4
6	DB5
7	DB6
8	DB7
9	DB8
10	DB9
11	DB10
12	DB11
13	DB12
14	DB13
15	DB14
16	DB15 (MSB)
17	CLK IN
18	A0
19	A1
20	$\overline{CS2}$
21	$\overline{CS1}$
22	$\overline{RD}$
23	$\overline{WR}$
24	REF
25	Reserved
26	PGND-2
27	ANA IN
28	DIFFAMP OUT
29	+AMP IN
30	CH0
31	CH1
32	CH2
33	CH3
34	CH4
35	CH5
36	CH6
37	CH7
38	CH8
39	CH9
40	CH10
41	CH11
42	CH12
43	CH13
44	CH14
45	CH15
46	MUX OUT
47	-AMP IN
48	+15V
49	PGND-1
50	-15V
51	PGND-3
52	MA2
53	MA1
54	MA0
55	EN2
56	EN1
57	+5V
58	DGND
59	$\overline{EOT}$
60	$\overline{EOC}$
61	SCLK
62	SDATA

PACKAGE OUTLINE

(DIMENSIONS IN INCHES (mm))



GEN TOL ± .005

ABSOLUTE MAXIMUM RATINGS

+15V to PGND
(Positive Analog Supply) ..... +18V

-15V to PGND
(Negative Analog Supply) ..... -18V

+5V to DGND (Digital Supply) 5.8V

Analog Input Voltage ..... Analog Supplies +20V

Digital Input Voltage ..... Digital Supply

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SCREENING
SP9488C	0°C to 70°C	—
SP9488B	-55°C to +125°C	MIL-STD-883C

PIN DESCRIPTION

The description given in this paragraph is not exhaustive: a more complete explanation of how to use the different pins is done in the "THEORY OF OPERATION" chapter.

A. Power Pins:

- +15V (pin 48): positive analog power supply. Nominally +15V.
- -15V (pin 50): negative analog power supply. Nominally -15V.
- PGND (pins 26, 49 and 51): analog ground reference. These three pins must be tied together close to the package.
- +5V (pin 57): positive digital supply. Nominally +5V.
- DGND (pin 58): digital ground reference.

B. Analog Pins:

1. Inputs:

- CH0 to CH15 (pins 30 to 45): analog inputs channels of the SP9488. They can be used individually as single-ended channels or in pair as differential inputs.
- +AMP IN and -AMP IN (pins 29 and 47): non-inverting and inverting inputs of the instrumentation amplifier. These pins used with MUX OUT (pin 46) permit the choice between single-ended and differential configuration for the input multiplexers of the SP9488.
- ANA IN (pin 27): A/D input of the SP9488. This signal generally comes from the DIFFAMP OUT pin (pin 28) and can be either a bipolar 20V, 10V or 5V, or a unipolar 10V, 5V or 2.5V following the mode and range selected digitally.

2. Outputs:

- MUX OUT (pin 46): output of one of the multiplexers of the SP9488. Used with +AMP IN and -AMP IN (pins 29 and 47), this pin permits the choice between single-ended and differential configuration for the input multiplexers of the SP9488.
- DIFFAMP OUT (pin 28): output of the instrumentation amplifier. This pin is generally tied to ANA IN (pin 27), unless a filter, a PGA, etc., is used between the output of the instrumentation amplifier and the A/D input.
- REF (pin 24): output of the internal reference of the sampling A/D (4.5V). A 0.47µF tantalum capacitor must be tied to this pin. This output can not be used for other purposes without being buffered.
- Pin 25: this pin is reserved for factory use. It must be left open for the correct operation of the SP9488.

C. Digital Pins:

1. Inputs:

- CLKIN (pin 17): all conversions and calibrations are timed from a master clock which can be either supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND (pin 58).
- A0, A1, $\overline{CS2}$, $\overline{CS1}$, $\overline{RD}$, $\overline{WR}$ (pins 18 to 23): control inputs for the proper management of the Data Bus (pins 1 to 16) of the SP9488.

2. Outputs:

- DB0 to DB15 (pins 1 to 16): bidirectional Data Bus. It can carry FROM the SP9488 the result of a conversion or a status word of the A/D. It can carry TO the SP9488 control bits to the A/D or a new input channel address. The bus is controlled by the input pins 18 to 23.
- SCLK (pin 61): serial clock. Used to synchronize the serial result of an A/D conversion coming from the SDATA pin (pin 62).
- SDATA (pin 62): serial output data. The result of an A/D conversion is presented bit by bit after each bit is determined by the successive approximation algorithm. Valid on the rising edge of SCLK (pin 61), data appears MSB first, LSB last.
- $\overline{EOC}$ (pin 60): this output indicates the end of a conversion or calibration cycle of the A/D. It is high during conversion and will fall to a low state upon completion of the conversion cycle indicating the data is valid at the output. Returns high on the first subsequent read or the start of a new conversion.
- $\overline{EOT}$ (pin 59): if low, it indicates that enough time has elapsed since the last conversion for the A/D to acquire the analog input signal.
- MA2, MA1, MA0, EN2 and EN1 (pins 52 to 56): multiplexer addresses pins. They are used for addressing external multiplexers when more than 16 single-ended or 8 differential input channels are desired.

THEORY OF OPERATION

The SP9488 includes complex circuitry. The description of its operation will be gradual, starting at a system level to finish with a detailed explanation, including timing informations.

A. System Description:

The SP9488 can be seen as a two part system:

- The "Signal Conditioning" section, including the multiplexers and the instrumentation amplifier.
- The "Converting" section, including the sampling A/D (plus an input amplifier).

The Data Bus (pins 1 to 16) is shared by both sections. The "Signal Conditioning" section uses it to get new channel addresses and the "Converting" section uses it to get control bits (like selection of the mode and range) or to give the external world the result of a conversion or a status report. The management of the bus between these two sections is insured by the control lines A0, A1, $\overline{CS2}$, $\overline{CS1}$, $\overline{RD}$ and $\overline{WR}$ (pins 18 to 23).

Table 1 gives a summary of the SP9488 functions, versus the logic levels on the control lines:

$\overline{CS1}$	$\overline{CS2}$	A0	A1	$\overline{WR}$	$\overline{RD}$	FUNCTION
1	1	X	X	X	X	No operation (Data Bus in tri-state)
1	0	X	X	↓	1	The external world selects a new input channel
0	1	X	1	↓	1	The external world writes control bits to the A/D
0	1	1	0	↓	1	The A/D starts a conversion
0	1	1	0	X	0	The external world reads the result of a conversion
0	1	0	0	1	0	The external world reads the status register of the A/D

Note: X means "do not care" (but do not leave pin open).
↓ means that the event occurs on a high to low transition.

Table 1. SP9488 Functions

B. "Signal Conditioning" Section Description:

1. Single-Ended or Differential Input Configuration:

The SP9488 contains two 8 single-ended channels multiplexers which can be configured in 1 16 single-ended channels or 8 differential channels multiplexer following the user's choice. Table 2 shows the connections to obtain one or the other input configuration.

2. Addressing the Multiplexers:

As mentioned earlier the multiplexer addressing is done through the shared Data Bus: the 7 LSB's (DB0 to DB6) are used to carry a new input channel address. Table 1 indicates that $\overline{CS1}$ and $\overline{RD}$ must be high and $\overline{CS2}$ low (the logic levels on A0 and A1 do not care) to select a new input channel. A high to low transition on the $\overline{WR}$ control line makes the new channel selection. Table 3 lists the selected channel as a function of the code on the Data Bus.

In Table 3, the value on DB5 and DB6 does not care. These two addresses are important only when a channel input expansion is desired.

Single-Ended Input Configuration:

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNEL
X	X	0	1	0	0	0	CH0
X	X	0	1	0	0	1	CH1
X	X	0	1	0	1	0	CH2
X	X	0	1	0	1	1	CH3
X	X	0	1	1	0	0	CH4
X	X	0	1	1	0	1	CH5
X	X	0	1	1	1	0	CH6
X	X	0	1	1	1	1	CH7
X	X	1	0	0	0	0	CH8
X	X	1	0	0	0	1	CH9
X	X	1	0	0	1	0	CH10
X	X	1	0	0	1	1	CH11
X	X	1	0	1	0	0	CH12
X	X	1	0	1	0	1	CH13
X	X	1	0	1	1	0	CH14
X	X	1	0	1	1	1	CH15

Differential Input Configuration:

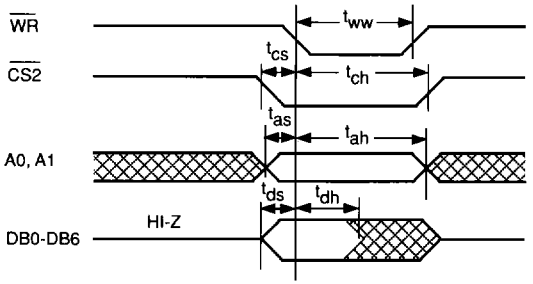
DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED DIFFERENTIAL CHANNELS
X	X	1	1	0	0	0	CH0/CH8
X	X	1	1	0	0	1	CH1/CH9
X	X	1	1	0	1	0	CH2/CH10
X	X	1	1	0	1	1	CH3/CH11
X	X	1	1	1	0	0	CH4/CH12
X	X	1	1	1	0	1	CH5/CH13
X	X	1	1	1	1	0	CH6/CH14
X	X	1	1	1	1	1	CH7/CH15

Table 3. Multiplexer Addressing in the SP9488

INPUT CONFIGURATION	CONNECT PIN 46 (MUX OUT) TO	CONNECT PIN 47 (-AMP IN) TO	CONNECT PIN 29 (+AMP IN) TO
16 Single-Ended Channels	Pin 29 (+AMP IN)	Pin 49 (PGND1)	Pin 46 (MUX OUT)
8 Differential Channels	Pin 47 (-AMP IN)	Pin 46 (MUX OUT)	Left Open

Table 2. Multiplexers Configuration for the SP9488

Figure 1 shows the Data Bus timing when used to address the multiplexers.



Note: $\overline{CS1}$ is high

-t_{ds} = t_{cs} = t_{as} = data and address set-up times = 20 ns min.
-t_{dh} = data hold time = 5 ns min.
-t_{ch} = t_{ah} address hold time = 40 ns min.
-t_{ww} = write width pulse = 40 ns min.
Timing guaranteed but not tested

FIGURE 1
DATA BUS TIMING (MULTIPLEXER ADDRESSING)

3. Input Channel Expansion:

The SP9488 can be extended to 24 or 32 single-ended, or 16 differential input channels without the addition of any component. Figure 2a shows how to connect two external 8 channels single-ended multiplexers to get a 32 channels single-ended input system. Table 4a shows the associated addresses.

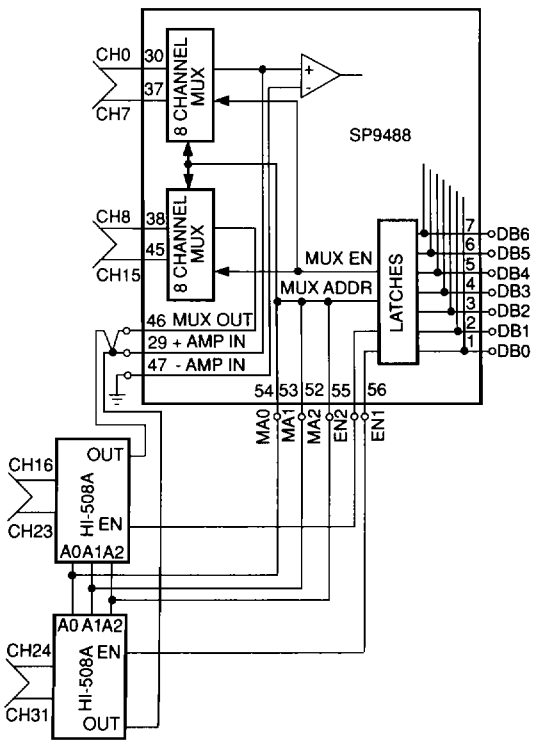


FIGURE 2a
INPUT EXPANSION OF THE SP9488
(32 SINGLE-ENDED CHANNELS)

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNELS
0	0	0	1	•	•	•	CH0 to CH7
0	0	1	0	•	•	•	CH8 to CH15
0	1	0	0	•	•	•	CH16 to CH23
1	0	0	0	•	•	•	CH24 to CH31

Table 4a. Addresses for the Input Expansion of the SP9488 (32 Single-Ended Channels)

Figure 2b shows how to connect one external 16 channel single-ended multiplexer to get the same 32 single-ended expansion and table 4b indicates the associated addresses.

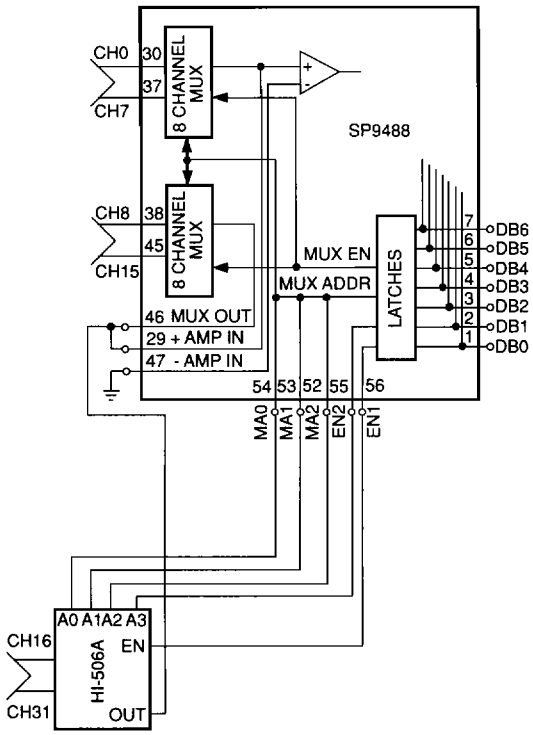


FIGURE 2b
INPUT EXPANSION OF THE SP9488
(32 SINGLE-ENDED CHANNELS)

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNELS
0	0	0	1	•	•	•	CH0 to CH7
0	0	1	0	•	•	•	CH8 to CH15
1	•	0	0	•	•	•	CH16 to CH31

Table 4b. Addresses for the Input Expansion of the SP9488 (32 Single-Ended Channels)

Figure 2c shows how to connect 2 external 8 single-ended multiplexers to get a 16 differential input channels system. Table 4c indicates the associated addresses.

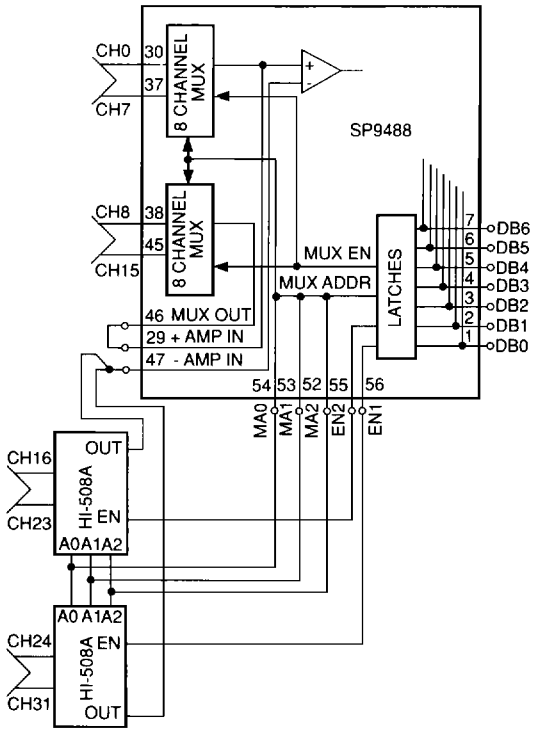


FIGURE 2c
INPUT EXPANSION OF THE SP9488
(16 DIFFERENTIAL CHANNELS)

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNELS
0	1	0	1	•	•	•	CH0/CH16 to CH7/CH23
1	0	1	0	•	•	•	CH8/CH24 to CH15/CH31

Table 4c. Addresses for the Input Expansion of the SP9488 (16 Differential Channels)

Note: In Tables 4a, 4b, and 4c, only a range of selected channels is given: the value on DB0, DB1 and DB2 determines one channel.

C. "Converting" Section Description:

1. A/D Description:

The A/D used in the SP9488 is a 16-bit sampling A/D converter using the successive approximation algorithm. It uses a charge redistribution architecture that achieves high accuracy: the linearity, offsets and gains can be calibrated in different ways (see next paragraph). The A/D converter of the SP9488 comes complete with an internal reference. The modes and ranges are digitally programmable. However, the user has to supply a master clock (through the CLKIN pin) with a frequency between 100 kHz and 4 MHz. The relationship between the clock frequency and the conversion time is explained in paragraph 3c. Paragraph 3b explains how to initiate a conversion.

2. Set-up of the A/D Through the Data Bus:

As mentioned earlier, the mode and range of the A/D and the calibration modes are selected through the Data Bus. To be able to write control bits to the A/D, Table 1 shows that a high to low transition on the $\overline{WR}$ pin is necessary at the same time as $\overline{CS2}$, A1 and $\overline{RD}$ are high, $\overline{CS1}$ is low (the logic level on A0 does not care). The control bits are brought to the A/D by the DB0 to DB6 line (the same as the ones which carry the multiplexers addresses):

- DB3, DB4, DB5, DB6 carry the mode and range selection bits. Table 5 shows a truth table for these bits.

DB3	DB4	DB5	DB6	MODE AND RANGE SELECTED
1	0	1	1	Bipolar 20V
1	1	0	1	Bipolar 10V
1	1	1	0	Bipolar 5V
0	0	1	1	Unipolar 10V
0	1	0	1	Unipolar 5V
0	1	1	0	Unipolar 2.5V
X	0	0	0	Forbidden

Table 5. A/D Mode and Range Selection Bits

- DB1 sets the format of the conversion result (16-bit output code). When high, the output code can be read in one shot (16-bits); if low it can be read in two bytes available on pins DB0 to DB7, the eight most significant bits first.
- DB0 and DB2 are calibration bits. These two bits allow the user to choose between two different calibration procedures:

1. DB2: When this bit is brought high, all the internal logic of the A/D clears. When it returns low a full calibration begins, which takes 1,443,840 master clock cycles (360 ms with a 4 MHz clock) to complete. The same reset cycle can be obtained by performing a write operation with A0, $\overline{CS1}$, A1, low; $\overline{CS2}$ and $\overline{RD}$ high. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon completion. This mode of calibration is performed after a power-up or after the operating temperature of the SP9488 has changed.

2. DB0: When this bit is low, a calibration, termed "interleave" is initiated. Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. A calibration cycle is performed after 72,192 conversions. Practically this type of calibration extends the conversion time by 20 master clock periods. Other than reduced throughput, interleave is totally transparent to the user.

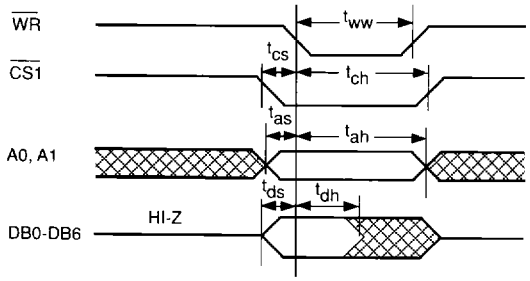
Table 6 summarizes the functions of DB0, and DB2 when used as control bits for the A/D of the SP9488.

DB0	DB2	FUNCTIONS
X	1	Full Reset Calibration
0	0	Initiate Interleave Calibration
1	0	Terminate Interleave Calibration

X means "do not care"

Table 6. Calibration Control Bits for the SP9488

The timing for writing control bits to the A/D is given at Figure 3.



Note: $\overline{CS2}$ is high

-t_{ds} = t_{cs} = t_{as} = data and address set-up times = 20 ns min.
-t_{dh} = data hold time = 5 ns min.
-t_{ch} = t_{ah} address hold time = 40 ns min.
-t_{ww} = write width pulse = 40 ns min.
Timing guaranteed but not tested

FIGURE 3
DATA BUS TIMING (WRITING OF CONTROL BITS TO A/D)

Generally before starting a conversion, a set of bits must be written to the A/D in order to be sure that the conversion will be properly performed and to take advantage of the high accuracy of the SP9488. A calibration must be performed after the system is powered up.

3. Detailed Timing of the A/D:

a. Master Clock

The A/D of the SP9488 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the SP9488 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal. All calibration, conversion and throughput times directly scale to the master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the A/D's internal oscillator will vary from unit to unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The SP9488 is specified for accurate operation with an external clock up to 4 MHz; its internal is specified at a minimum of 2 MHz.

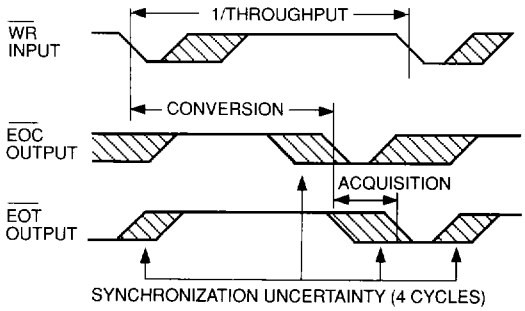
b. Initiation of Conversion

Table 1 indicates that a falling transition on the $\overline{WR}$ input with $\overline{CS1}$, A1 low and $\overline{CS2}$, A0, $\overline{RD}$ high will initiate a conversion. Under microprocessor control, it means that a "write" instruction to the base address of the SP9488's A/D (determined by $\overline{CS1}$, $\overline{CS2}$, A0 and A1) will initiate a conversion. A falling edge on the $\overline{WR}$ input puts the A/D sample-hold in the hold mode. The $\overline{WR}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50 ns. Upon completion of the conversion cycle, the sample-hold automatically returns to the track mode.

c. Conversion Time/System Throughput

Upon completion of a conversion cycle and returning to the track mode, the SP9488's A/D requires time to acquire the analog signal before another conversion can be initiated. The acquisition of the A/D is specified as six master clock cycles plus 2.25 µs. This adds to the conversion time to define the A/D and the SP9488's maximum throughput. The conversion time of the A/D, in turn, depends on the sampling, calibration and master clock conditions. There are basically two different sampling modes: the asynchronous and synchronous modes. Figure 4 shows their timing respectively, while Table 7 shows the conversion times and throughput rates associated with these two modes.

ASYNCHRONOUS SAMPLING



SYNCHRONOUS SAMPLING

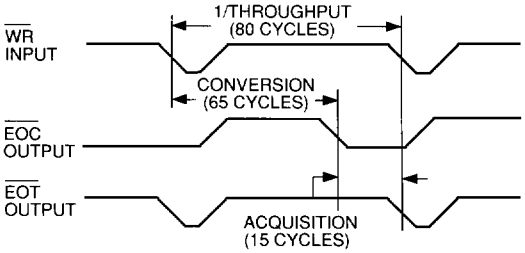


FIGURE 4
ASYNCHRONOUS AND SYNCHRONOUS SAMPLING OF SP9488'S (A/D)

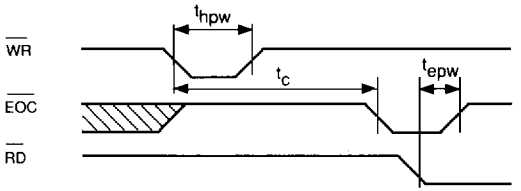
SAMPLING MODE	CONVERSION TIME	THROUGHPUT TIME
Asynchronous	65T min.	
	69T+235 ns max.	75T+2.25 µs max.
Synchronous	65T	80T

T=one master clock cycle

Table 7. Conversion and Throughput Times

The 4 cycles uncertainty that can be seen in the asynchronous mode are due to the fact that the sampling clock (on the $\overline{WR}$ pin) and the master clock are not synchronous. The maximum throughput is obtained by tying the $\overline{EOT}$ output to the $\overline{WR}$ input. In this case the master clock and the sampling clock are synchronous and the maximum throughput (50 kHz with a 4 MHz master clock) is achievable.

$\overline{EOC}$ is high during conversion. It will fall at the end of the conversion and will return high within four master clock cycles from the start of a read data operation or a conversion cycle. Figure 5 shows the conversion timing.



t_{hpw} = $\overline{WR}$ pulse width = $1/f_{CLK}$ + 50 ns min.; t_c max.
t_c = conversion time
t_{epw} = $\overline{EOC}$ pulse width = $4/f_{CLK}$ -20 ns.

FIGURE 5
CONVERSION TIMING

So far only the A/D has been taken in account in the evaluation of the throughput rate. In fact the total throughput of the system (SP9488) is not reduced by the presence of the multiplexers and the instrumentation amplifier, because of the pipeline technique for acquiring the analog signal. This technique selects a new channel immediately after the conversion of the former channel has started. So the acquisition of the "Signal Conditioning Section" is done while the conversion of the former channel is performed. Figure 6 illustrates the pipeline technique.

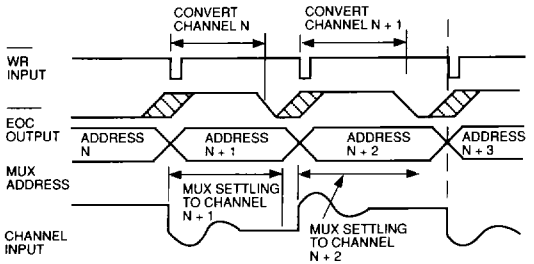
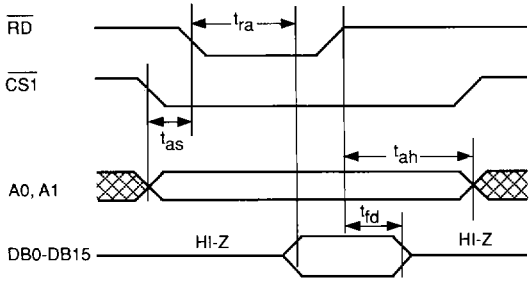


FIGURE 6
PIPELINED MUX INPUT CHANNELS

d. Reading of the Output Code

The result of a conversion can be read by strobing low the $\overline{RD}$ control input with $\overline{CS2}$, A0, high and $\overline{CS1}$, A1 low (the value on $\overline{WR}$ does not care). The data is read in one 16-bit word or two bytes following the control bits written to the A/D. Figure 7 shows a detailed timing of the reading cycle.



t_{as} = address set-up time = 20 ns min.
t_{ah} = address hold time = 50 ns min.
t_{ra} = $\overline{RD}$ low to data valid (access time) = 150 ns max.
t_{fd} = $\overline{RD}$ high to output HI-Z (output float delay) = 140 ns max.

FIGURE 7
DATA BUS TIMING (READING THE OUTPUT DATA OF THE SP9488)

The A/D of the SP9488 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in the SP9488 throughput. Enabling the tri-state outputs while a conversion is in process will not introduce errors. When TTL loads are utilized, the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the Data Bus of the SP9488 is therefore recommended.

e. Reading of the Status Word of the A/D

A status information byte can be read from the SP9488 when $\overline{RD}$ is strobed low while $\overline{CS1}$, A0, A1 are low, $\overline{CS2}$, and $\overline{WR}$ are high (see Table 1). The timing for reading the status byte is the same as reading the result of a conversion (figure 7). Table 8 defines all the status bits and their position on the Data Bus.

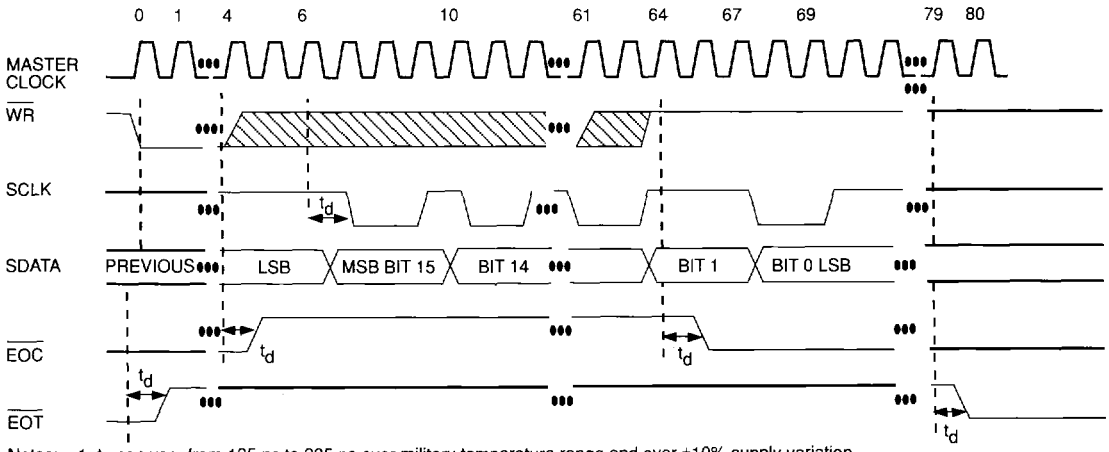
f. Serial Interface

The SP9488 presents also the result of a conversion serially (MSB first). It is available on the SDATA pin (pin 62) and to ease the interface with the external world, a serial clock, SCLK (pin 61) is provided. Figure 8 shows the general timing for the serial output.

11

PIN	STATUS	DEFINITION
DB0	$\overline{\text{End of conversion}}$	Falls upon completion of a conversion and returns high on the first subsequent read
DB1	Reserved	Reserved for factory use
DB2	Low byte/$\overline{\text{high byte}}$	When data is to be read in an 8 bit format, indicates which byte will appear at the output next
DB3	$\overline{\text{End of track}}$	When low, indicates the input has been acquired to the A/D accuracy
DB4	Reserved	Reserved for factory use
DB5	Tracking	High when the A/D is tracking the input
DB6	Converting	High when the A/D is converting a held input
DB7	Calibrating	High when the A/D is in a calibration cycle

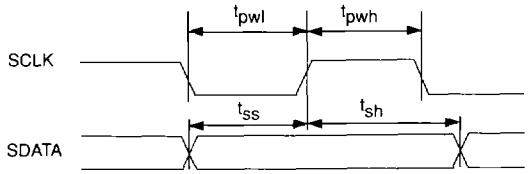
Table 8. Status Bit Definition



Notes: 1. t_d can vary from 135 ns to 235 ns over military temperature range and over ±10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{\text{EOC}}$, $\overline{\text{EOT}}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SCLK, SDATA, $\overline{\text{EOC}}$, and $\overline{\text{EOT}}$ is fixed.

FIGURE 8
SERIAL OUTPUT TIMING

Figure 8 shows that, just subsequent to each bit decision the serial clock (SCLK) will fall and return high once the bit information on SDATA has stabilized. Hence the rising edge of the SCLK output should be used to clock the data out of the SP9488. It can be seen too that the first bit of information is available after 8 master clock cycles (from the falling edge of $\overline{\text{WR}}$). Figure 9 specifies the timing for the SCLK and SDATA pin.



t_{pwl} = pulse width low = $2/f_{CLK}$ ns
t_{pwh} = pulse width high = $2/f_{CLK}$ ns
t_{ss} = SDATA to SCLK rising = $2/f_{CLK}$ -100 ns min.
t_{sh} = SCLK rising to SDATA = $2/f_{CLK}$ -100 ns min.
Timing guaranteed but not tested

FIGURE 9
TIMING FOR THE SCLK AND SDATA OUTPUT PINS

APPLICATION INFORMATION

A. Power Supply and Grounding Considerations, Layout Precautions:

Power supplies for the SP9488 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power supplies. It is important to remember that 310 µv is 1LSB15 bit for a 10 volt range. Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable capacitors are 10 µF tantalum types in parallel with 0.1 µF disc ceramic types.

To ensure maximum accuracy, the SP9488 has three different analog grounds separated from the digital ground, which must be routed properly to prevent DC and transient errors. DC errors can be caused by current flowing through a run resistance between the system ground reference (1 mA through 0.3 Ohm can cause 1LSB15 bit of error for a 10 volts range). The best way to prevent this type of error is to connect the digital and analog grounds very close to the SP9488 and use this point as the system ground. This can be done as a so-called "star-ground" as shown in Figure 10. The single common ground reference ensures no ground current or ground loop errors.

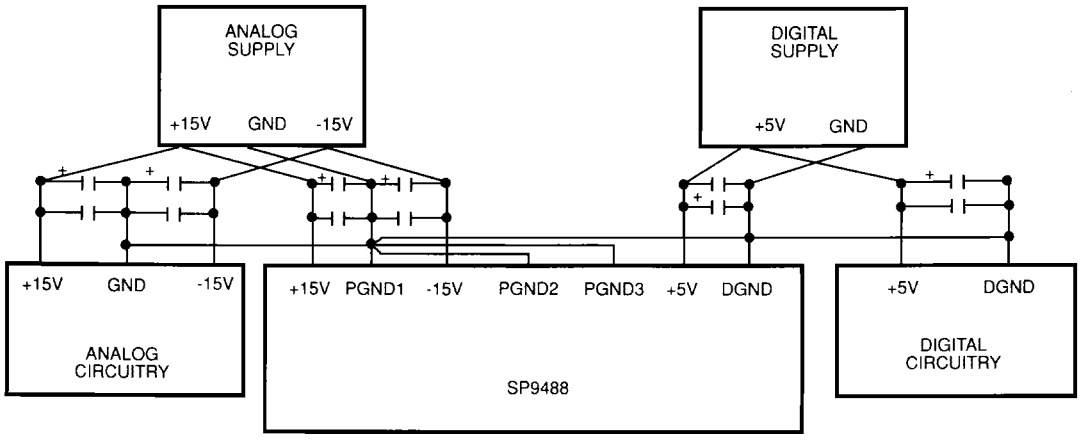


FIGURE 10
GROUNDING THE SP9488

The SP9488 has been laid out so that all the analog pins (24 to 51) and the digital pins (52 to 62 and 1 to 23) are together. This can simplify the design of a printed circuit board layout and make easier the separation of analog and digital signals. Figure 11 shows a suggested layout of the SP9488 and other circuitry.

B. Reference Capacitor:

As mentioned in the "pin description" paragraph, a 0.47 µF tantalum capacitor must be provided by the user at pin 24 (REF). This pin is the output of the 4.5V voltage reference used by the A/D of the SP9488. It can not be used for other purposes without being buffered.

C. Utilization of the SP9488 Under Static or Dynamic Input Signals:

The SP9488 has been designed to give the user the liberty of tailoring the "Signal Conditioning" section following his application. More precisely, there is no filtering element in the "Signal Conditioning" section, limiting the bandwidth of the input amplifiers; this gives maximum performance (fast settling time) when DC input signals are digitized. When wideband AC signals are digitized however, no filtering means that wideband noise is presented to the input of the A/D of the SP9488. Such noise is sampled at 50 kHz, and aliased back into the DC to 25 kHz band. The Signal-to-Noise measurement of the system can then be affected seriously. In this type of application, it is recommended that the user provides a filter between Pin 28 (DIFFAMPOUT) and Pin 27 (ANAIN) to limit the bandwidth of the input signal. A filter may even be needed for each input channel, depending on the application. Figure 12 shows the frequency response of the analog front end of the SP9488 when no filtering is processed (Pins 27 and 28 tied together).

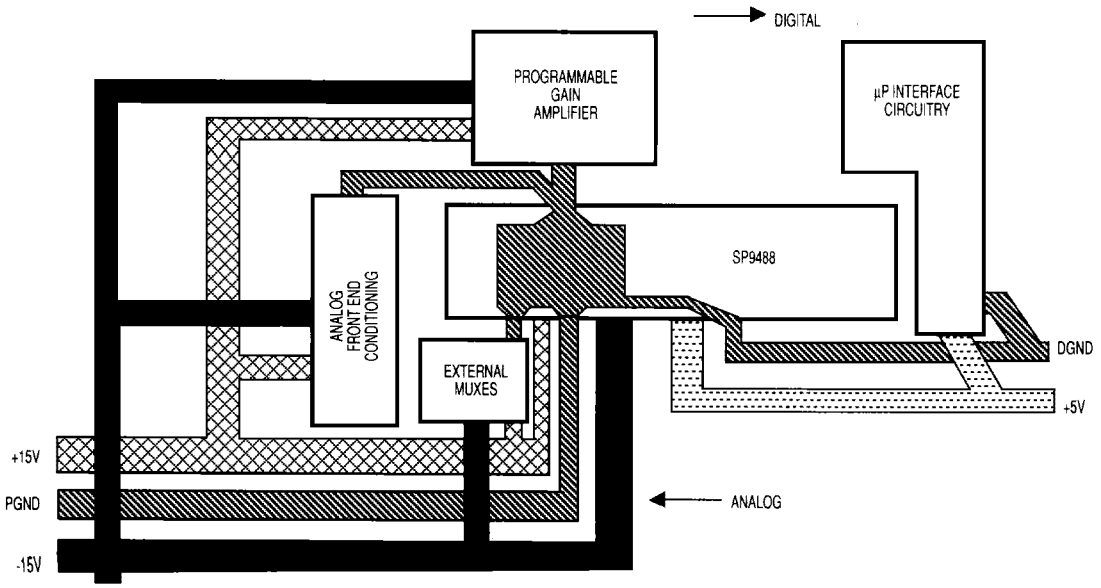


FIGURE 11
PCB LAYOUT FOR THE SP9488

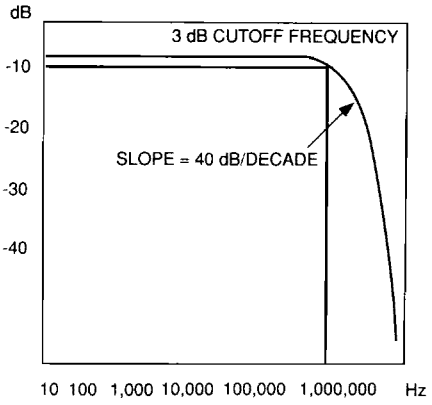


FIGURE 12
FREQUENCY RESPONSE OF THE SP9488
ANALOG FRONT END

D. General Interface of the SP9488 to a Microprocessor:

The interface of the SP9488 to a microprocessor involves several questions. First, write instructions must be executed by the processor to select new input channels, control the A/D or start a conversion. Read instructions have to be performed to inform the µP on the SP9488 status or receive the result of a conversion. When a conversion has been started, the processor has to wait for its end before reading valid conversion results. The SP9488 provides an output signal EOC which indicates when a conversion is in progress. This signal can be polled by reading it through an external tri-state buffer. The EOC can also generate an interrupt upon completion of conversion, if the processor has other tasks to perform (for instance selecting a new input channel). Another possible time-out method is to insert a sufficient number of "do-nothing" instructions to ensure that enough processor time has elapsed before reading the conversion result. Once established that the conversion is finished, the processor can get the result. For the SP9488 it can be read immediately by 8 or 16 bits µP, thanks to the user selected output format (two bytes or one 16 bit word).

The following paragraphs show the SP9488 interface to different families of microprocessors. For clarity, no linear hardware has been shown.

1. Intel:

The interface of the SP9488 to any INTEL processor is basically the same. It is the simplest too because INTEL processors have $\overline{RD}$ and $\overline{WR}$ output signals directly compatible with the $\overline{RD}$ and $\overline{WR}$ input signals of the SP9488. Figure 13 shows the interface to a 8088 µP. Writing data to the SP9488 consists in <MOV addr, AX> where AX is the register containing the data to be loaded, and addr the decoded address of the SP9488. The read instructions are <MOV AX, addr> type instructions.

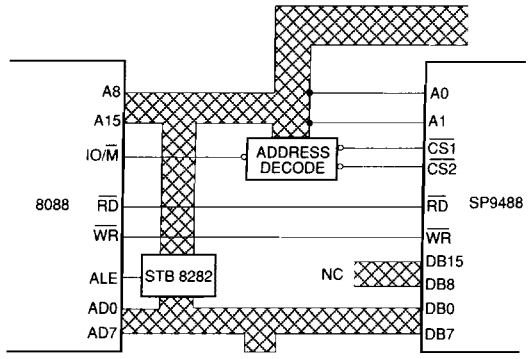


FIGURE 13
INTERFACE OF THE SP9488 TO AN INTEL µP

2. Motorola 8-Bit Non-Multiplexed Format (6800, 6500 Series):

Figure 14 shows this interface. Writing data to the SP9488 consists of <STAA,addr> instructions, where A is the accumulator (register) containing the data to be loaded and addr is the decoded address of the SP9488. The conversion result or the status word of the A/D is read by <LDAA,addr> type instructions: the data is then transferred from the SP9488 to the processor's accumulator.

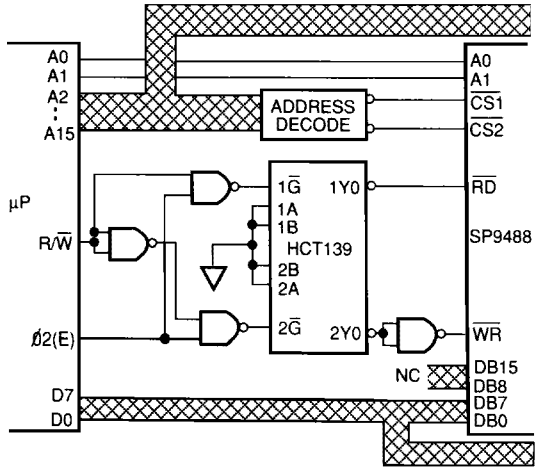


FIGURE 14
INTERFACE OF THE SP9488 TO A 6800 TYPE µP

3. Motorola 8-Bit Multiplexed Format (6801, 146805 Series):

The interface is very similar to the non-multiplexed format. Same type of instructions can be used to execute data transfers between the processor and the SP9488. Figure 15 shows how to demultiplex the data/address bus when the processor is used in expanded multiplexed mode. The rest of the interface is the same as Figure 14.

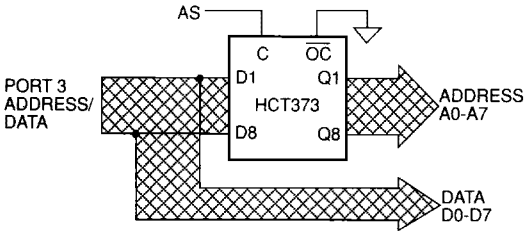


FIGURE 15
DEMULTIPLEXING THE ADDRESS/DATA BUS
OF A 6801 µP TYPE

4. Motorola 16-Bit Multiplexed Asynchronous Format (68000 Series):

A typical interface to the 68000 is shown in Figure 16. The extra logic gates are necessary to generate the $\overline{DTACK}$ signal of the 68000 when it writes to the SP9488 or reads the status word of the SP9488. If the processor tries to read the result of a conversion while the SP9488 is still converting, the read cycle will be stretched out over the entire conversion time by taking the $\overline{EOC}$ output of the SP9488 back into the $\overline{DTACK}$ input of the 68000. Writing data to the SP9488 consists of a <MOV.B Dn,addr> where Dn is the data register which contains the data to be loaded to the SP9488 and addr is the decoded address. Data is read from the SP9488 using a <MOV.B addr,Dn> instruction with the result of a conversion or a status report placed in the register Dn.

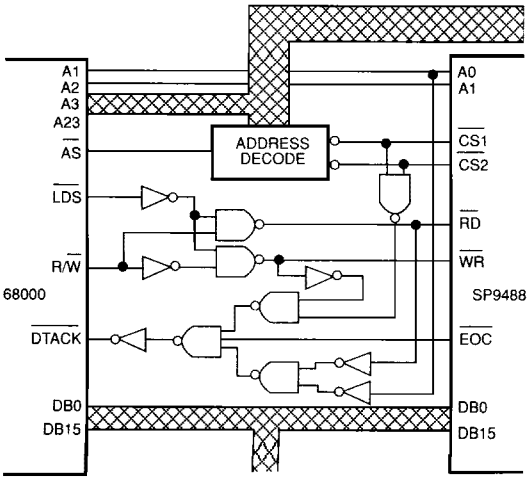


FIGURE 16
INTERFACE OF THE SP9488 TO A 68000 TYPE µP

E. Autocalibrated System:

The A/D of the SP9488 is self-calibrating: it means that when the opportunity is given to the device to perform a calibration, offset and gain errors due to it are negligible. Most of the offset and gain errors of the SP9488 are due to the front-end circuitry. These errors are actively trimmed at the factory to reduce them to a minimum. However, if the user desires it, there is an elegant way to reduce these errors to zero: the system autocalibration. Figure 17 shows a block diagram of the hardware configuration.

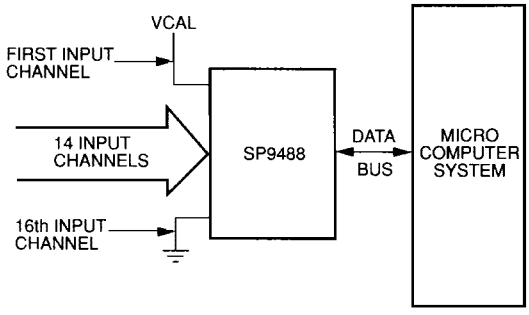


FIGURE 17
HARDWARE CONFIGURATION OF AN AUTOCALIBRATED
SYSTEM USING THE SP9488

The different steps for correcting offsets and gain errors are as follows:

1. Measure of ground (GND): it gives the offset system error.
2. Measure of a known voltage (VCAL): the following formula gives the system gain error (GE):

   GE = (ACVCAL - ACGND) / ICVCAL

   Where ACVCAL is the actual code measured for VCAL, ACGND is the actual code measured for GND, and ICVCAL is the ideal code for VCAL.
3. Storage of these numbers to correct future readings. The following formula gives the corrected code for any reading (CC):

   CC = (AC - ACGND) * GE

   Where AC is the actual code measured.

To apply this adjustment procedure, a stable and accurate VCAL is required.

SP9488 PERFORMANCE

A. Integral Linearity

Integral linearity is defined as the deviation of the transfer function from an ideal straight line through zero and full scale (End Point definition). Thanks to a unique calibration algorithm in SP9488's A/D and a fine design of the analog front end the integral linearity errors are kept below 0.001% of full scale typically.

Table 9 shows the integral linearity errors of a typical unit measured at the center code on both sides of each major 15 bit transition (bipolar 5V mode).

CODE-1 (OCTAL)	I.L. ERR (%)	CODE (OCTAL)	I.L. ERR (%)
1	0.0000	1	0.0000
2	-0.0000	2	0.0001
4	-0.0001	3	-0.0001
10	-0.0003	5	-0.0002
20	-0.0003	11	-0.0004
40	-0.0004	21	-0.0001
100	-0.0003	41	-0.0002
200	-0.0002	101	-0.0001
400	-0.0004	201	0.0001
1000	-0.0003	401	-0.0003
2000	-0.0002	1001	0.0001
4000	-0.0001	2001	0.0001
10000	-0.0002	4001	0.0002
20000	-0.0001	10001	0.0002
40000	-0.0009	20001	0.0003
60000	-0.0006	40001	-0.0008
70000	0.0004	60001	-0.0004
74000	-0.0000	70001	0.0007
76000	0.0001	74001	0.0002
77000	0.0003	76001	0.0003
77400	0.0001	77001	0.0006
77600	0.0003	77401	0.0002
77700	0.0004	77601	0.0005
77740	0.0004	77701	0.0006
77760	0.0003	77741	0.0007
77770	0.0003	77761	0.0005
77774	0.0002	77771	0.0002
77776	0.0001	77775	0.0000
		77777	0.0001

Table 9. Integral Linearity Error of a Typical Unit

B. Dynamic Performance:

The integral linearity is specified statically for the SP9488. This type of error under dynamic conditions is generally quantified by a Signal to Noise Ratio (SNR) test. In this test a finite time sequence of sampled data from a spectrally pure sine wave input is computed by the tester into a frequency spectrum using a Fast Fourier Transform algorithm. From this frequency domain representation of the output data, the effect of integral non-linearity may be measured: harmonics of the input sine wave caused by I.L. errors are aliased into the base band spectrum. The magnitude of the fundamental's spectral lines (the signal) is summed, then divided by the sum of the remaining spectral lines (the noise). The logarithm of this number multiplied by 20 provides the SNR expressed in decibels. For an ideal converter, it can be shown that:

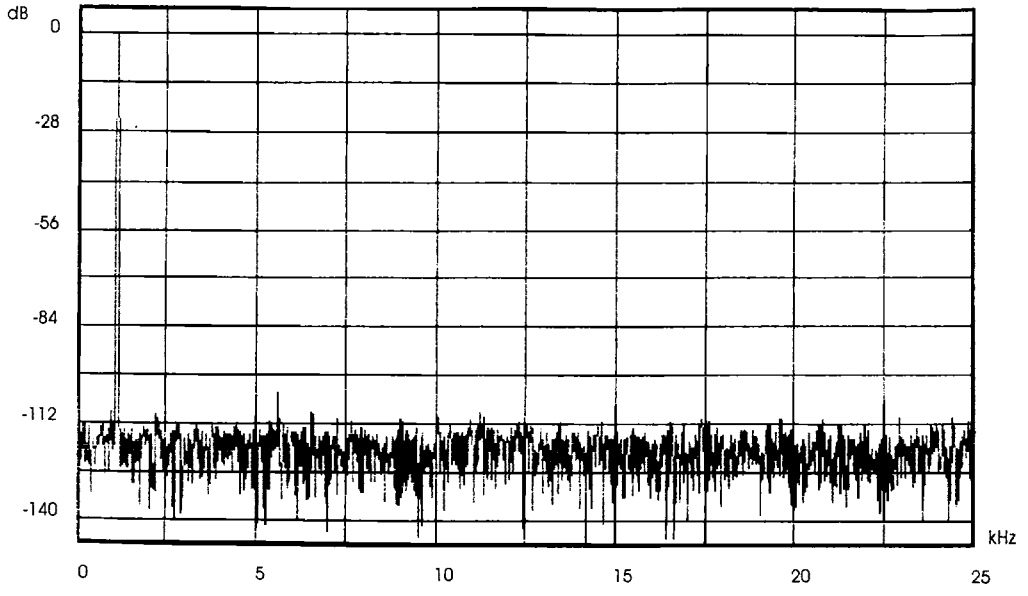
$$SNR = 6.02 \times N + 1.76 \text{ dB}$$

(N = number of bits of the converter)

Graph 1 shows the behavior of the SP9488 with a 1.123 kHz sine wave input: the accuracy is 14 bits.

C. Noise:

The result of each conversion performed by the SP9488 depends on the analog input level on the selected channel and the instantaneous value of noise sources in the data acquisition system. Because the SP9488's output is in digital form, any filtering of its noise must be performed in the digital domain and can be implemented in software with minimal overhead.



Graph 1. FFT of the SP9488, F_{in} = 1.123 kHz, F_{Sample} = 50 kHz

An easy way of measuring the noise of the SP9488 is to plot an histogram of the codes obtained for a given DC input voltage. Figure 18 shows the histogram for the results of 5000 conversions performed by a SP9488 in bipolar 10V mode; the decimal code 49,152 was arbitrarily chosen and the analog input was set close to the code center.

SP9488 NOISE MEASUREMENT AT CODE 49,152

0	49,145
0	49,146
0	49,147
1	49,148
32	49,149
239	49,150
870	49,151
2595	49,152
1028	49,153
209	49,154
24	49,155
2	49,156
0	49,157
0	49,158
0	49,159

FIGURE 18
HISTOGRAM PLOT AT CODE 49,152 FOR THE SP9488

With a noiseless converter, code 49152 would always appear. The histogram shows a bell shape with all codes other than 49152 due to internal noise. From this histogram it is possible to extract the RMS value of the noise: in this case it is 0.9 LSB 16-bit RMS.

Noise in digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the noise over a wider frequency band (leading to a lower noise density in the desired bandwidth), then the averaging applies a low-pass filtering of the noise above the desired signal bandwidth.

In general, the SP9488's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz and digitally filtering to the desired signal bandwidth.

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