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transforming specialty electronics

FAIRCHILD

N-Channel Power Trench Mosfet Chip

FDP150N10A

100V, 50A, 15mΩ[1]

Part	$V_{(BR)DSS}$	I_{Dn}	$R_{DS(on)}$ Max	Die Size
FDP150N10A	100V	50A	15mΩ[1]	3.2 x 1.9 mm[2]
See page 2 for ordering part numbers & supply formats				

Chip Photo TBA

Applications

- High density AC / DC Converters
- Motor drives & Micro Inverters

Features

- High Power & Current Handling Capability
- Low $R_{DS\ (on)}$ per mm^2
- Low Gate Charge, Fast Switching

Maximum Ratings

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current[2]	Continuous (T_C = 25°C)	50	A
		Continuous (T_C = 100°C)	36	
I_{DM}	Drain Current[3]	Pulsed	200	
T_J, T_{STG}	Operation Junction & Storage Temperature		-55 to 175	°C
E_{AS}	Single Pulsed Avalanche Energy[4]	L = 2mH, I_{AS} = 9.2A, R_G=25Ω Starting T_J =25°C	84.6	mJ
dv/dt	Peak Diode Recovery dv/dt[4]	I_{SD}≤100A,di/dt≤200A/µs, V_{DD}≤BV_{DSS} Starting T_J=25°C	6	V/ns

Static Characteristics, T_J = 25° unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250µA, V_{GS} = 0V	100	-	-	V
$V_{GS(th)}$	Gate threshold Voltage	V_{GS} = V_{DS}, I_D =250µA	2.0	-	4.0	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	µA
	Zero Gate Voltage Drain Current @ 150°C	V_{DS} = 80V, V_{GS} = 0V	-	-	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20V , V_{DS} = 0V	-	-	±100	nA
$R_{DS(on)}$	Static Drain to Source On Resistance[1]	V_{GS} = 10V, I_D = 50A	-	12.5	15.0	mΩ

Notes:

1. Defined by chip design, not subject to 100% production test at wafer level
2. Performance will vary based on assembly technique and substrate choice
3. Repetitive Rating: Pulse width limited by maximum junction temperature

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Dynamic Characteristics[4], T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 50A	-	40	-	S
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	1.3	-	Ω
C_{iss}	Input Capacitance	V_{DS} =50V, V_{GS} = 0V f = 1MHz	-	1080	1440	pF
C_{oss}	Output Capacitance		-	267	355	pF
C_{rss}	Reverse Transfer Capacitance		-	11	-	pF
C_{oss}(er)	Energy Related Output Capacitance	V_{DS} =50V, V_{GS} = 0V	-	436	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} =50V, I_D = 50A V_{GS} = 10V[5]	-	16.2	21.0	nC
Q_{gs}	Gate to Source Gate Charge		-	5.3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	2.6	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	3.7	-	nC

Switching Characteristics[4], T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 50A V_{GS} = 10V R_{GEN} = 4.7Ω[5]	-	13	36	ns
t_r	Turn-On Rise Time		-	16	42	ns
$t_{d(off)}$	Turn-Off Delay Time		-	21	52	ns
t_f	Turn-Off Fall Time		-	5	20	ns

Drain-Source Diode Characteristics[4], T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 50A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V,V_{DD} =50V,I_{SD} = 50A dI_F/dt = 100A/µs	-	50	-	ns
Q_{rr}	Reverse Recovery Charge		-	55	-	nC

Notes:

4. Characterised by design & tested at component level, not subject to production test at wafer level
5. Essentially independent of Operating Temperature Typical Characteristics

Ordering Guide

Part Number	Format	Detail / Drawing
FDP150N10AMW	Un-sawn wafer, electrical rejects inked	Page 3
FDP150N10AMWF	Sawn wafer on film-frame	Page 4
FDP150N10AMD	Singulated die / chips in waffle pack	Page 4
Note: Singulated Die / Chips can also be supplied in Pocket Tape or SurfTape® on request		

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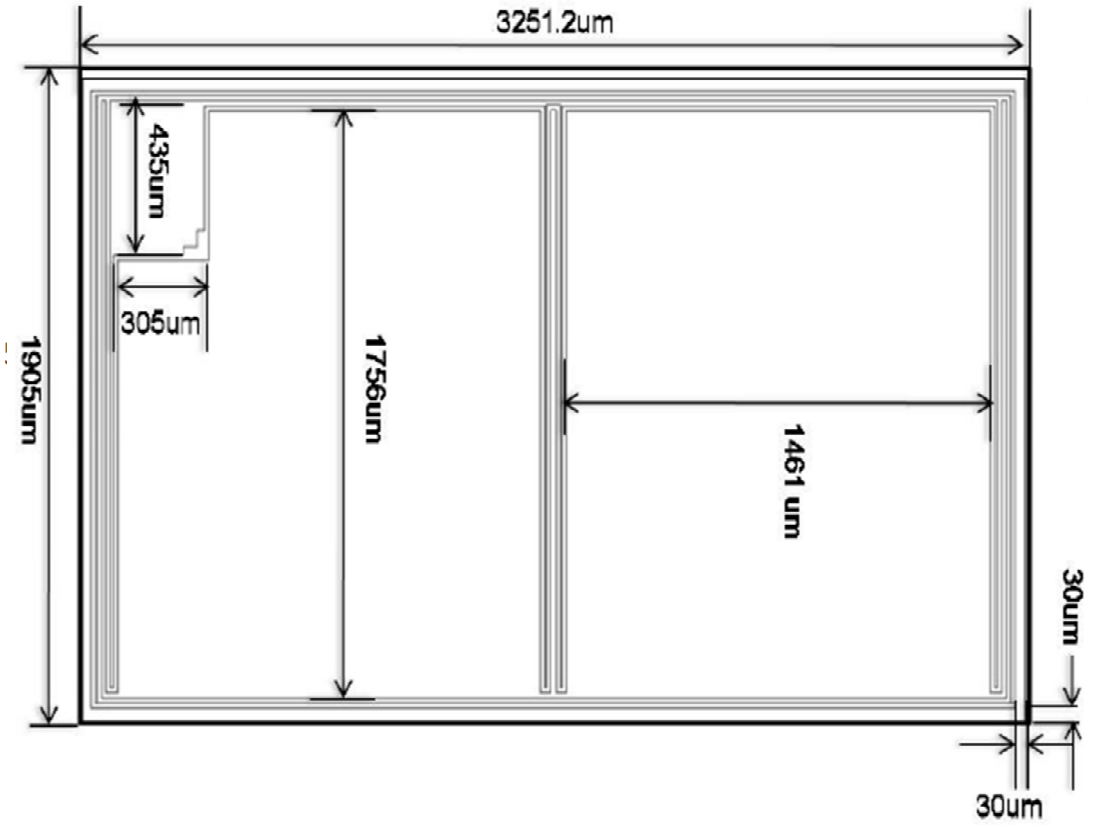
Die Drawing



Mechanical Data

Parameter			Units
Chip Dimensions Un-sawn	3251 x 1905		µm
Chip Thickness (Nominal)	200		µm
Gate Pad Size	305 x 435		µm
Wafer Diameter	200 (subject to change)		mm
Saw Street	80 (subject to change)		µm
Wafer orientation on frame	Wafer notch parallel with frame flat		
Topside Metallisation & Thickness	Al / Cu +TiW+Ti	4	µm
Backside Metallisation & Thickness	Ti-VNi-Ag	0.65	µm
Topside Passivation	Unpassivated		
Recommended Die Attach Material	Soft Solder or Conductive Epoxy		
Recommended Wire Bond - Gate	Al 125µm X1		
Recommended Wire Bond – Source	Al 500µm X2		

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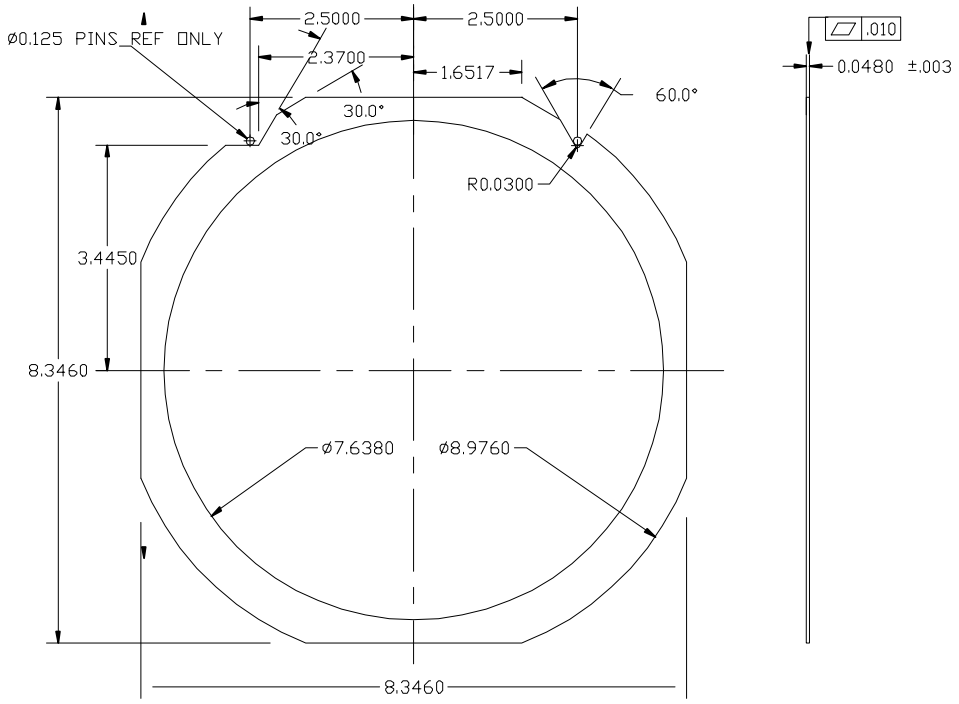
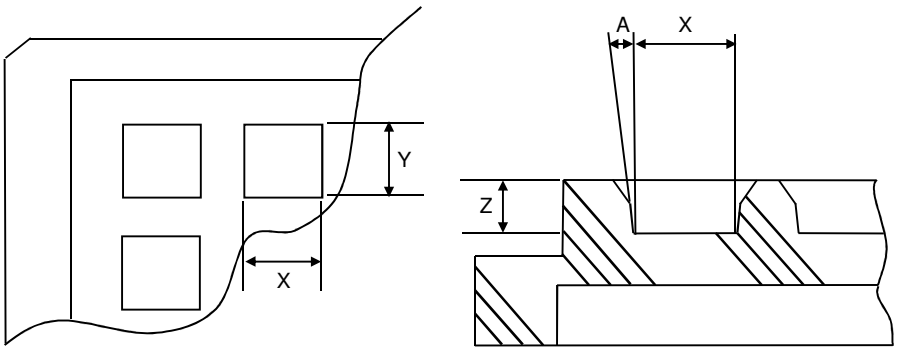
Sawn Wafer on Film-Frame – Dimensions (inches)



Die in Waffle Pack – Dimensions (mm)



X = 2.29mm ±0.13mm pocket size
Y = 3.30mm ±0.13mm pocket size
Z = 0.51mm ±0.08mm pocket depth
A = 5° ±1/2° pocket draft angle
No Cross Slots
Array = 13 X 10 (12)

OVERALL TRAY SIZE

Size = 50.67mm ±0.25mm
Height = 3.94mm ±0.13mm
Flatness = 0.30mm

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