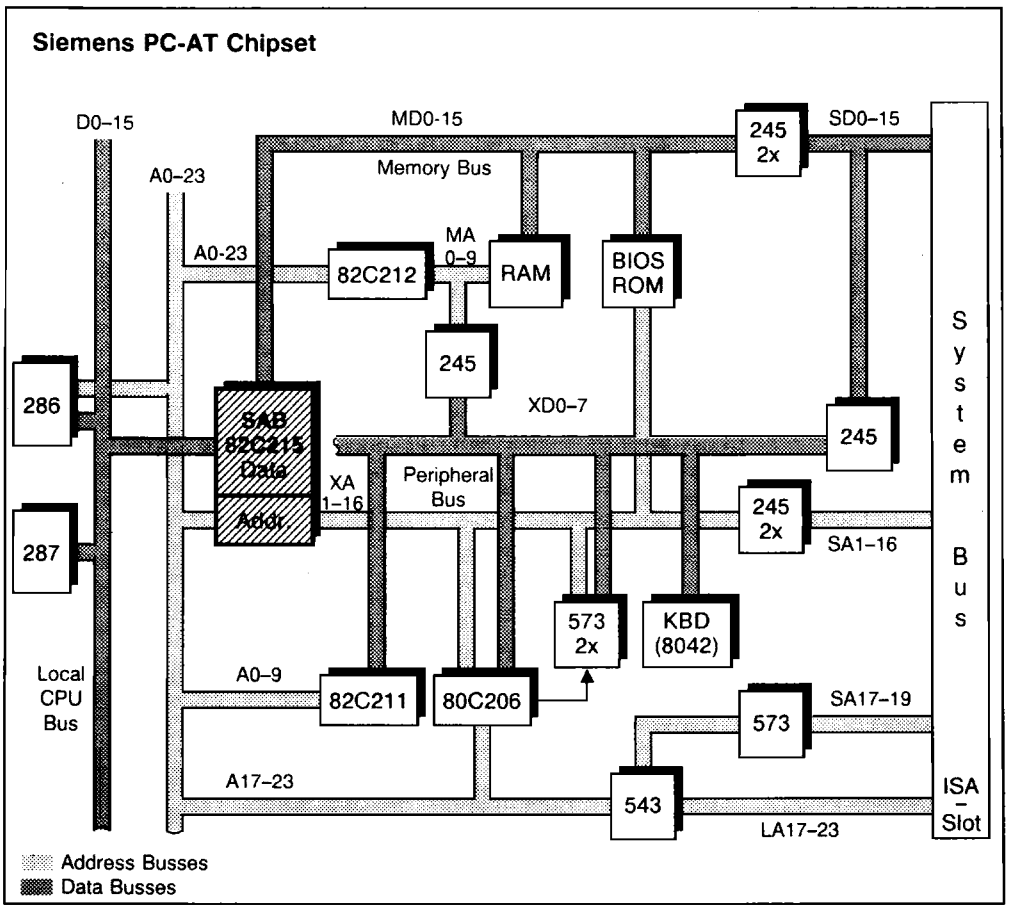
# Data / Address Buffer of Siemens PC-AT™ Chipset

# SAB 82C215

- Address buffer and latch for local CPU- and X-address bus interface
- Data buffer and latch for local CPU data bus / memory data bus interface
- Bus conversion logic for 16-bit to 8-bit transfers
- Parity generation / detection logic for memory data bus
- CMOS implementation for high speed and low power requirements
- 84-pin plastic leaded chip carrier package (PL-CC-84)



As a member of the Siemens PC-AT Chipset the SAB 82C215 provides address buffer / latch, data bus buffer / latch, data bus path conversion logic and parity logic.

The SAB 82C215 data / address buffer, the SAB 82C211 system controller, the SAB 82C212 memory controller and the SAB 82C206 integrated peripheral controller provide a highly integrated high performance system solution for PC-AT compatible systems.

The SAB 82C215 is fabricated in Siemens ACMOS technology and packaged in a 84-pin plastic leaded chip carrier package (PL-CC-84).

**Figure 1**
**Logic Symbol**

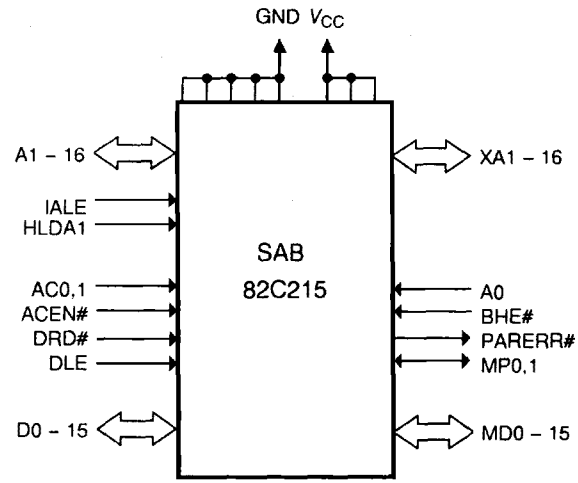
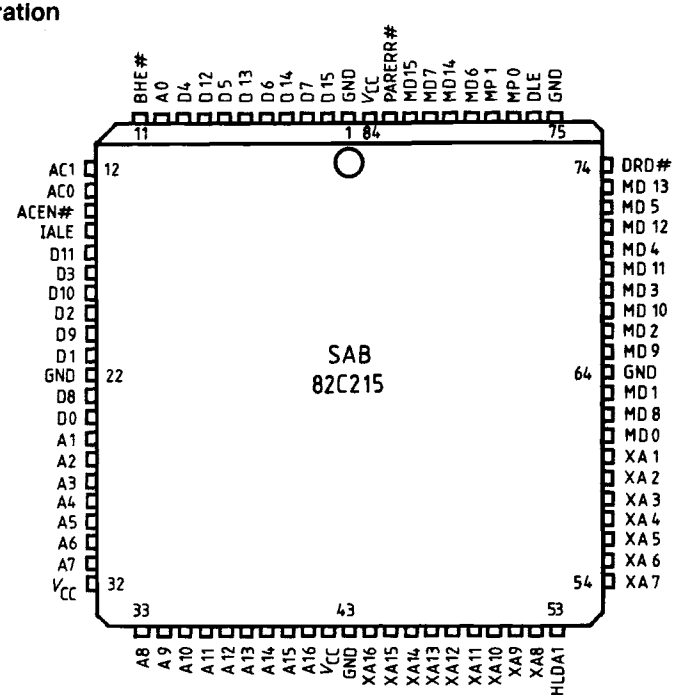



**Figure 2**
**Pin Configuration**



## Pin Definitions and Functions

| Symbol | Pin | Input (I) Output (O) | Function |
|---|---|---|---|
| **Address Latch / Buffers** | | | |
| IALE | 15 | I | **Address Latch Enable** IALE is the strobe input line of the address latch. It is used to latch the CPU addresses onto the X-address lines. |
| A1 – A16 | 25 – 31<br>33 – 41[1)] | I/O | **CPU Address Lines 1 – 16** During CPU cycles (HLDA1 = 0) A1 – A16 are the inputs to the internal address latch of the SAB 82C215. During DMA cycles (HLDA1 = 1) A1 – A16 are outputs. The address latch is controlled by IALE. |
| XA1 – XA16 | 60 – 54<br>52 – 44[1)] | I/O | **XBUS Address Lines 1 – 16** During CPU cycles (HLDA1 = 0) XA1 – 16 are the outputs of the address latch. During DMA cycles (HLDA1 = 1) XA1 – 16 are inputs. |
| HLDA1 | 53 | I | **Hold Acknowledge** HLDA1 indicates the type of cycle currently executing. CPU cycles are executed with HLDA1 = 0. During DMA cycles HLDA1 = 1. HLDA1 controls the direction of the address and data bus transfers. |
| **Data Buffers / Latch** | | | |
| D0 – D15 | 24, 23<br>21 – 16<br>9 – 2[1)] | I/O | **CPU Data Bus Lines 0 – 15** D0 – D15 represent the local CPU data bus lines. The data bus buffers are controlled by HLDA1 and DRD#. |
| AC0,1 | 13, 12 | I | **Action Code Line 0, 1** The two action code lines control the data path during CPU and DMA cycles. AC0,1 are qualified (enabled) by the ACEN# signal. At the Siemens PC-AT chipset AC0,1 are generated by the SAB 82C211. |

[1)] For detailed pin numbers see also pin configuration (figure 2).

4

## Pin Definitions and Functions (cont'd)

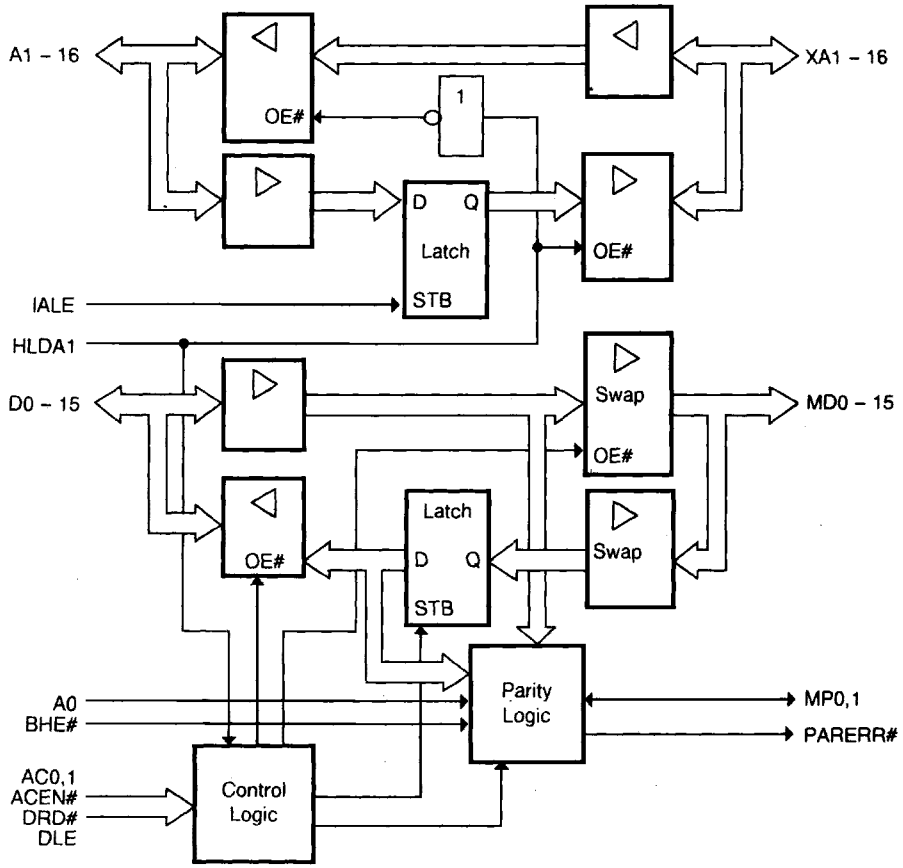
| Symbol | Pin | Input (I) Output (O) | Function |
|---|---|---|---|
| **Data Buffers / Latch** | | | |
| ACEN# | 14 | I | **Action Code Enable#** ACEN# = 0 validates the action code signals AC0,1. |
| MD0 – MD15 | 61 – 63<br>65 – 73<br>79 – 82[1)] | I/O | **Memory Data Bus 0 – 15** MD0 – MD15 are the memory data bus lines. They are controlled by HLDA1, DRD#, AC1,0 and ACEN#. |
| DRD# | 74 | I | **Data Read#** DRD# controls the direction of the data bus buffer path. DRD# = 1 sets the data path from local CPU bus to memory bus. DRD# = 0 sets the data path from memory to local CPU bus. |
| DLE | 76 | I | **Data Latch Enable** DLE controls the data bus latch. Memory bus data is stored in the latch with the high-to-low transition of DLE. |
| **Parity Generator / Checker** | | | |
| A0 | 10 | I | **Address Line 0** A0 is used to enable the low byte parity checking. |
| BHE# | 11 | I | **Byte High Enable#** BHE# is used to enable the high byte parity checking. |
| MP1, MP0 | 78, 77 | I/O | **Memory Parity Bit 1,0** MP1 and MP0 are the parity bits for the high and low order bytes of the system DRAM's. These lines are inputs during memory read operations for parity error detection and are outputs during memory write operations for parity generation. |
| PARERR# | 83 | O | **Parity Error#** PARERR# = 0 indicates that a parity error has been detected during a system memory read operation. At the Siemens PC-AT chipset PARERR# is checked by the SAB 82C211 system controller. |

1) For detailed pin numbers see also pin configuration (figure 2).

## Pin Definitions and Functions (cont'd)

| Symbol | Pin | Input (I) Output (O) | Function |
|---|---|---|---|
| **Power Supply** | | | |
| $V_{CC}$ | 32, 42, 84 | – | **Power Supply** (+5 V) |
| GND | 1, 22, 43, 64, 75 | – | **Ground** (0 V) |

**Figure 3**
**Block Diagram**




4

## Functional Description

The SAB 82C215 data / address buffer for the SIEMENS PC-AT chipset provides the following functional units:

- Address buffer and latch
- Data buffer and latch
- Data bus conversion logic
- Parity generation / detection logic

### Address Buffer and Latch

For local CPU cycles (HLDA1 = 0) the SAB 82C215 provides the address buffering and latching between the CPU address lines A1 – A16 and the peripheral bus address lines XA1 – XA16. A1 – A16 can be latched by the address latch enable signal IALE. The latch is transparent with IALE = high.

During DMA cycles (HLDA1 = 1) the peripheral address bus XA1 – XA16 is routed to the A1 – A16 address bus lines. The address latch is not available during DMA cycles.

### Data Buffer and Latch

The SAB 82C215 provides the buffering between the CPU data bus D0 – D15 and the memory data bus MD0 – MD15 for local cycles (on-board memory read / write cycles) or AT-bus cycles (on-board peripherals or AT-slot read / write cycles).

DRD# is the direction control signal for the data buffer. For local write cycles DRD# is at high level and sets the data path from the CPU data bus to the memory data bus. For local read cycles DRD# = 0 sets the data path from MD-bus to D-bus. DLE controls the data latch. DLE = 1 makes the latch transparent. During local cycles the action code enable signal is inactive (ACEN# = 1).

During AT-bus cycles DLE is inactive (low), and instead of DLE the ACEN# signal is used to strobe the data into the data latch. With ACEN# = 0 the data latch is transparent and data is stored with the low-to-high transition of ACEN#.

During DMA cycles the D-bus of the SAB 82C215 is switched off. During DMA memory write operations (AC1,0 = 0,0 and 1,0), the MD-bus lines are connected to the parity generator. If data bus conversion is required during DMA cycles (AC1,0 = 1,0 and 1,1), the corresponding data path is set between MD0 – 7 and MD8 – 15.

### Data Bus Conversion Logic

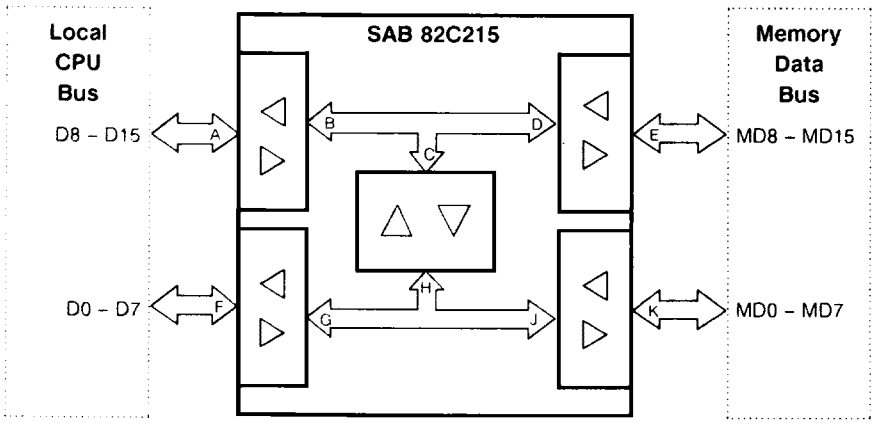
The SAB 82C215 provides data bus conversion when the 16-bit CPU reads from or writes to 8-bit devices. It also provides data bus conversion for DMA cycles. Table 1 lists the possible cases of the data paths for CPU and DMA cycles. The action code signals AC1, 0, which are qualified by ACEN#, control the different data path configurations.

**Table 1:**
**Action Code Functions**

| AC1 | AC0 | HLDA1 | Operation | Data path [1] |
|---|---|---|---|---|
| 0 | 0 | 0 | 16-bit Write | A-B-D-E and F-G-J-K |
| | | | 8-bit Low Write | F-G-J-K |
| 0 | 1 | 0 | 16-bit Read | E-D-B-A and K-J-G-F |
| | | | 8-bit Low Read | K-J-G-F |
| 1 | 0 | 0 | 8-bit High Write to MD-bus low | A-B-C-H-J-K |
| 1 | 1 | 0 | 8-bit Read MD-bus Low to D-bus high | K-J-H-C-B-A |
| 0 | 0 | 1 | MD-bus tristated: 16-bit/8-bit (low byte) DMA read / write at MD-bus | – |
| 0 | 1 | 1 | reserved | – |
| 1 | 0 | 1 | High memory Write to MD8 – 15 from MD0 – 7 | K-J-H-C-D-E |
| 1 | 1 | 1 | High memory Read from MD8 – 15 to MD0 – 7 | E-D-C-H-J-K |

1) see figure 4

**Figure 4**
**Data Bus Conversion Paths**




4

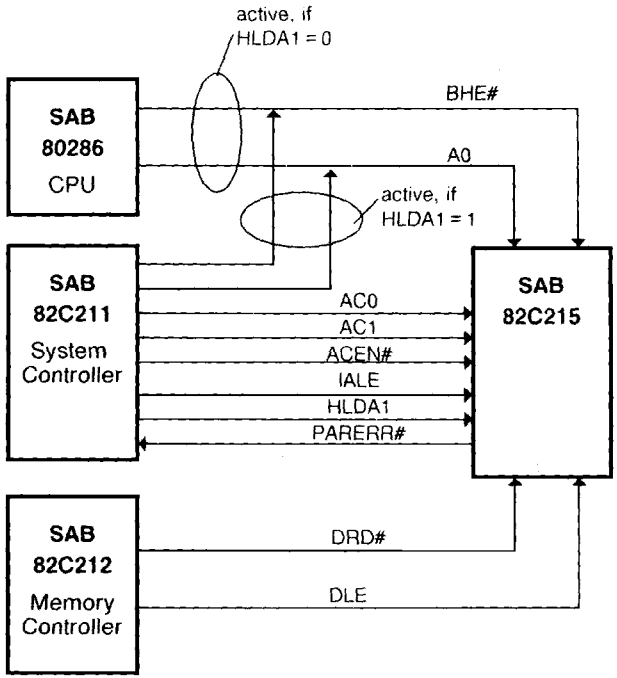
### Parity Generation / Detection Logic

For local memory write cycles the SAB 82C215 generates an even parity bit (MP0, MP1) for each of the two data bytes MD0 – 7 and MD8 – 15. The parity bit is set if the corresponding data byte has an even number of 1's. During local memory read cycles the SAB 82C215 checks the data bytes for even parity. If a parity error is detected, the PARERR# output becomes active (low). PARERR# is activated by the falling edge of DLE and deactivated by the rising edge of DRD#. For DMA cycles (HLDA1 = 1) the parity checker is disabled. During parity checking A0 and BHE# select the data bytes to be checked.

### SAB 82C215 control lines interface

The SAB 82C215 has several control lines. In a PC-AT design using the Siemens PC-AT chipset the interface of the SAB 82C215 control lines is shown in the next figure.

**Figure 5**
**Interface of the SAB 82C215 control lines in the Siemens PC-AT Chipset**



## Absolute Maximum Ratings

Ambient temperature under bias ..... 0 to 70 °C
Storage temperature ..... - 65 to + 150 °C
Supply voltage ..... - 0.5 to + 7.5 V
Voltage on any pin with respect to ground ..... - 0.5 to $V_{CC}$ + 0.5 V
Power dissipation ..... 1 W

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## DC Characteristics

$T_A$ = 0 to 70 °C; $V_{CC}$ = + 5 V ± 5 %; GND = 0 V

| Parameter | Symbol | Limit values | | Unit | Test condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Input low voltage | $V_{IL}$ | – 0.5 | 0.8 | V | – |
| Input high voltage | $V_{IH}$ | 2.0 | $V_{CC}$ + 0.5 | V | – |
| Output low voltage | $V_{OL}$ | – | 0.45 | V | MD0 – 15: $I_{OL}$ = 8 mA<br>other outputs:<br>$I_{OL}$ = 4 mA |
| Output high voltage | $V_{OH}$ | 2.4 | – | V | MD0 – 15: $I_{OH}$ = - 8 mA<br>other outputs:<br>$I_{OH}$ = - 4 mA |
| Input leakage current | $I_{IL}$ | – | ± 10 | µA | 0 V < $V_{IN}$ < $V_{CC}$ |
| Output tristate leakage current | $I_{OZ}$ | – | ± 10 | µA | 0.45 V < $V_{OUT}$ < $V_{CC}$ |
| Power supply current | $I_{CC}$ | – | 80 | mA | @16 MHz |
| Standby power supply current | $I_{CCSB}$ | – | 1.0 | mA | – |

4

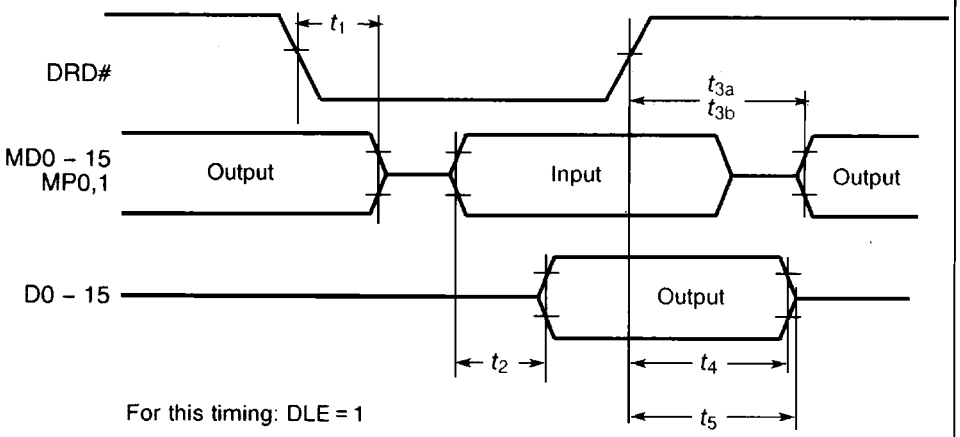
## AC Characteristics

$T_A$ = 0 to 70 °C; $V_{CC}$ = +5 V ± 5 %; GND = 0 V

| Parameter | Symbol | Limit values | | Unit | Test condition |
|---|---|---|---|---|---|
| | | min. | max. | | |
| MD-bus tristated after DRD# active | $t_1$ | 7.5 | 24 | ns | – |
| MD-bus valid to D-bus valid | $t_2$ | 8 | 18.5 | ns | – |
| MD-bus being driven after DRD# inactive | $t_{3a}$ | 7.5 | 28 | ns | – |
| MP0, MP1 being driven after DRD# inactive | $t_{3b}$ | 6 | 23 | ns | – |
| D-bus invalid after DRD# inactive | $t_4$ | 4 | 13 | ns | – |
| D-bus tristated after DRD# inactive | $t_5$ | 6 | 15 | ns | – |
| D-bus valid to MD-bus valid | $t_6$ | 11 | 19 | ns | – |
| D-bus valid to MP1, MP0 valid | $t_7$ | 11 | 20 | ns | – |
| ACEN# active to D-bus valid | $t_8$ | 16 | 27 | ns | – |
| Action code valid to MD-bus valid | $t_9$ | 10 | 19 | ns | – |
| Action code invalid to MD-bus invalid | $t_{10}$ | 11 | 20 | ns | – |
| DLE inactive to PARERR# enabled | $t_{11}$ | 17 | 30 | ns | – |
| DRD# inactive to PARERR# disabled | $t_{12}$ | 17 | 28 | ns | – |
| IALE active to XA-bus valid | $t_{13}$ | 11 | 19 | ns | – |
| XA-bus valid to A-bus valid SAB 82C215-12<br>SAB 82C215-15 | $t_{14}$ | 7<br>7 | 19<br>16 | ns<br>ns | –<br>– |
| MD, MP setup time to DLE trailing edge | $t_{15}$ | 0 | – | ns | – |
| MD, MP hold time from DLE trailing edge | $t_{16}$ | 6 | – | ns | – |
| DRD# setup time to DLE trailing edge | $t_{17}$ | 12 | – | ns | – |
| MD-bus hold time from ACEN# trailing edge | $t_{19}$ | 7.5 | – | ns | – |
| MD-bus valid to MP valid during DMA memory write cycle | $t_{20}$ | 14 | 24 | ns | – |
| MD-bus high byte valid to MD low byte valid during DMA high memory read cycle | $t_{21}$ | 10 | 19 | ns | – |
| Action code valid to MD high byte valid during DMA high memory write cycle | $t_{22}$ | 9 | 18 | ns | – |
| Action code valid to MP valid during DMA high memory write cycle | $t_{23}$ | 17 | 28 | ns | – |

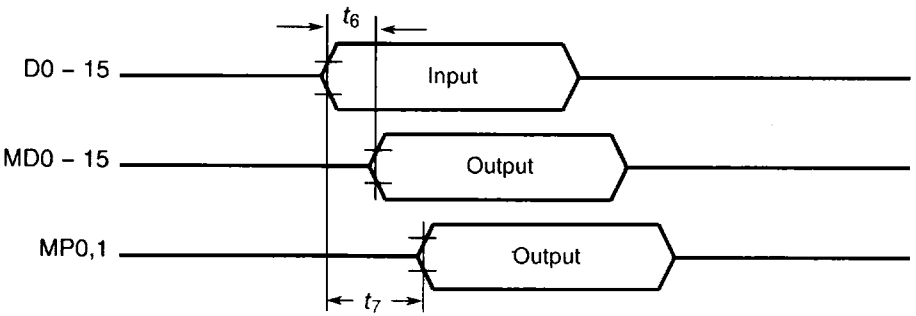
## Timing Diagrams

### CPU Read Timing

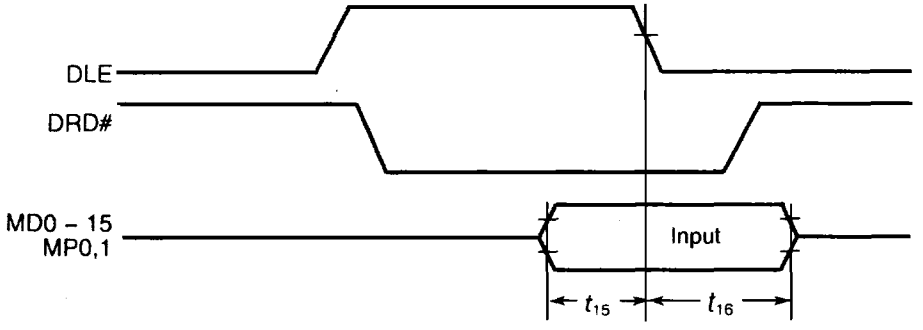



For this timing: DLE = 1

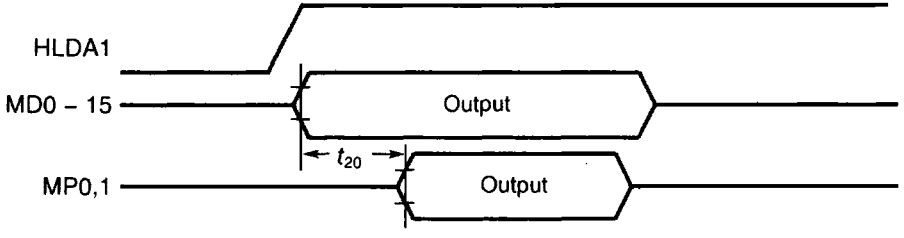
### CPU Write Timing



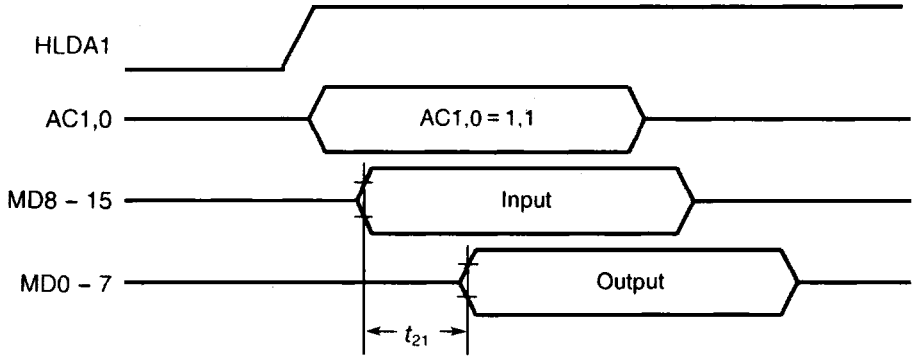
**Data Latch Timing (CPU Read)**



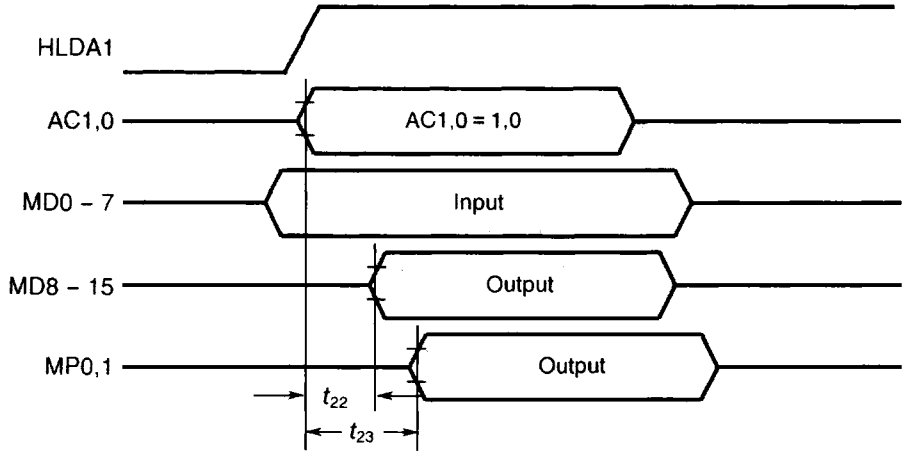

**DMA Timing (HLDA1 = 1)**
Memory Write Cycle



**DMA Timing (HLDA1 = 1)**
Memory Read High Byte / I/O Write Low Byte

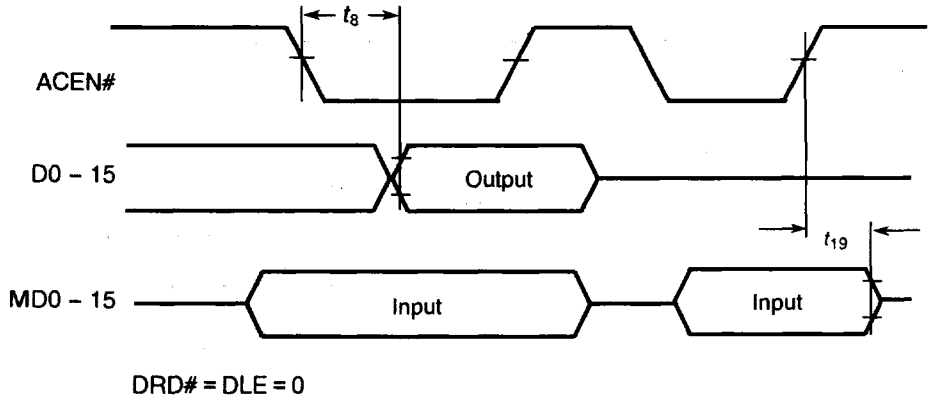



**DMA Timing (HLDA1 = 1)**
I/O Read Low Byte / Memory Write High Byte



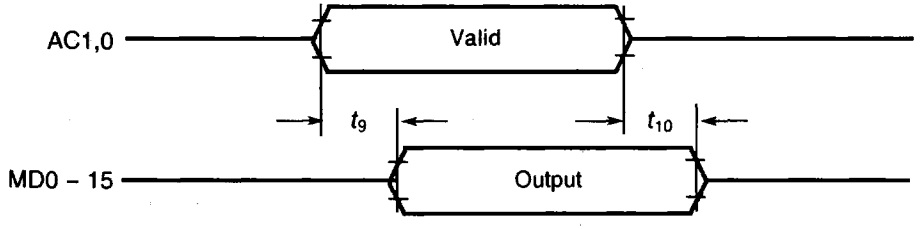

4

**ACEN# Timing**



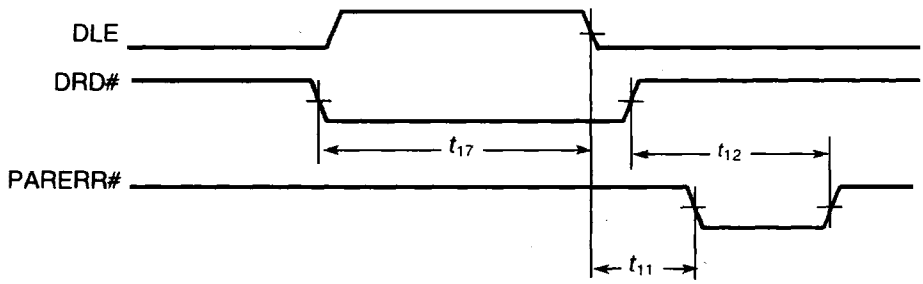

DRD# = DLE = 0

**Action Code Timing**

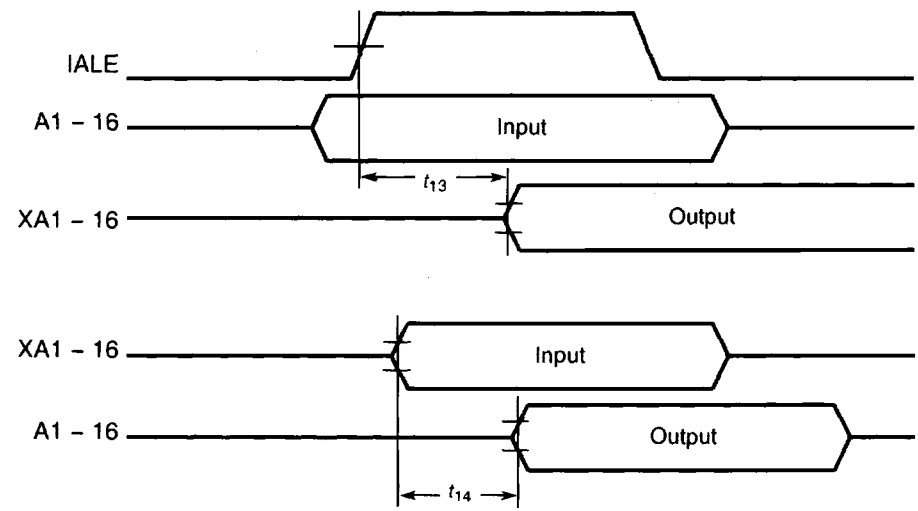



ACEN# = 0

**PARERR# Timing**

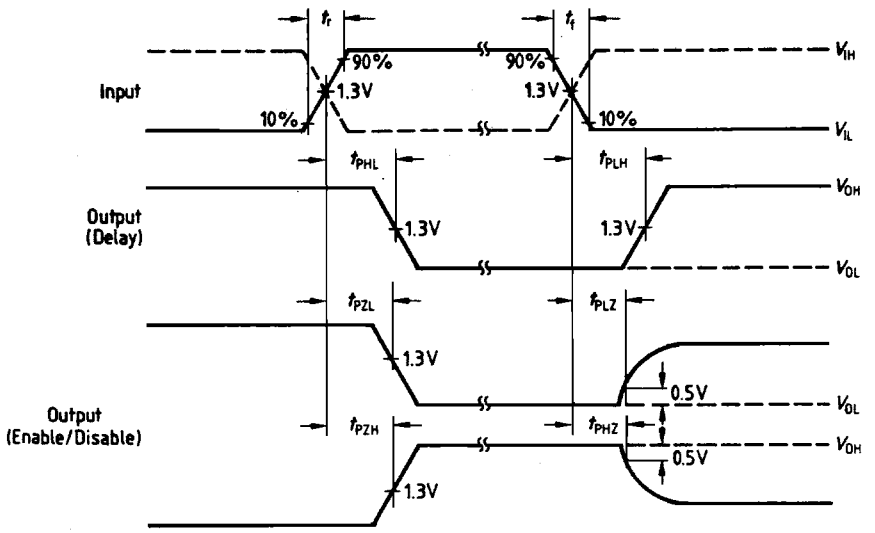



**Adress Latch Timing**

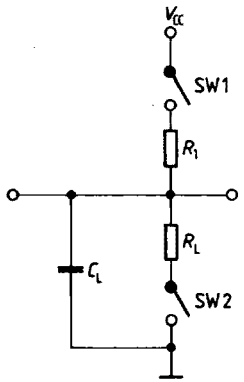



4

## Load Circuit and AC Characteristics Measurement Waveform




$V_{IH}$ = 3V, $V_{IL}$ = 0V, $t_r \leq 10$ns, $t_f \geq 5$ns



### Load Circuit Measurement Conditions

| Parameter | Output Type | Symbol | $C_L$ (pF) | $R_1$ (kΩ) | $R_L$ (kΩ) | $SW_1$ | $SW_2$ |
|---|---|---|---|---|---|---|---|
| Propagation Delay Time | Totem Pole | | | | | | |
| | Tristate | $t_{PLH}$ | 50 | – | 1.0 | OFF | ON |
| | Bidirectional | $t_{PHL}$ | 50 | – | 1.0 | OFF | ON |
| Propagation Delay Time | Open Drain or | $t_{PLH}$ | 50 | 0.5 | – | ON | OFF |
| | Open Collector | $t_{PHL}$ | 50 | 0.5 | – | ON | OFF |
| Disable Time | Tristate | $t_{PLZ}$ | 5 | 0.5 | 1.0 | ON | |
| | Bidirectional | $t_{PHZ}$ | 5 | 0.5 | 1.0 | OFF | ON |
| Enable Time | Tristate | $t_{PZL}$ | 50 | 0.5 | 1.0 | ON | ON |
| | Bidirectional | $t_{PZH}$ | 50 | 0.5 | 1.0 | OFF | ON |

4