



## 54F/74F524 8-Bit Registered Comparator

### General Description

The 'F524 is an 8-bit bidirectional register with parallel input and output plus serial input and output progressing from LSB to MSB. All data inputs, serial and parallel, are loaded by the rising edge of the input clock. The device functions are controlled by two control lines ( $S_0$ ,  $S_1$ ) to execute shift, load, hold and read out.

An 8-bit comparator examines the data stored in the registers and on the data bus. Three true-HIGH, open-collector outputs representing 'register equal to bus', 'register greater than bus' and 'register less than bus' are provided. These outputs can be disabled to the OFF state by the use of Status Enable ( $\overline{SE}$ ). A mode control has also been provided

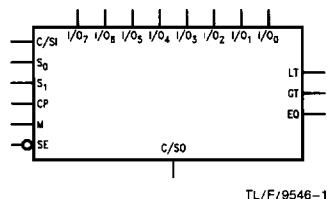
to allow two's complement as well as magnitude compare. Linking inputs are provided for expansion to longer words.

### Features

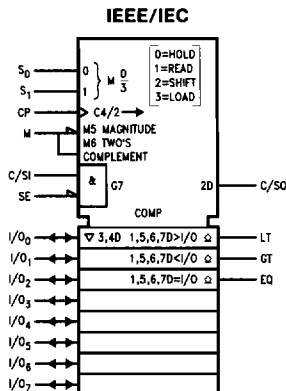
- 8-Bit bidirectional register with bus-oriented input-output
- Independent serial input-output to register
- Register bus comparator with 'equal to', 'greater than' and 'less than' outputs
- Cascadable in groups of eight bits
- Open-collector comparator outputs for AND-wired expansion
- Two's complement or magnitude compare

**Ordering Code:** See Section 5

### Logic Symbols



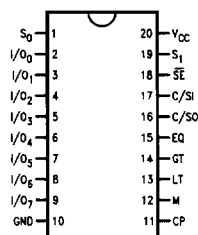
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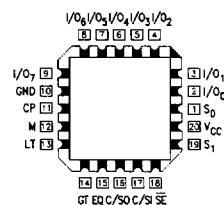
### Connection Diagrams

**Pin Assignment for  
DIP, SOIC and Flatpak**



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**Pin Assignment  
for LCC and PCC**



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## Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$S_0, S_1$	Mode Select Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
C/SI	Status Priority or Serial Data Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
SE	Status Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
M	Compare Mode Select Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$I/O_0-I/O_7$	Parallel Data Inputs or TRI-STATE* Parallel Data Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A/ -0.65 mA -3 mA/24 mA (20 mA)
C/SO	Status Priority or Serial Data Output	50/33.3	-1 mA/20 mA
LT	Register Less Than Bus Output	OC*/33.3	*/20 mA
EQ	Register Equal Bus Output	OC*/33.3	*/20 mA
GT	Register Greater Than Bus Output	OC*/33.3	*/20 mA

\*OC = Open Collector

## Functional Description

The 'F524 contains eight D-type flip-flops connected as a shift register with provision for either parallel or serial loading. Parallel data may be read from or loaded into the registers via the data bus  $I/O_0-I/O_7$ . Serial data is entered from the C/SI input and may be shifted into the register and out through the C/SO output. Both parallel and serial data entry occur on the rising edge of the input clock (CP). The operation of the shift register is controlled by two signals  $S_0$  and  $S_1$  according to the Select Truth Table. The TRI-STATE parallel output buffers are enabled only in the Read mode.

One port of an 8-bit comparator is attached to the data bus while the other port is tied to the outputs of the internal register. Three active-OFF, open-collector outputs indicate whether the contents held in the shift register are 'greater than', (GT), 'less than' (LT), or 'equal to' (EQ) the data on the input bus. A HIGH signal on the Status Enable (SE) input disables these outputs to the OFF state. A mode control input (M) allows selection between a straightforward magnitude compare or a comparison between twos complement numbers.

For 'greater than' or 'less than' detection, the C/SI input must be held HIGH, as indicated in the Status Truth Table. The internal logic is arranged such that a LOW signal on the C/SI input disables the 'greater than' and 'less than' outputs. The C/SO output will be forced HIGH if the 'equal to' status condition exists, otherwise C/SO will be held LOW. These facilities enable the 'F524 to be cascaded for word length greater than eight bits.

Word length expansion (in groups of eight bits) can be achieved by connecting the C/SO output of the more significant byte to the C/SI input of the next less significant byte and also to its own SE input (see Figure 1). The C/SI input of the most significant device is held HIGH while the SE input of the least significant device is held LOW. The corresponding status outputs are AND-wired together. In the case of twos complement number compare, only the Mode input to the most significant device should be HIGH. The Mode inputs to all other cascaded devices are held LOW.

Suppose that an inequality condition is detected in the most significant device. Assuming that the byte stored in the register is greater than the byte on the data bus, the EQ and LT outputs will be pulled LOW and the GT output will float HIGH. Also the C/SO output of the most significant device will be forced LOW, disabling the subsequent devices but enabling its own status outputs. The correct status condition is thus indicated. The same applies if the registered byte is less than the data byte, only in this case the EQ and GT outputs go LOW and LT output floats HIGH.

If an equality condition is detected in the most significant device, its C/SO output is forced HIGH. This enables the next less significant device and also disables its own status outputs. In this way, the status output priority is handed down to the next less significant device which now effectively becomes the most significant byte. The worst case propagation delay for a compare operation involving 'n' cascaded 'F524s will be when an equality condition is detected in all but the least significant byte. In this case, the status priority has to ripple all the way down the chain before the correct status output is established. Typically, this will take  $35 + 6(n-2)$  ns.

Select Truth Table

$S_0$	$S_1$	Operation
L	L	Hold—Retains Data in Shift Register
L	H	Read—Read Contents in Register onto Data Bus, Data Remains in Register Unaffected by Clock
H	L	Shift—Allows Serial Shifting on Next Rising Clock Edge
H	H	Load—Load Data on Bus into Register

### Functional Description (Continued)

### Number Representation Select Table

M	Operation
L	Magnitude Compare
H	Twos Complement Compare

### Status Truth Table (Hold Mode)

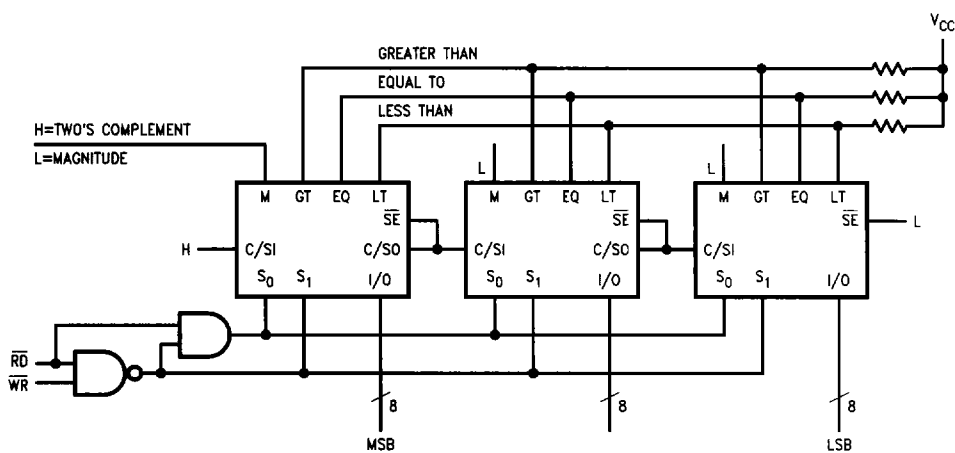
Inputs			Outputs			
SE	C/SI	Data Comparison	EQ	GT	LT	C/SO
H	H	X	H	H	H	1
H	L	X	H	H	H	L
L	L	$O_A - O_H > 1/O_0 - 1/O_7$	L	H	H	L
L	L	$O_A - O_H = 1/O_0 - 1/O_7$	H	H	H	L
L	L	$O_A - O_H < 1/O_0 - 1/O_7$	L	H	H	L
L	H	$O_A - O_H > 1/O_0 - 1/O_7$	L	H	L	L
L	H	$O_A - O_H = 1/O_0 - 1/O_7$	H	L	L	H
L	H	$O_A - O_H < 1/O_0 - 1/O_7$	L	L	H	L

1 = HIGH if data are equal, otherwise LOW

H = HIGH Voltage Level

L = LOW Voltage Level

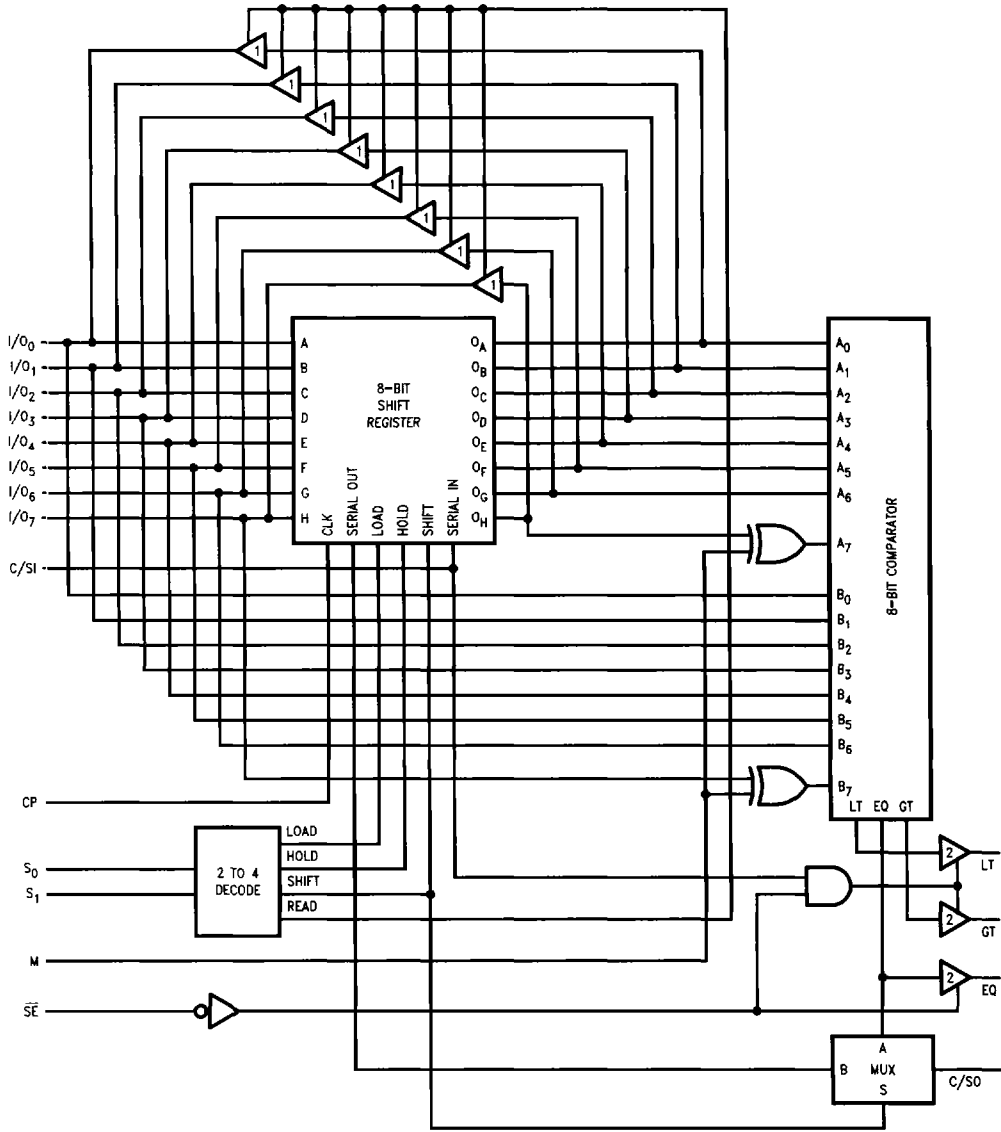
X = Immaterial



**FIGURE 1. Cascading 'F524s for Comparing Longer Words**

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# Block Diagram



TL/F/9546-5

## Notes:

1. TRI-STATE Output
2. Open-Collector Output

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	– 65°C to + 150°C
Ambient Temperature under Bias	– 55°C to + 125°C
Junction Temperature under Bias	– 55°C to + 175°C
V <sub>CC</sub> Pin Potential to Ground Pin	– 0.5V to + 7.0V
Input Voltage (Note 2)	– 0.5V to + 7.0V
Input Current (Note 2)	– 30 mA to + 5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	– 0.5V to V <sub>CC</sub>
TRI-STATE Output	– 0.5V to + 5.5V

Current Applied to Output in LOW State (Max) twice the rated I<sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	– 55°C to + 125°C
Commercial	0°C to + 70°C
Supply Voltage	
Military	+ 4.5V to + 5.5V
Commercial	+ 4.5V to + 5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			– 1.2	V	Min	I <sub>IN</sub> = – 18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = – 1 mA I <sub>OH</sub> = – 3 mA I <sub>OH</sub> = – 1 mA I <sub>OH</sub> = – 3 mA I <sub>OH</sub> = – 1 mA I <sub>OH</sub> = – 3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA (I/O <sub>n</sub> ) I <sub>OL</sub> = 20 mA (I/O <sub>n</sub> ) I <sub>OL</sub> = 24 mA (LT, GT, EQ, C/SO)
I <sub>IH</sub>	Input HIGH Current			20	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			100	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V <sub>IN</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current			– 0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			– 650	μA	Max	V <sub>I/O</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	– 60	– 150		mA	Max	V <sub>OUT</sub> = 0V
I <sub>CEX</sub>	Output HIGH Leakage Current			250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>OHC</sub>	Open Collector, Output OFF Leakage Test			250	μA	Min	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCH</sub>	Power Supply Current		128	180	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current		128	180	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current		128	180	mA	Max	V <sub>O</sub> = HIGH Z

# AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig No
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f <sub>max</sub>	Maximum Shift Frequency	50	75				50		MHz	2-1
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I/O <sub>n</sub> to EQ	9.0 5.0	16.5 9.5	20.0 12.0			9.0 5.0	21.0 13.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I/O <sub>n</sub> to GT	8.5 6.5	14.1 13.0	19.0 16.5			8.5 6.5	20.0 17.5		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I/O <sub>n</sub> to LT	7.0 4.5	15.5 10.0	20.0 14.0			7.0 4.5	21.0 15.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay I/O <sub>n</sub> to C/SO	8.0 6.0	15.2 12.5	19.5 16.0			8.0 6.0	20.5 17.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to EQ	10.0 4.0	20.0 8.5	25.0 16.5			10.0 4.0	26.0 17.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to GT	10.0 8.5	16.5 17.0	21.0 22.0			10.0 8.5	22.0 23.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to LT	9.0 5.5	20.0 13.5	25.0 17.0			9.0 5.5	26.0 18.0		
t <sub>PLH</sub>	Propagation Delay CP to C/SO (Load)	8.5	16.5	21.0			8.5	22.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to C/SO (Serial Shift)	5.0 4.5	10.0 9.0	13.0 11.5			5.0 4.5	14.0 12.5		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C/SI to GT	9.0 3.0	15.0 6.5	19.0 8.5			9.0 3.0	20.0 9.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C/SI to LT	8.0 3.5	15.5 6.5	20.0 8.5			8.0 3.5	21.0 9.5		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> , S <sub>1</sub> to C/SO	6.5 5.5	11.5 14.0	14.5 18.0			6.5 5.5	15.5 19.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SE to EQ	3.5 2.5	8.0 6.0	10.5 8.0			3.5 2.5	11.5 9.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SE to GT	6.5 3.5	12.5 6.0	16.0 8.0			6.5 3.5	17.0 9.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SE to LT	5.0 3.5	10.5 6.0	13.5 8.0			5.0 3.5	14.5 9.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C/SI to C/SO	4.0 4.0	8.5 8.5	11.0 11.0			4.0 4.0	12.0 12.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay M to GT	8.0 6.0	15.0 12.0	19.5 15.5			8.0 6.0	20.5 16.5	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay M to LT	8.0 4.5	17.0 9.5	22.0 12.0			8.0 4.5	23.0 13.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> , S <sub>1</sub> to EQ	15.0 9.0	25.0 15.0	33.0 19.0			15.0 9.0	35.0 20.0	ns	2-3
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> , S <sub>1</sub> to GT	10.5 10.5	18.0 18.0	23.0 23.0			10.5 10.5	24.0 24.0		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay S <sub>0</sub> , S <sub>1</sub> to LT	13.0 12.0	22.0 19.0	28.0 24.0			13.0 12.0	30.0 25.0		
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time S <sub>0</sub> , S <sub>1</sub> to I/O <sub>n</sub>	4.5 5.5	10.0 11.0	13.0 15.0			4.5 5.5	14.0 16.0	ns	2-5
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time S <sub>0</sub> , S <sub>1</sub> to I/O <sub>n</sub>	3.5 4.5	8.0 9.6	12.0 12.5			3.5 4.5	13.0 13.5		

# AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		54F		74F		Units	Fig No
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW I/O <sub>n</sub> to CP	6.0 6.0				6.0 6.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW I/O <sub>n</sub> to CP	0 0				0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	10.0 10.0				10.0 10.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW S <sub>0</sub> or S <sub>1</sub> to CP	0 0				0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW C/SI to CP	7.0 7.0				7.0 7.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW C/SI to CP	0 0				0 0			
$t_w(\text{H})$	Clock Pulse Width, HIGH	5.0				5.0		ns	2-4