MOTOROLA

Quad TTL-to-MECL Translator

ELECTRICALLY TESTED PER:
MIL-M-38510/06301

The 10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MECL 10524 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the logic low level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, + 5.0 Volts, and – 5.2 Volts. Propagation delay of the 10524 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the 10515 or 10516 differential receivers. The 10524 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communication systems.

- 205 mW Max/Pkg (No Load)
- t_{pd} = 3.5 ns typ (1.5 Vdc in to 50% out)
- t_r, t_f = 2.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
B_{OUT}	1	5	2	50 Ω to V_{TT}
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{B_{OUT}}$	3	7	4	50 Ω to V_{TT}
$\overline{A_{OUT}}$	4	8	5	50 Ω to V_{TT}
A_{IN}	5	9	7	V_{CC}
Common Strobe	6	10	8	V_{CC}
B_{IN}	7	11	9	V_{CC}
V_{EE}	8	12	10	V_{EE}
V_{CC}	9	13	12	V_{CC}
C_{IN}	10	14	13	V_{CC}
D_{IN}	11	15	14	V_{CC}
$\overline{C_{OUT}}$	12	16	15	51 Ω to V_{TT}
$\overline{D_{OUT}}$	13	1	17	51 Ω to V_{TT}
D_{OUT}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	GND
GND	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

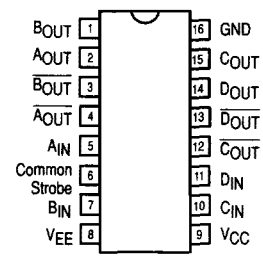
Military 10524

AVAILABLE AS

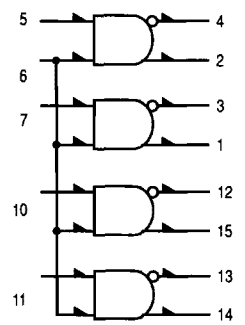
1) JAN: JM 38510/06301
2) SMD: N/A
3) 883: 10524/BXAJC
X = CASE OUTLINE AS FOLLOWS:

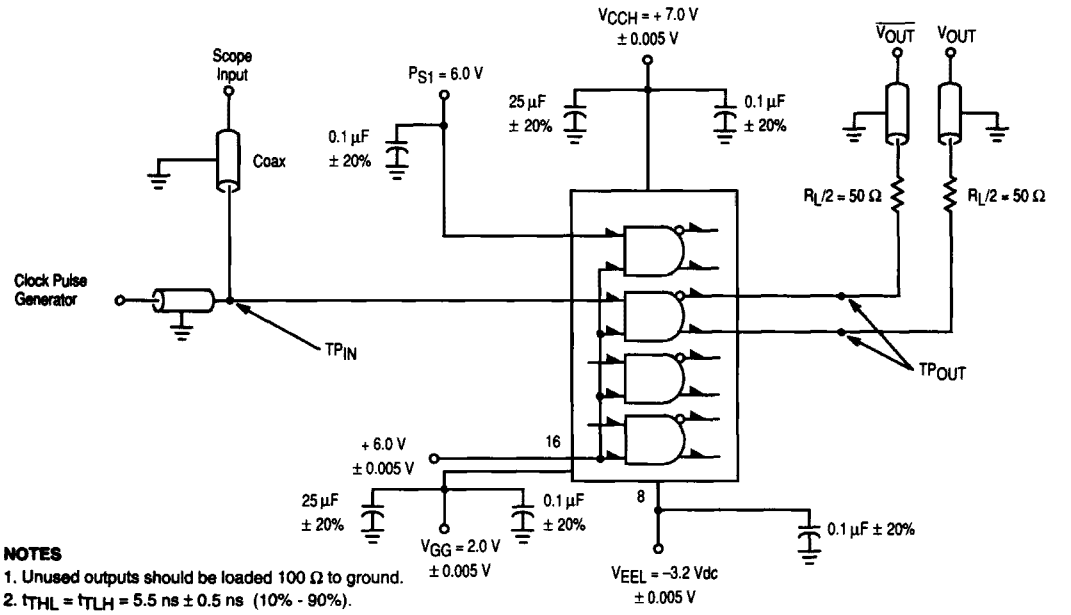
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Unused outputs should be loaded 100 Ω to ground.
2. $t_{THL} = t_{TLH} = 5.5$ ns ± 0.5 ns (10% - 90%).
3. $t_p = 40$ ns ± 2.0 ns.
4. $Z_{OUT} \approx 50\ \Omega$.
5. C_L = Jig and stray capacitance ≤ 5.0 pF.

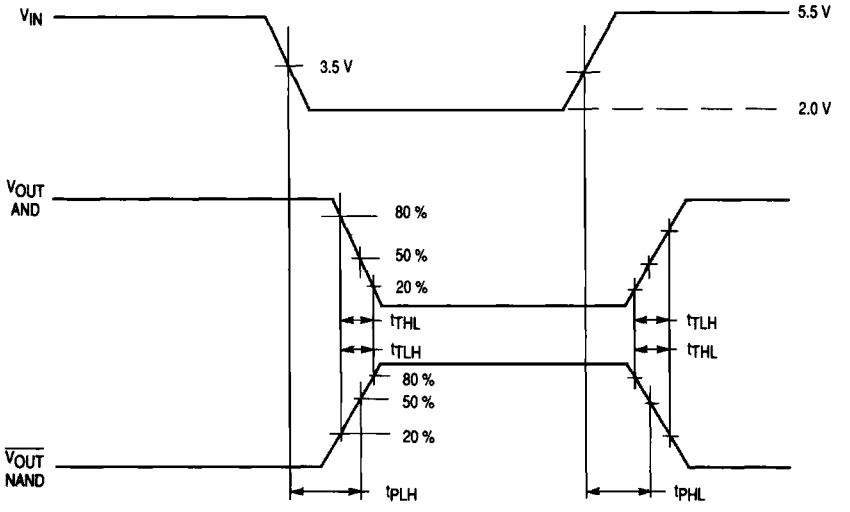


Figure 1. Switching Test Circuit and Waveforms

NOTES

1. 50 Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.

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QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CCH}	V_{GG}	V_{EE}	V_{EEL}
T_A = 25 °C	+ 2.4	+ 0.4	+ 1.10	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = 125 °C	+ 2.4	+ 0.4	+ 0.80	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = - 55 °C	+ 2.4	+ 0.4	+ 1.10	+ 2.00	+ 7.0	+ 2.0	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 5.0 V, I_{IN} = 10 mA, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	I_{IN}	GND	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.76	- 0.825	- 0.63	- 1.08	- 0.88	V	5, 6, 7, 10, 11	6				16	8	9	1 - 4, 12 - 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	5, 6, 7, 10, 11	6				16	8	9	1 - 4, 12 - 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	5, 6, 7, 10, 11		5, 6, 7, 10, 11	5, 6, 7, 10, 11		16	8	9	1 - 4, 12 - 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	5, 6, 7, 10, 11		5, 6, 7, 10, 11	5, 6, 7, 10, 11		16	8	9	1 - 4, 12 - 15
I_{EE}	Power Supply Current	- 66		- 73		- 73		mA						16	8	9	8
I_{IH1}	Input Current High		50		85		85	µA	5, 7, 10, 11					6, 16	8	9	5, 7, 10, 11
I_{IL1}	Input Current Low	- 3.2		- 5.5		- 3.2		mA	6	5, 7, 10, 11				16	8	9	5, 7, 10, 11
I_{IH2}	Input Current High		200		340		340	µA	6					5, 7, 10, 11, 16	8	9	6
I_{IL2}	Input Current Low	- 12.8		- 22		- 12.8		mA		6				16	8	9	6
V_{IC}	Input Clamp Voltage	- 1.5						V					5 - 7 10, 11	16	8	9	5 - 7 10, 11

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QUIESCENT LIMIT TABLE *

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Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CCH}	V_{GG}	V_{EE}	V_{EEL}
T_A = 25 °C	+ 2.4	+ 0.4	+ 1.10	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = 125 °C	+ 2.4	+ 0.4	+ 0.80	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = - 55 °C	+ 2.4	+ 0.4	+ 1.10	+ 2.00	+ 7.0	+ 2.0	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 5.0 V, I_{IN} = 1.0 mA, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	I_{IN}	GND	V_{EE}	V_{CC}	P. U. T.
I_{CCL} I_{CCH}	Positive Power Supply Current Drain		25 16		28 18		28 18	mA mA						5, 7, 10, 11, 16	8	5 - 7, 9, 10, 11	9
BV_{IN}	Input Breakdown Voltage	5.5		5.5		5.5		V		6			5 - 7 10, 11	16	8	9	5 - 7 10, 11

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 5.0 V, I_{IN} = - 10 mA or - 20 mA Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CCH}	V_{EEL}	V_{GG}	+ 6.0 V	P. U. T.
t_{TLH}	Rise Time	1.1	3.9	1.0	5.0	1.0	5.0	ns	5, 7, 10, 11	1 - 4 12 - 15	9	8	16	6	1 - 4 12 - 15
t_{THL}	Fall Time	1.1	3.9	1.0	5.0	1.0	5.0	ns	5, 7, 10, 11	1 - 4 12 - 15	9	8	16	6	1 - 4 12 - 15
t_{PHL}	Propagation Delay High to Low	1.0	6.0	1.0	8.0	1.0	8.0	ns	5, 7	1 - 4 10, 11	9, 12 - 15	8	16	6	1 - 4 12 - 15
t_{PLH}	Propagation Delay Low to High	1.0	6.0	1.0	8.0	1.0	8.0	ns	5, 7	1 - 4 10, 11	9, 12 - 15	8	16	6	1 - 4 12 - 15