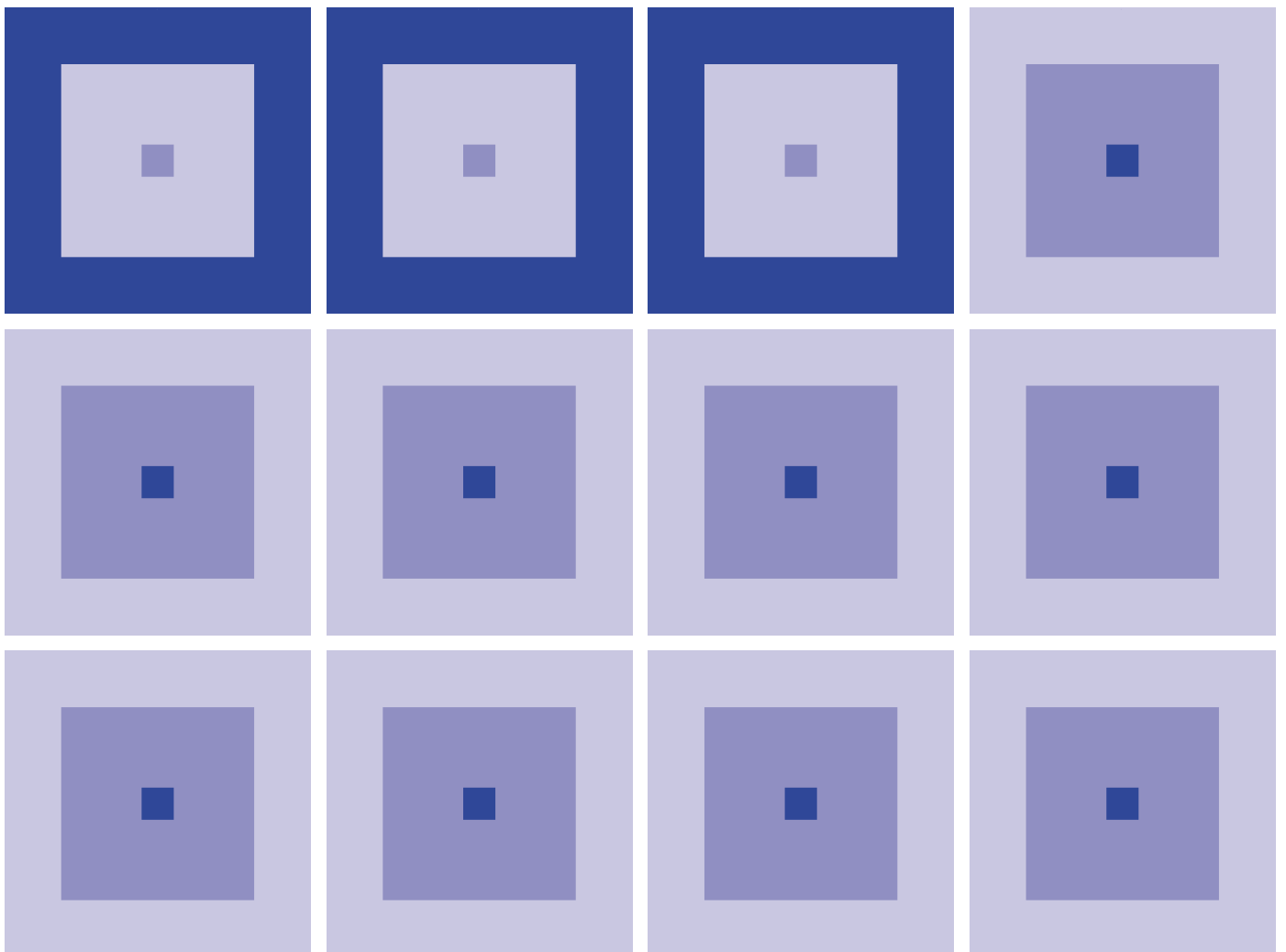


Network Control for Module
S4E10A01001
Technical Manual



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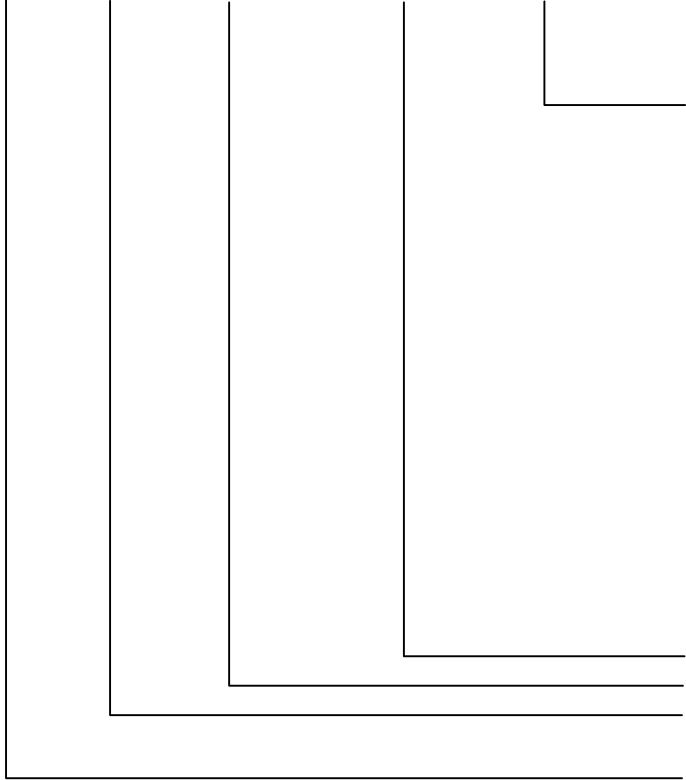
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Configuration of product number

●DEVICES

S4 E 10A01 00100 00



Packing specifications

- 00: Besides tape & reel
- 0A: TCP BL 2 directions
- 0B: Tape & reel Back
- 0C: TCP BR 2 directions
- 0D: TCP BT 2 directions
- 0E: TCP BD 2 directions
- 0F: Tape & reel FRONT
- 0G: TCP BT 4 directions
- 0H: TCP BD 4 directions
- 0J: TCP SL 2 directions
- 0K: TCP SR 2 directions
- 0L: Tape & reel LEFT
- 0M: TCP ST 2 directions
- 0N: TCP SD 2 directions
- 0P: TCP ST 4 directions
- 0Q: TCP SD 4 directions
- 0R: Tape & reel RIGHT
- 99: Specs not fixed

Specifications

Model number

Model name

(E: Assembled product)

Product classification

- S : Semiconductor
- 4 : Micro assembly

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1. BASIC SPECIFICATIONS

S4E10A01001 is a modular product comprised of Ethernet physical layer IC(PHY), EEPROM for storing setting, and various kinds of interface connectors mounted on a miniature board as well as TCP/IP protocol processing-contained network controller for incorporation as key component. This board alone provides network supporting equipment.

Supporting protocols

IP, ICMP, UDP, TCP, ARP, SNMP (MIB II), HTTP, TFTP, and DHCP

Serial Interface

Start-stop synchronous serial

Data transfer rate 1200 to 115.2kbps

The above specifications comply with the S1S60000 specifications.

Interface

GPIO 8 (3.3V output/5V input allowable)

GPIO 8 (3.3V output/3.3V CMOS Schmitt input)

I²C Normal mode(100kHz), Fast mode (400kHz)

Master function (multi-master, 10 bit address-ready, Fast/Normal)

Slave function

Host Interface

Debug Interface

Host Interface

Type 6-type selection

Bus width 8 bits and 16 bits

Endian Selectable between Big and Little

EEPROM

Equivalent to 93C46LV (3.3V, 64×16bit, 3-wire serial Interface)

Area used by system 40 words

Flash ROM

Area accessible by user 1KB

Ethernet

Compliance with IEEE 802.3

Communication rate 10 Base-T/100 Base-TX

Access method CSMA/CD

Supply voltage +3.3V±5%

Current Consumption 300mA Max. (main body only)

1.1 Block Diagram

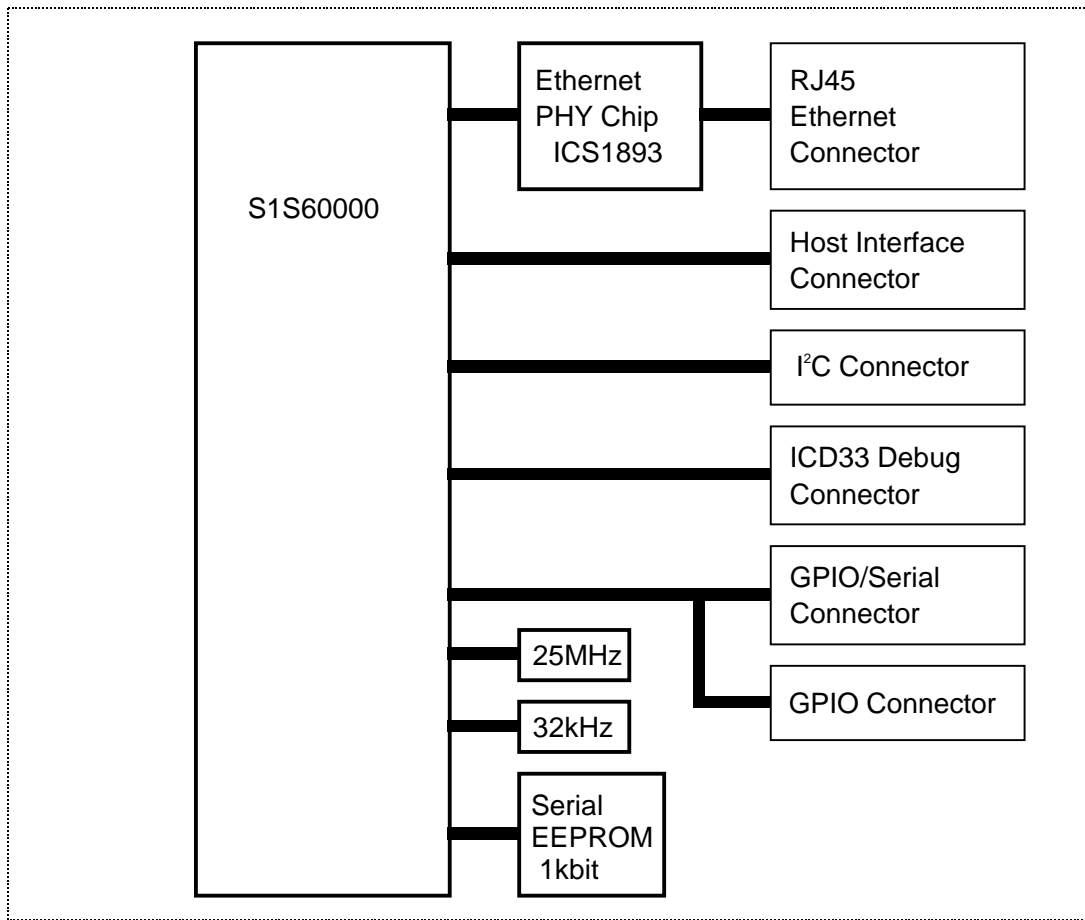


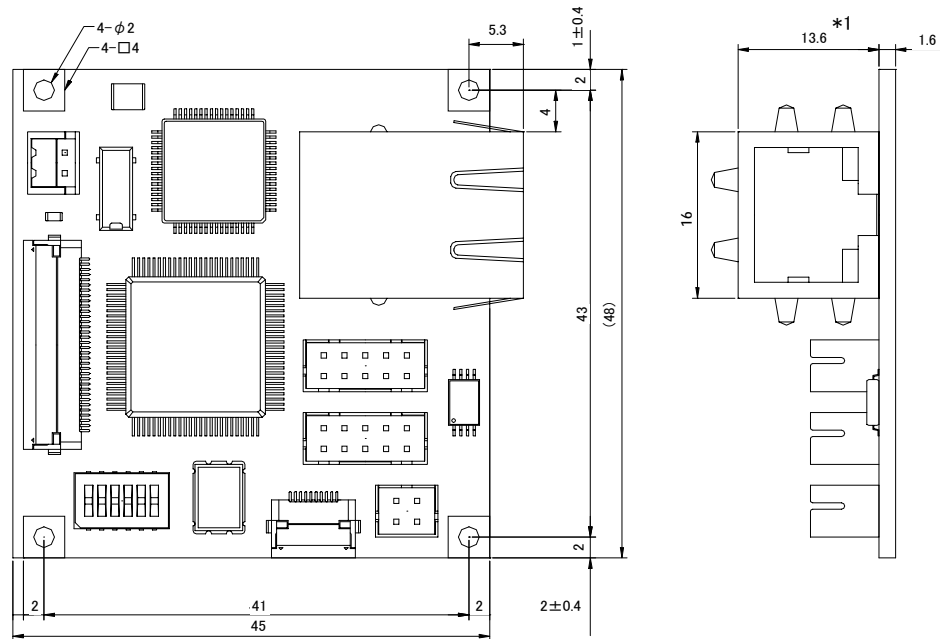
Fig.1.1 S4E10A01001 Block Diagram

2. MECHANICAL SPECIFICATIONS

2.1 Outer Dimensions

Main body: 48(W) × 45(D) × 13.6(H :component surface) mm (excluding protrusions)

Board: FR-4 t=1.6mm, 4 layers



Unit:mm

*1: Protrusions are excluded.

Fig.2.1 S4E10A01001 Outline Dimensional Drawing

2.2 Weight

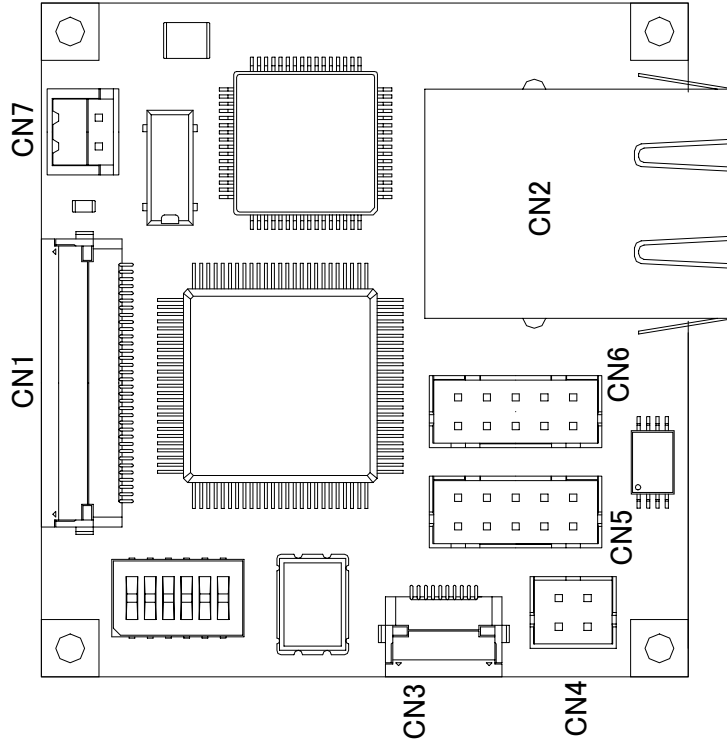
Approximately 18g

2.3 Connector

Mate/demate cycles are according to the value guaranteed on the connector.

3. PIN LAYOUT

3.1 Interface Connector Layout



3.2 Host Interface Connector (CN1)

Hirose Electric Co., Ltd.'s (HRS) FH12-34S-0.5SH or its equivalent is used.

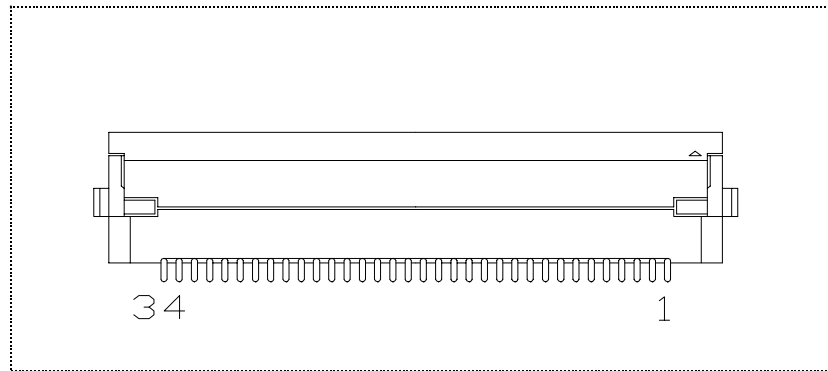


Fig.3.1 Number of Pins on Host Interface Connector

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	GND	10	HD1	19	HD9	28	HRD1#
2	RESET#	11	HD2	20	HD10	29	HWR0#
3	HCS#	12	HD3	21	HD11	30	HWR1#
4	GND	13	HD4	22	HD12	31	HINT
5	HA0	14	HD5	23	HD13	32	Reserved
6	HA1	15	HD6	24	HD14	33	Reserved
7	HA2	16	HD7	25	HD15	34	GND
8	GND	17	GND	26	GND	—	—
9	HD0	18	HD8	27	HRD0#	—	—

3.3 Ethernet Connector (CN2)

Pulse Engineering Inc.'s J0026D21B or its equivalent is used. This connector contains a pulse transformer.

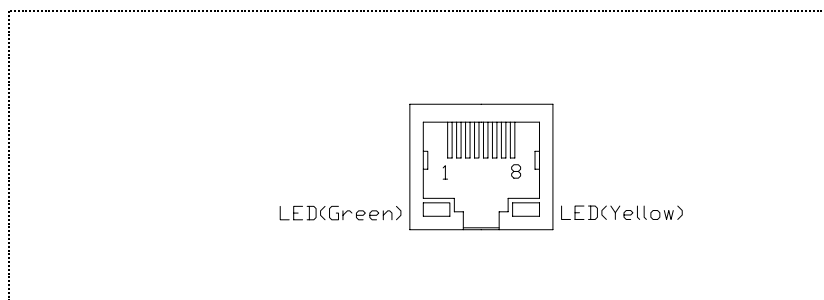


Fig.3.2 Number of Pins on Ethernet Connector

Pin	Signal name	Pin	Signal name
1	TXP	5	Reserved (*1)
2	TXN	6	RXN
3	RXP	7	Reserved (*1)
4	Reserved (*1)	8	Reserved (*1)

*1: This pin is connected inside the connector. For further information, see connector specification.

3.4 Debugging Connector (CN3)

Hirose Electric Co., Ltd.'s (HRS) FH12-10S-0.5SH or its equivalent is used.

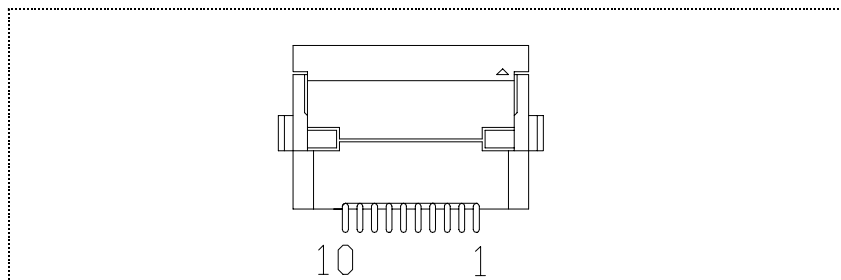


Fig.3.3 Number of Pins on Debugging Connector

Pin	Signal name	Pin	Signal name
1	DCLK	6	GND
2	GND	7	DST1
3	DSIO	8	GND
4	GND	9	DST0
5	DST2	10	DPCO

3.5 I²C Connector (CN4)

Hirose Electric Co., Ltd.'s (HRS) DF11-4DP-2DSA or its equivalent is used. For compatible connector on the receiving side, be sure to use DF11-4DS-2C or its equivalent.

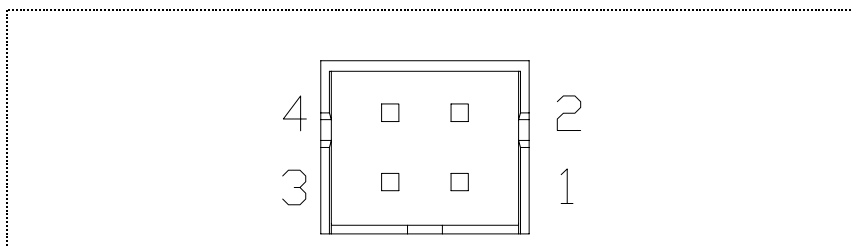


Fig.3.4 Number of Pins on I²C Connector

Pin	Signal name
1	SDA
2	SCL
3	GND
4	+3.3V

3.6 GPIO/Serial Interface Connector (CN5)

Hirose Electric Co., Ltd.'s (HRS) DF11-10DP-2DSA or its equivalent is used. For compatible connector on the receiving side, be sure to use DF11-10DS-2C or its equivalent.

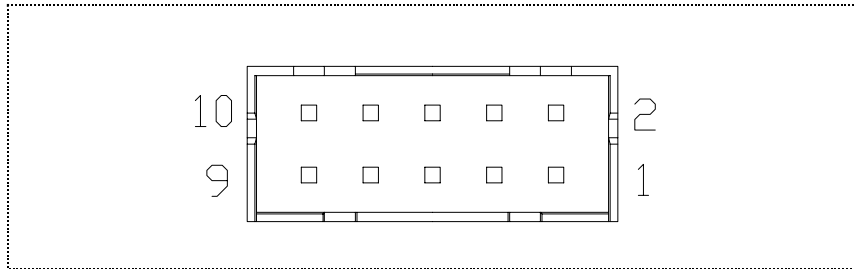


Fig.3.5 Number of Pins on GPIO/Serial Interface Connector

Pin	Signal name	Pin	Signal name
1	GPIO8/RXD	6	GPIO13/DSR#
2	GPIO9/TXD	7	GPIO14/RTS#
3	GPIO10/MODE	8	GPIO15/DTR#
4	GPIO11/RSV1	9	GND
5	GPIO12/CTS#	10	+3.3V

3.7 GPIO Interface Connector (CN6)

DF11-10DP-2DSA of Hirose Electric Co., Ltd. (HRS) or its equivalent is used. For compatible connector on the receiving side, be sure to use DF11-10DS-2C or its equivalent.

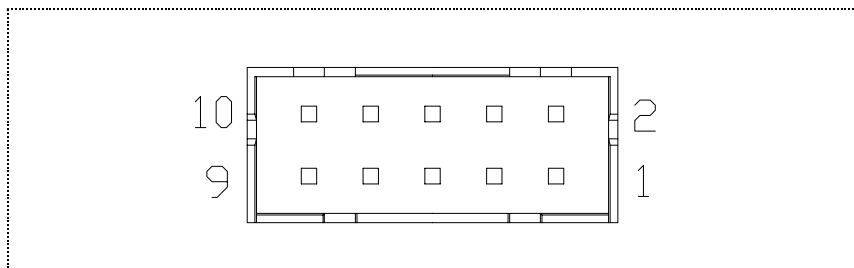


Fig.3.6 Number of Pins on GPIO Interface Connector

Pin	Signal name	Pin	Signal name
1	GPIO0/INT0	6	GPIO5
2	GPIO1	7	GPIO6
3	GPIO2/CRS	8	GPIO7/OSCCTL
4	GPIO3	9	GND
5	GPIO4	10	+3.3V

3.8 Power Connector (CN7)

Hirose Electric Co., Ltd.'s (HRS) DF3A-2P-2DSA or its equivalent is used. For compatible connector on the receiving side, be sure to use DF3-2S-2C or its equivalent.

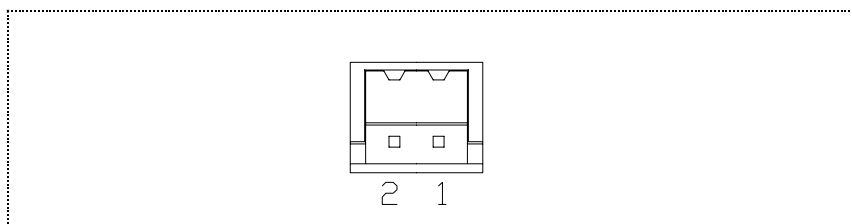


Fig.3.7 Number of Pins on Power Connector

Pin	Signal name
1	+3.3V
2	GND

4. PIN FUNCTIONS

Following is a brief description of pin functions with regard to respective interfaces.

Symbols in the “Type” Column are as follows:

I	-	Input pin
O	-	Output pin
O OD	-	Output pin (open drain pin)
Tri	-	Output pin (3-state output)
I/O	-	Input/output pin
I/O OD	-	Input/output pin (open drain output)

Host interface (CN1)

Pin name	Pin No.	Type	Function
RESET#	2	I	A LOW-level input causes this module to be reset. This pin contains a pull up resistor.
HCS#	3	I	A host interface access control signal. During LOW conditions of this signal, access to the host interface can be made. This pin contains a pull up resistor that allows 5 V input.
HA[2:0]	5,6,7	I	A host interface port selection signal. Selects a port to which access is made during HCS# = LOW conditions. Selectable ports are as follows: 00x: Command port (write)/status port (read) 01x: Data port (write/read) 1xx: Flag port (read only) This pin contains a pull up resistor that allows 5 V input. ※ The HA0 is used for selecting between HIGH and LOW order byte at 8-bit interface. It becomes invalid at 16-bit interface.
HD[15:0]	9 to 16 18 to 25	I/O	Host interface data signal line. At 8-bit interface only HDATA[7:0] is valid. The HDATA[15:8] is not driven and it goes into HIGH state. This pin contains a pull up resistor that allows 5 V input. The output is 3.3 V CMOS.
HRD0#	27	I	A host interface R/W control signal. The function varies with host interface types. This pin contains a pull up resistor that allows 5 V input.
HRD1#	28	I	
HWR0#	29	I	
HWR1#	30	I	
HINT	31	I	Interrupt line for host interface. Determine the factors responsible for interrupt by the contents of flag port. The polarity of interrupt can be changed depending on the HINTPOL conditions at the time of reset. Since this signal is a 3.3 V/3-state output signal, externally connect a pull up resistor at HINTPOL = 0 or a pull down resistor at HINTPOL = 1.
Reserved	32,33	—	Leave this unconnected as it is likely to be used for other equipment in the years ahead.
GND	1,4,8,17,26,34	—	Ground (0V)

Ethernet (CN2)

Signal name	Pin No.	Type	Function
TXP	1	O	Twisted pair on the sending side (+)
TXN	2	O	Twisted pair on the sending side (-)
RXP	3	I	Twisted pair on the receiving side (+)
RXN	6	I	Twisted pair on the receiving side (-)
Reserved	4,5,7,8	—	Connected inside the connector.

Debug (ICD) (CN3)

Signal name	Pin No.	Type	Function
DCLK	1	O	These pins are used for communication with the ICD33 debug tool. The ICD33 tool is primarily used to rewrite Flash memories in S1S60000. In normal times, do not connect any.
DSIO	3	I/O	
DST[2:0]	5,7,9	O	
DPCO	10	O	
GND	2,4,6,8	—	Ground (0V)

I²C (CN4)

Signal name	Pin No.	Type	Function
SDA	1	I/O	I ² C bus data input/output pins. A bidirectional signal for data input/output and ACK input/output.
SCL	2	I/O	I ² C bus serial clock pins. For master setting, it goes in the state of output or for slave setting, it goes in that of input.
GND	3	—	Ground (0V)
+3.3V	4	—	Supply pin

GPIO/serial (CN5)

Signal name	Pin No.	Type	Function
GPIO8/RXD	1	I/O	General-purpose input/output pins. Designed specifically for 3.3V CMOS level and Schmitt input. Setting the GENCR resistor to the SERCONF bit makes it a start-stop synchronous serial pin. For further information, see “S1S60000 Technical Manual.” After resetting hardware, all of them are set to input.
GPIO9/TXD	2	I/O	
GPIO10/MODE	3	I/O	
GPIO11/RSV1	4	I/O	
GPIO12/CTS#	5	I/O	
GPIO13/DSR#	6	I/O	
GPIO14/RTS#	7	I/O	
GPIO15/DTR#	8	I/O	
GND	9	—	Ground (0V)
+3.3V	10	—	Supply pin

GPIO(CN6)

Signal name	Pin No.	Type	Function
GPIO0/INT0	1	I/O	General-purpose input/output pins. 5 V input is allowed. The GPIO0 is used as interrupt pin, which is capable of sending a notice of interrupt to a pre-determined destination. The GPIO2 is used as CRS input pin when a half-duplex communication is carried out. The GPIO7 can be used as OSC control pin in sleep mode. For further information, see "S1S60000 Technical Manual." After resetting hardware, all of them are set to input.
GPIO1	2	I/O	
GPIO2/CRS	3	I/O	
GPIO3	4	I/O	
GPIO4	5	I/O	
GPIO5	6	I/O	
GPIO6	7	I/O	
GPIO7/OSCCTL	8	I/O	
GND	9	—	Ground (0V)
+3.3V	10	—	Supply pin

Power supply (CN7)

Signal name	Pin No.	Type	Function
+3.3V	1	—	A supply for this module. Supply power of approximately +3.3V±5%, 300 mA.
GND	2	—	Ground (0V)

5. FUNCTIONAL DESCRIPTION

This chapter provides description of basic functions of S4E10A01001.

5.1 Host Interface

The host interface is an 8-bit or 16-bit parallel interface used to connect the S4E10A01001 with the external MPU. Following settings are available by selecting a DIP switch (SW1) on the board.

Table 5.1 DIP Switch (SW1) Setting

SW	Description of setting	Detail
6	Bus width setting	ON : 16-bit bus OFF: 8-bit bus
5	Endian setting	ON : Little endian OFF: Big endian
4	Polarity of interrupt signal	ON : LOW Active OFF: HIGH Active
3	Host interface type	3 : 2 : 1
		ON : ON : ON Type0 SH-3/4
		ON : ON : OFF Type1 MC68000
2		ON : OFF: ON Type2 MC68030,MC68040
	ON : OFF: OFF Type3 Generic	
	OFF: ON : ON Reserved	
1	OFF: ON : OFF Type5 MIPS,ISA	
	OFF: OFF: ON Type6 PCMCIA	
	OFF: OFF: OFF EEPROM setting	

For further information on host interface type, see “S1S60000 Technical Manual.” The SW1, 4, 5 and 6 are factory-set to ON.

Example of connection

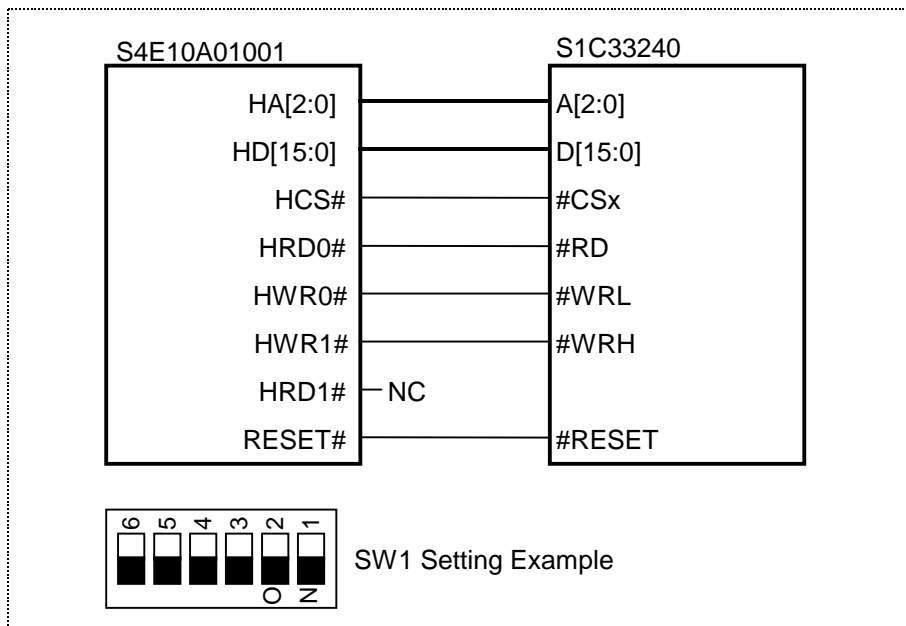


Fig.5.1 Host Interface Example

5.2 I²C

The I²C is an inter IC bus developed by Philips Company Ltd. The S1S60000 on this board incorporates I²C master/slave functions and has the following features:

Master/slave send/receive

Bus arbitration function

Clock synchronization function

Restart generation function

Bus error detection function

Programmable noise cancel function

10-bit/7-bit master/slave addressing function

Supports standard mode (Max.100 Kbps)/HIGH-speed mode (Max.400 Kbps).

Supports multiple masters.

Example of connection

Fig.5.2 shows an example of circuit of I²C interface. Since a pull up resistor is included in this board, external data input/output and pull up to clock signal are not required.

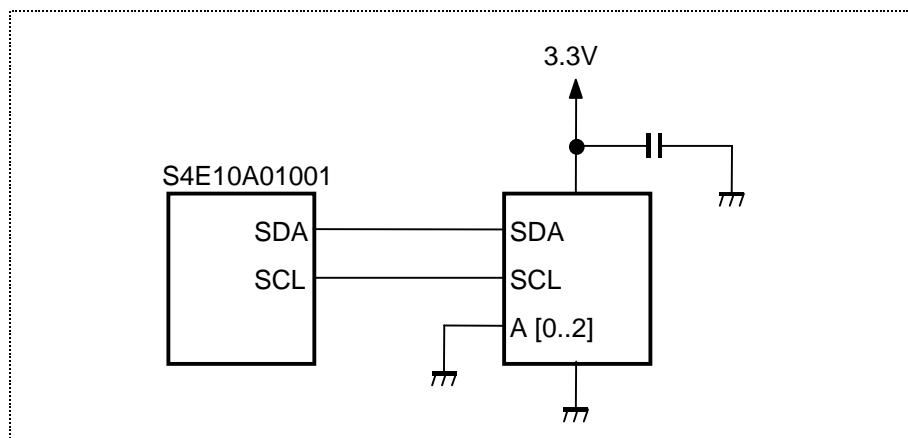


Fig.5.2 I²C Interface Example

5.3 GPIO

Each of 16 GPIO pins of GPIO[7:0] and GPIO[15:8] on this board can be independently operated. Special functions other than GPIO are assigned to some pins. The switching is done with setting the resistor built into S1S60000.

For further information on GPIO, see “S1S60000 Technical Manual.”

Example of connection

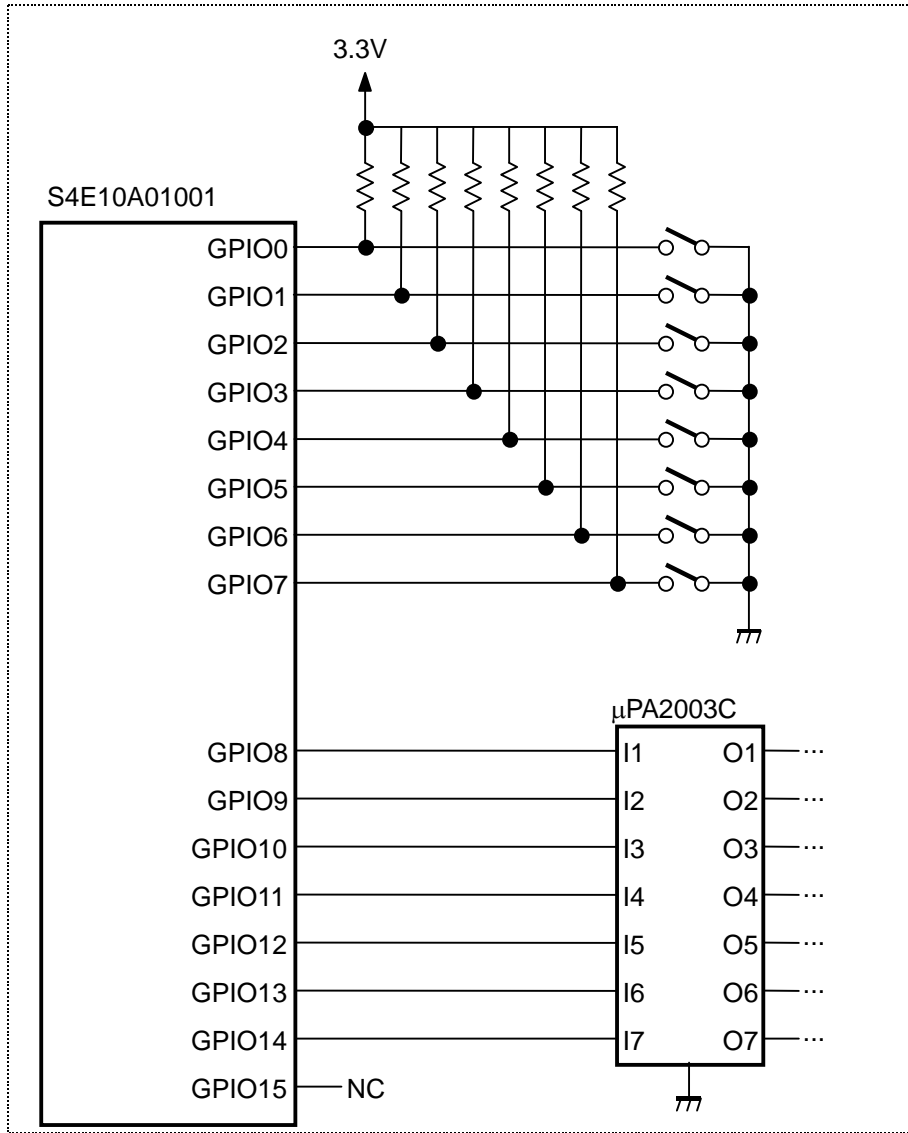


Fig.5.3 GPIO Interface Example

5.4 Serial Interface

When all of SW1, 2 and 3 DIP switch (SW1) are set to OFF, the GPIO[15:8] becomes serial interface pin by the setting of EEPROM. At this moment, the GPIO10 signal level causes a changeover to hardware control mode and serial emulation mode. The switching of the GPIO[15:8] function is basically done with the setting of the GPALT[15:8] resistor built into S1S60000. For further information on serial interface, see “S1C33240 Technical Manual.”

5.4.1 Hardware Control Mode

Setting the GPIO10 to HIGH puts into hardware control mode via serial interface. At this time, communication conditions are fixed as follows:

Start-stop synchronous serial, 9600 bps, 8-bit data, 1 STOP bit, no parity and no flow control.

Following shows an example of connection in hardware control mode:

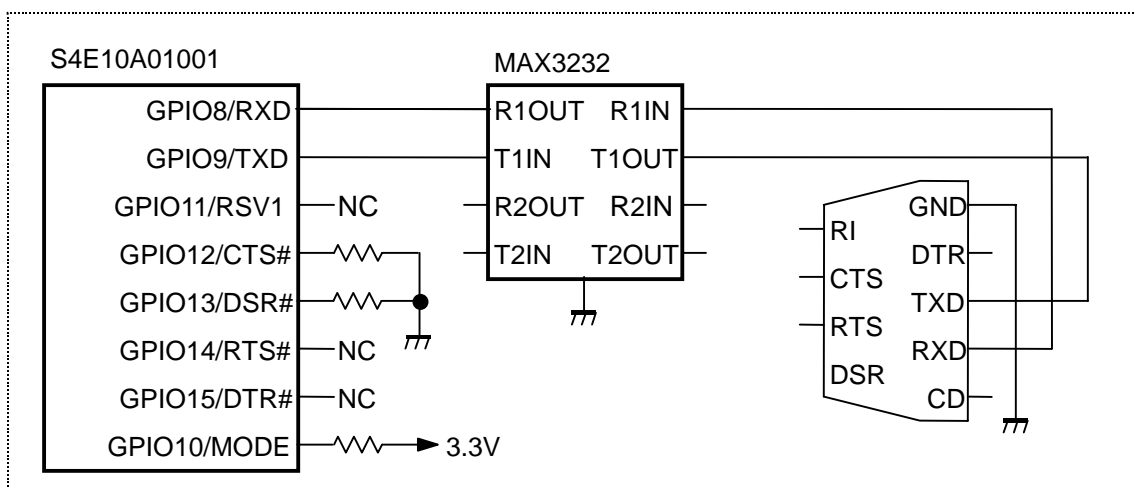


Fig.5.4 Serial Interface Hardware Control Mode Example

5.4.2 Serial Emulation Mode

Setting GPIO10 to LOW and the GENCR resistor at SERCONF(bit[10:8]) = 010 puts into serial emulation mode. Serial send/receive data can be sent/received via predetermined destination and network. This setting is valid when data of the equipment with the RS232 interface is sent/received to/from other equipment on the Ethernet. Functions of respective pins in this mode are as shown in the following table:

Table 5.2 Pin Function at Start-Stop Synchronous Serial Setting

Pin	Pin No.	Name	In/Out	Function
GPIO15	1	DTR#	O	Data Terminal Ready Display of receive-enabled state LOW active signal
GPIO14	2	RTS#	O	Request to Send Display of send-enabled state LOW active signal
GPIO13	3	DSR#	I	Data Set Ready Input of external send-enabled state LOW active signal When this signal is in LOW state and it is not ready to receive, the S1S60000 places DTR# in an inactive state.
GPIO12	4	CTS#	I	Clear to Send Input of external receive-enabled state LOW active signal When this pin is in a HIGH state, sending is temporarily stopped. When it changes state into LOW, sending is resumed. Due to software control by interrupt, the time between stop and resumption is inconstant after the signal change. Control the control side by allowing for adequate margin of buffer capacity.
GPIO11	5	RSV1	—	Reserved This pin is reserved for future extension.
GPIO10	6	MODE	I	Mode Select The switching between normal mode and hardware control mode is done. In normal mode, set to LOW.
GPIO9	7	TXD	O	Transmit Data Serial send data
GPIO8	8	RXD	I	Receive Data Serial receive data

For further information on this mode, see “Section 5. Hardware Control” in “S1S60000 Technical Manual.” Following shows an example of connection in serial emulation mode:

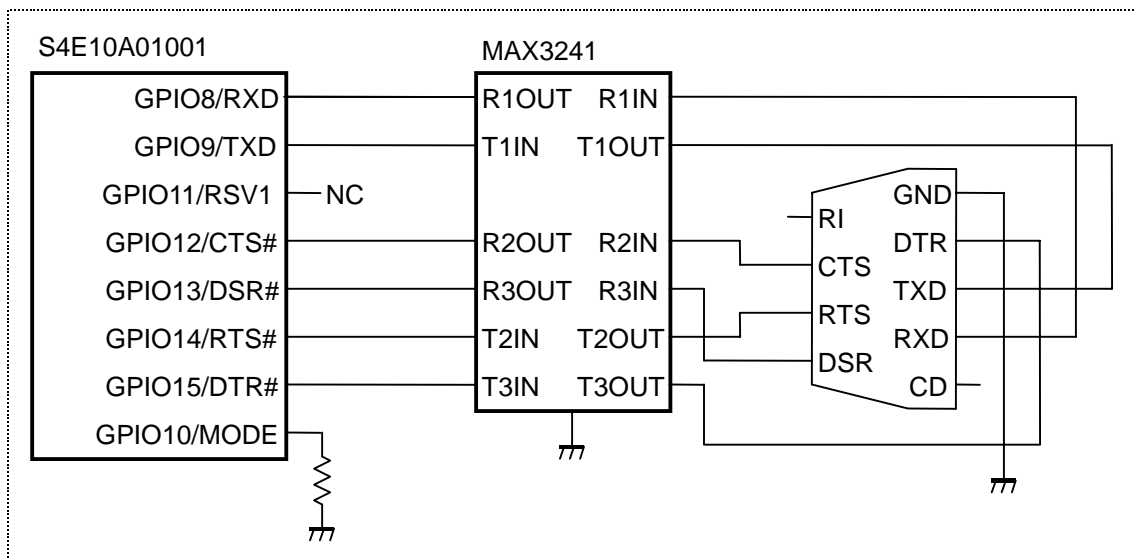


Fig.5.5 Serial Interface Emulation Mode Example

5.5 Debugging Connector

Connector for connecting the ICD33 in-circuit debugger for the EPSON S1C33 family. These pins are used for communication with the ICD33 debugging tool. The ICD33 tool is primarily used to rewrite Flash memories in S1S60000. In normal times, do not connect any.

5.6 EEPROM

Each data of EEPROM has a width of 16 bits. Table 5.3 shows data map. Data from index 01h to 27h is set in the appropriate internal resistor in S1S60000 after resetting.

Table 5.3 EEPROM Data Map

Index	Data	Set value	Contents
00h	ID	E0C3h	0xE0C3 fixed
01h	MAC0	0000h	MAC resistor initial value EPSON's organizationally unique identifier (OUI) is 00-00-48. The address varying with modules is written in the "xx" section.
02h	MAC1	xx48h	
03h	MAC2	xxxxh	
04h	GENCR	0310h	GENCR resistor set value
05h	HIFCR	0700h	HIFCR resistor set value
06h	I2CSADR	0030h	I2CSADR resistor set value
07h	I2CCONF	0235h	I2CCONF resistor set value
08h	GPALT	FF84h	GPALT resistor set value
09h	GPCFG	0000h	GPCFG resistor set value
0Ah	GPDAT	0000h	GPDAT resistor set value
0Bh	GPMSK	0000h	GPMSK resistor set value
0Ch	EPMSK	0000h	EPMSK resistor set value
0Dh	I2CMSK	0000h	I2CMSK resistor set value
0Eh	PMWAIT	000Fh	PMWAIT resistor set value
0Fh	PHYMODE	0200h	PHYMODE resistor set value
10h	ANEGR	10EFh	ANEGR resistor set value
11h	IPADRH	A8C0h	IP Address: Intra-office IP address initial value 192.168.0.254
12h	IPADRL	FE00h	
13h	SNMSKH	FFFFh	Subnet Mask: Subnet mask initial value 255.255.255.0
14h	SNMSKL	00FFh	
15h	DGWH	A8C0h	Default Gateway: Default gateway initial value 192.168.0.1
16h	DGWL	0100h	
17h	DADR0H	A8C0h	Destination IP Address 0: Destination address setting 0 192.168.0.2
18h	DADR0L	0200h	
19h	DADR1H	A8C0h	Destination IP Address 1: Destination address setting 1 192.168.0.3
1Ah	DADR1L	0300h	
1Bh	DADR2H	A8C0h	Destination IP Address 2: Destination address setting 2 192.168.0.4
1Ch	DADR2L	0400h	
1Dh	DADR3H	A8C0h	Destination IP Address 3: Destination address setting 3 192.168.0.5
1Eh	DADR3L	0500h	
1Fh	PORT	00C0h	PORT resistor set value
20h	DPORT	01C0h	DPORT resistor set value
21h	SERMODE	00E1h	SERMODE resistor set value
22h	TMOUT	4000h	TMOUT resistor set value
23h	SOPAR	0070h	SOPAR resistor set value
24h	COMN0	7570h	Set values of COMN0, COMN1, COMN2, COMN3 resistors. They hold community names that can be set in the SNMP agent. The default community name of the SNMP agent is "public" regardless of values in internal resistors
25h	COMN1	6C62h	
26h	COMN2	6369h	
27h	COMN3	0000h	

[Note 1] Access to the area from 00h to 0Fh for writing from network is inhibited at all times. Rewrite this area from other than network (host interface or I²C interface).

[Note 2] The EEPROM data can be rewritten from the Ethernet, host interface or serial interface.

6. SPECIFICATIONS

Environmental Condition

Ambient operating temperature	0 to 40°C
Ambient operating humidity	5 to 95% (Non-condensing)
Storage temperature	-40 to +70° C
Storage humidity	5 to 90% (Non-condensing)
Electrostatic withstand voltage	±2.0kV (contact discharge) ±8.0kV (aerial discharge) (IEC 61000-4-2,CISPR 24)

Weight

Approximately 18g

Power supply

Supply voltage	+3.3±5%
Maximum input current	300mA (when each connector is not connected)

Board

FR - 4 t=1.6mm, 4 layer

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

(V_{SS} = 0V)

Item	Symbol	Conditions	Ratings	Unit	Notes
Supply voltage	V _{DD}		-0.3 to +3.6	V	
Input voltage	V _I	Exclusive of fail safe pins (*1)	-0.3 to V _{DD} +0.5	V	
		Fail safe pins (*1)	-0.3 to +7.0	V	

*1:Fail safe pins = HCS#,HA[2:0], HD[15:0], HRD0#, HRD1#,HWR0#, HWR1#, and GPIO[7:0]

7.2 Recommended Operating Conditions

(V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Supply voltage	V _{DD}		3.14	—	3.47	V	
Input voltage	V _I	Exclusive of fail safe pins (*1)	V _{SS}	—	V _{DD}	V	
		Fail safe pins (*1)	V _{SS}	—	5.5	V	1

*1:Fail safe pins = HCS#,HA[2:0], HD[15:0], HRD0#, HRD1#,HWR0#, HWR1#, and GPIO[7:0]

Note 1: The voltage exceeding the output voltage must not be externally applied to fail safe pins at the time of HIGH level output.

7.3 DC Characteristics

(Unless otherwise specified: V_{DD} = 3.14V to 3.47V, T_a = 0°C to 40°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Input leak current	I _{LI}		-1	—	1	μA	
HIGH level output voltage	V _{OH}	I _{OH} =-2mA, V _{DD} =Min.	V _{DD} -0.4	—	—	V	
LOW level output voltage	V _{OL}	I _{OL} =2mA, V _{DD} =Min.	—	—	0.4	V	
HIGH level input voltage	V _{IH}	CMOS level, V _{DD} =Max.	2.4	—	—	V	
LOW level input voltage	V _{IL}	CMOS level, V _{DD} =Min.	—	—	0.4	V	
Positive trigger input voltage	V _{T+}	CMOS Schmitt, V _{DD} =Max.	1.1	—	2.4	V	
Negative trigger input voltage	V _{T-}	CMOS Schmitt, V _{DD} =Min.	0.6	—	1.8	V	
Hysteresis voltage	V _H	CMOS Schmitt	0.1	—	—	V	
Input pin capacity	C _I	f=1MHz, V _{DD} =0V	—	—	10	pF	
Output pin capacity	C _O	f=1MHz, V _{DD} =0V	—	—	10	pF	
Input/output pin capacity	C _{IO}	f=1MHz, V _{DD} =0V	—	—	10	pF	

7.4 Current Consumption

(Unless otherwise specified: V_{DD} = 3.14V to 3.47V, T_a = 0°C to 40°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Operating Current	I _{DD1}	f _{CPU} =50MHz, 10Base-T operation	—	—	220	mA	
		f _{CPU} =50MHz, 100Base-TX operation	—	—	190	mA	
In power save mode	I _{DD2}	f _{CPU} =12.5MHz, 10Base-T operation	—	—	130	mA	1
In sleep mode	I _{DD3}	f _{CPU} =32.768kHz	—	—	4.2	mA	

Note 1: 100 Base-TX communication is disabled in power save mode.

8. AC CHARACTERISTICS

8.1 Legend

t_{CYC}: bus clock cycle time: 20ns

8.2 AC Characteristics Measuring Conditions

Signal test level:

Input signal	HIGH level	$V_{IH}=V_{DD}-0.4V$
	LOW level	$V_{IL}=0.4V$
Output signal	HIGH level	$V_{OH}=1/2 V_{DD}$
	LOW level	$V_{OL}=1/2 V_{DD}$

Input signal waveform: Rise (10% → 90% V_{DD}) 5ns
 Fall (90% → 10% V_{DD}) 5ns

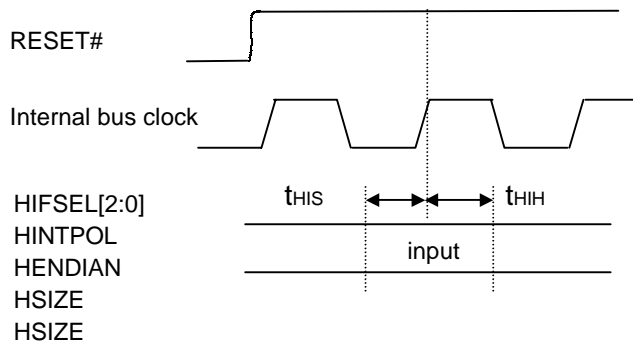
Output load capacity: C_L=50pF

8.3 AC Characteristics Table

Reset input characteristics

(Unless otherwise specified: V_{DD} = 3.14 to 3.47V, V_{SS} = 0V, Ta = 0 to 40°C)

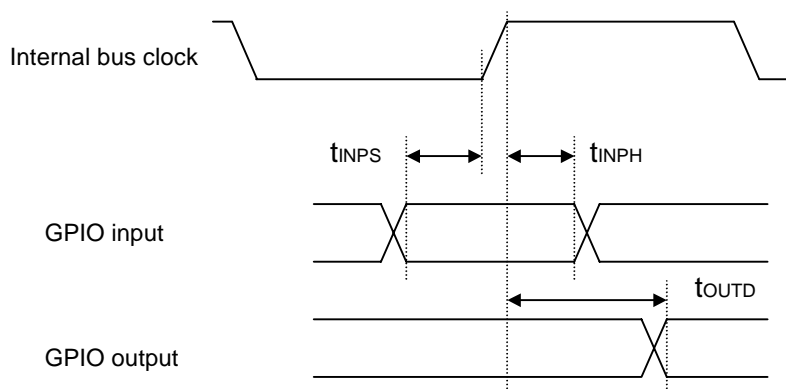
Item	Symbol	Min.	Max.	Unit	Notes
Minimum reset pulse width	t _{RST}	6 t _{CYC}	—	ns	
Set input data set-up time	t _{HIS}	20	—	ns	
Set input data hold time	t _{HIH}	10	—	ns	



Input, output, and input/output dual-purpose port (GPIO)

(Unless otherwise specified: V_{DD} = 3.14 to 3.47V, V_{SS} = 0V, Ta = 0 to 40°C)

Item	Symbol	Min.	Max.	Unit	Notes
Input data set-up time	t _{INPS}	20	—	ns	
Input data hold time	t _{INPH}	10	—	ns	
Output data delay time	t _{OUTD}	—	20	ns	

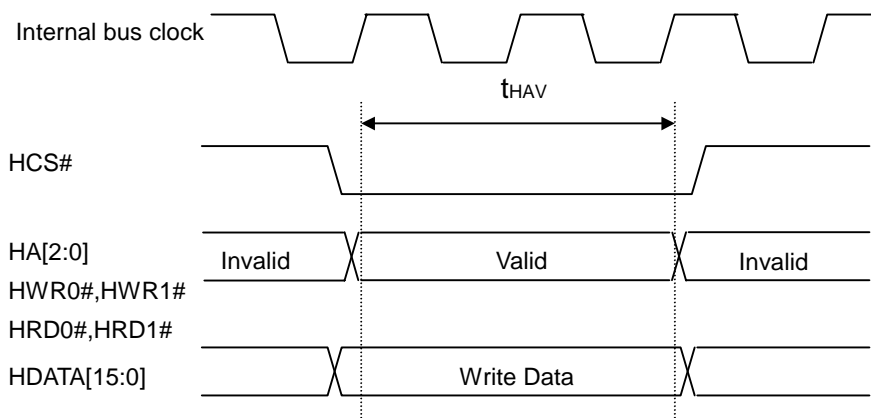


Host Interface

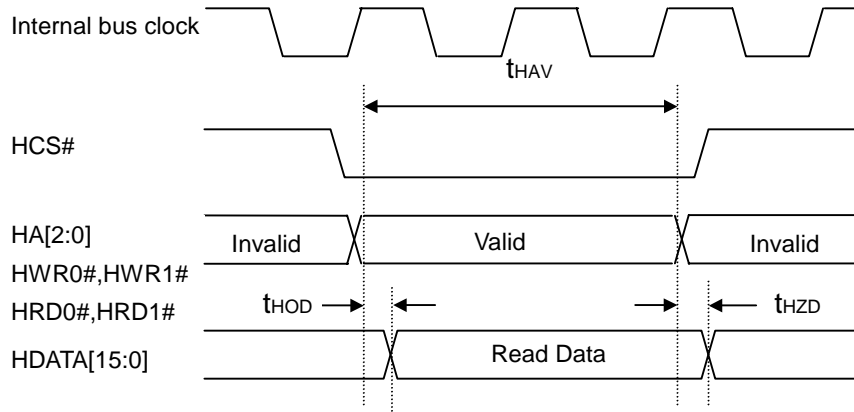
(Unless otherwise specified: $V_{DD} = 3.14$ to $3.47V$, $V_{SS} = 0V$, $T_a = 0$ to $40^{\circ}C$)

Item	Symbol	Min.	Max.	Unit	Notes
Host interface access available period (HCS#,HA[2:0],HWR0#,HWR1#, HRD0#,HRD1#)	t_{HAV}	$2t_{CYC}+10$	—	ns	
Host interface output data delay time	t_{HOD}	—	25	ns	
Host interface output floating delay time	t_{HZD}	—	25	ns	
Host interface interrupt output delay time	t_{HIOD}	—	20	ns	
Host interface interrupt floating delay time	t_{HIZD}	—	20	ns	
Host interface set input set-up time	t_{HIS}	10	—	ns	
Host interface set input hold time	t_{HID}	10	—	ns	

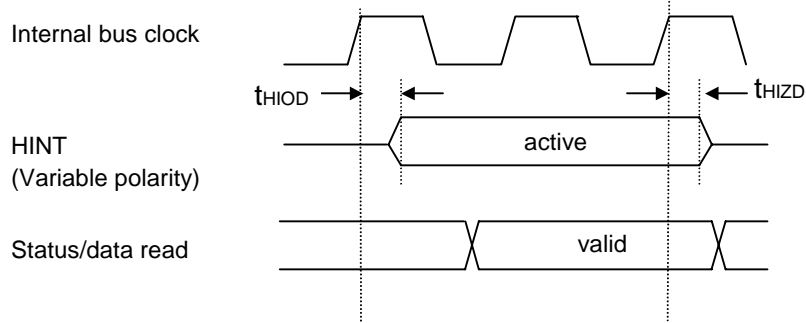
Host Interface (Write)



Host interface (Read)



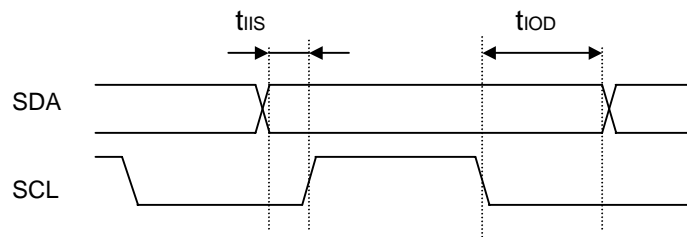
Host interface (Control line)



I²C bus

(Unless otherwise specified: V_{DD} = 3.14 to 3.47V, V_{SS} = 0V, T_a = 0 to 40°C)

Item	Symbol	Min.	Max.	Unit	Notes
SDA data set-up time	t _{IIS}	5	—	ns	
SDA output delay time	t _{IOD}	5t _{CYC}	—	ns	



9. DIRECTIONS FOR USE

Supply $+3.3V \pm 5\%$ power

Insert the FFC connector with the upper brown part open upward to fix in a closed position.

When detaching or attaching FFC from or to the FFC connector, great care should be taken not to damage the connector.

Connect or disconnect the Ethernet cable during power-down.

When power to this module is turned on again, be sure to wait for 5 seconds or longer after powering it off.

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