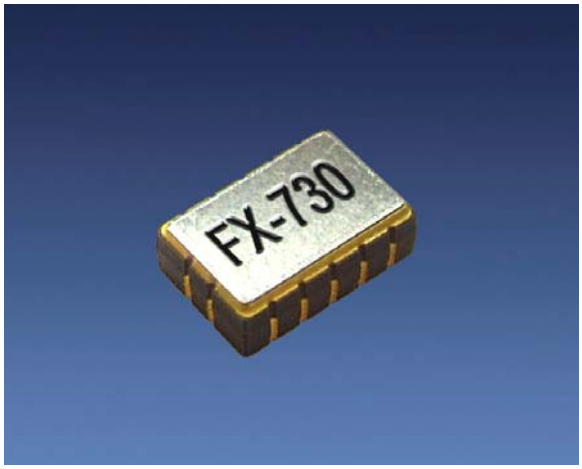
FX-730
Low Jitter VCSO Frequency Translator



Features

- 5 x 7.5 x 2.5 mm Package
- Frequency Translation up to 850 MHz
- VCSO based PLL for Ultra-Low Jitter
- CMOS / LVDS / LVPECL Inputs compatible
- Differential LVPECL or LVDS Output
- CMOS Lock Detect
- External Divider for Input Frequencies < 19 MHz
- 0°/70°C or -40°/+85°C Temperature Range
- Fully Compatible for Lead Free Assembly

Description

The FX-730 is a low jitter precision frequency translator used to translate input frequencies such as 19.44, 38.88, 77.76 MHz, etc. to a binary multiple frequency as high as 850 MHz. The FX-730's superior jitter performance is achieved through the PLL's integrated VCSO. The FX-730 is housed in a hermetically sealed leadless surface mount package offered on tape and reel.

Applications

Description	Standard
1-2-4 Gigabit FC	INCITS 352-2002
10 Gigabit FC	INCITS 364-2003
10GbE LAN / WAN	IEEE 802.3ae
OC-192	ITU-T G.709
SONET / SDH	GR-253-CORE Issue 3
FEC (Forward Error Correction) Scaling	

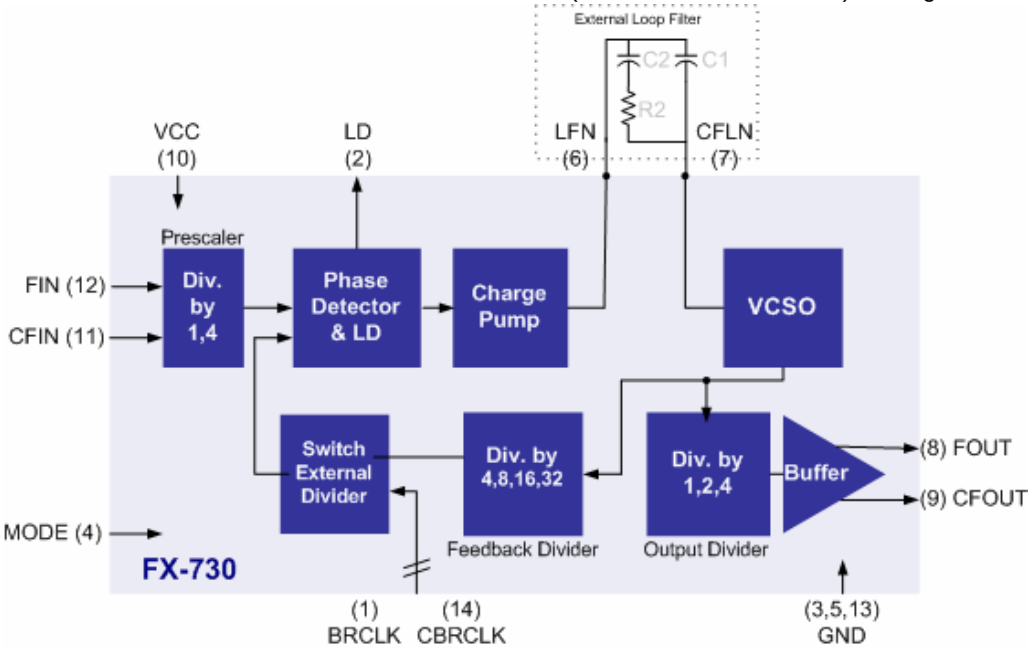


Table 1. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Input Frequency	F_{IN}	19.44		850	MHz	1,2,3
Capture Range (*ordering option*)	APR	±32 or ±50			ppm	1,2,3
Output Frequency	F_{OUT}	125		850	MHz	1,2,3
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}			100	mA	3
LVCMOS Input						
Input High Voltage	V_{IH}	2		V_{CC}	V	2,3
Input Low Voltage	V_{IL}	0		0.8	V	
LVPECL Input						
Input High Voltage	V_{IH}	1.49		2.72	V	2,3
Input Low Voltage	V_{IL}	0.86		2.125	V	2,3
Lock Detect Output						
Output High Voltage	V_{OH}	0.9*V_{CC}			V	
Logic Low Voltage	V_{OL}			0.1*V_{CC}	V	
Outputs						
Mid Level - LVPECL		V_{CC}-1.4	V_{CC}-1.25	V_{CC}-1.0	V	2,3
Swing - LVPECL		450	600	950	mV-pp	2,3
Mid Level - LVDS		V_{CC}-2.0	V_{CC}-1.6	V_{CC}-1.3	V	2,3
Swing - LVDS		250	410	450	mV-pp	2,3
Current	I_{OUT}			20	mA	5
Rise Time	t_R			400	ps	4,5
Fall Time	t_F			400	ps	4,5
Symmetry	SYM	45	50	55	%	2,3
Jitter Generation - 155.52 to 622.08 MHz						
(12 kHz – 20 MHz BW)	Φ_J		0.21	0.5	ps-rms	5
(50 kHz – 80 MHz BW)	Φ_J		0.12	0.4	ps-rms	5
Operating Temp. (Ordering Option)	T_{OP}	0/70, -40/85			°C	1,3

1. See Standard Frequencies and Ordering Information.
2. Parameters are tested with production test circuit below (Fig 1).
3. Parameters are tested at ambient temperature with test limits guard banded for specified operating temperature.
4. Measured from 20% to 80% of a full output swing (Fig 2).
5. Not tested in production, guaranteed by design, verified at qualification.

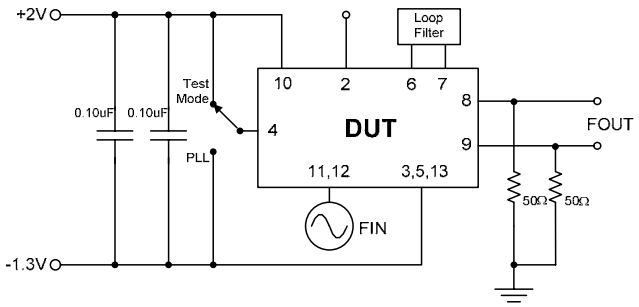


Figure 1. LVPECL Test Circuit

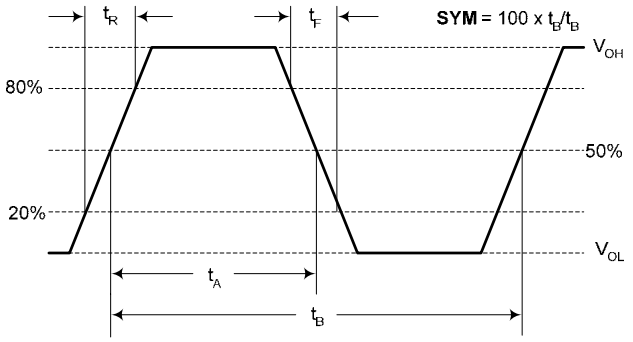


Figure 2. 10K LVPECL Waveform

Outline Diagram

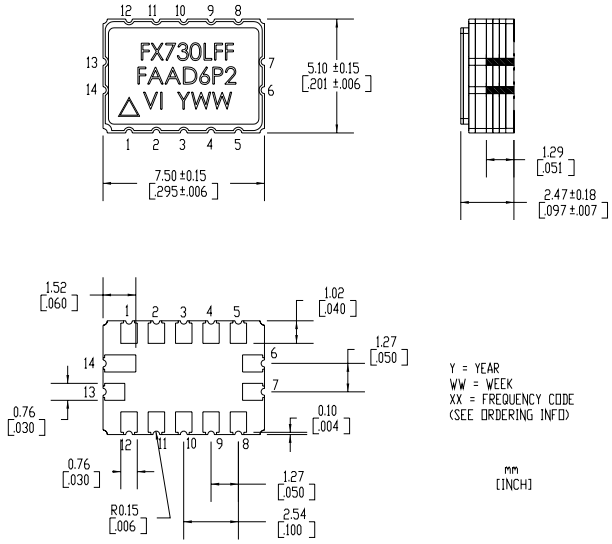


Figure 3.

Suggested Pad Layout

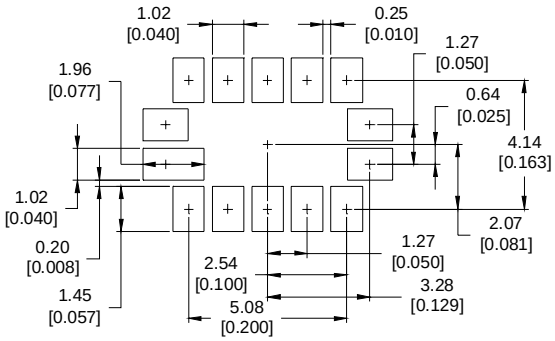


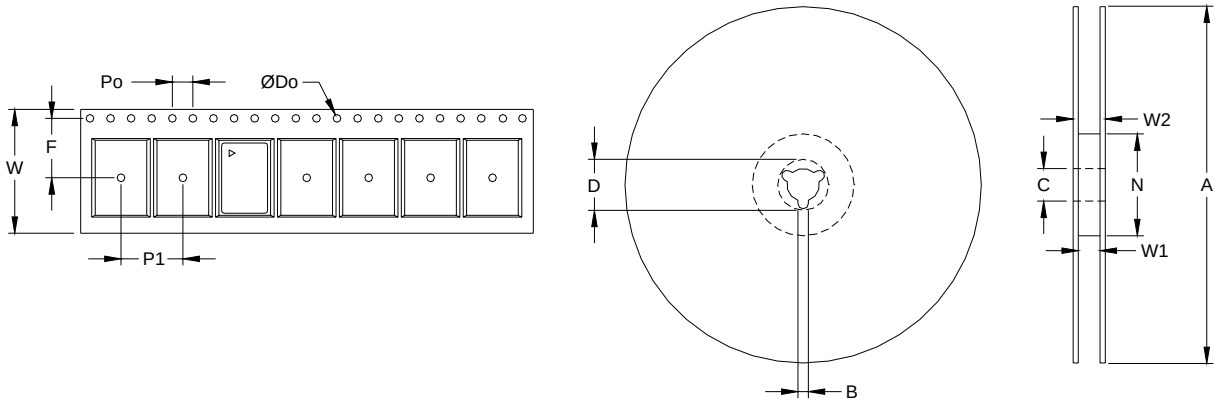
Figure 4.

Table 2. Pin Out

Pad #	Symbol	I/O	Level	Function
1	BRCLK	I	NC or LVPECL, LVDS	NC or For external divider applications = PD Feedback Frequency
2	LD	O	CMOS	Lock Detect Logic "0" = FX Locked Logic "1" = No input Output transitioning = Out of Lock
3	GND	GND	Supply	Case and Electrical Ground
4	MODE[1]	I	CMOS	FX Operating Mode Logic "0" = Standard PLL Operation *Normal setting* Logic "1" = FIN coupled to FOUT
5	GND	GND	Supply	Case and Electrical Ground
6	LFN		Analog	Loop Filter Node
7	CLFN		Analog	Complementary Loop Filter Node
8	FOUT	O	LVPECL or LVDS	Frequency Output
9	CFOUT	O	LVPECL or LVDS	Complementary Frequency Output
10	VCC	I	Supply	Power Supply Voltage (+3.3V ±5%)
11	CFIN	I	LVPECL	Complementary Input Frequency For CMOS inputs, AC-couple unused input to ground or negative supply.
12	FIN	I	CMOS or LVPECL	Input Frequency
13	GND	GND	Supply	Case and Electrical Ground
14	CBRCLK	I	NC or LVPECL, LVDS	NC or For external divider applications = Comp. PD Feedback Frequency

1. Do not leave the MODE pin floating, it should be set to a logic 0 or ground for normal operation.

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
FX-730	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Curret	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature/Duration	T_{PEAK} / t_P	260 / 40	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods can adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this data sheet. Permanent damage is also possible if any device input draws greater than 100 mA.

Application Circuits

Please contact Vectron application engineering for assistance.

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The FX-730 family is undergoing the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the FX-730 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

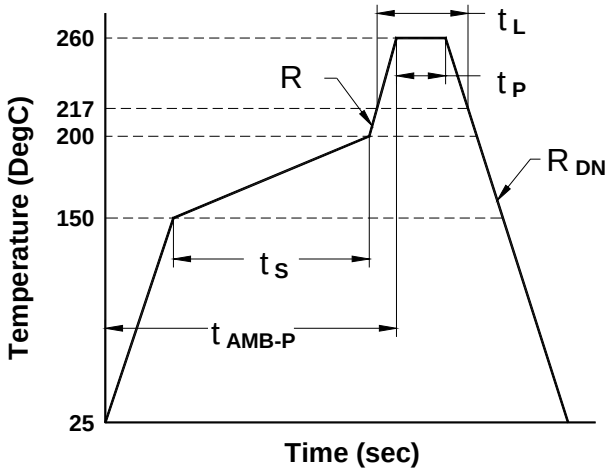
ESD Ratings

Model	Minimum	Conditions
Human Body Model	1000 V	MIL-STD 883, Method 3015
Charged Device Model	350 V	JEDEC, JESD22-C101

Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The FX-730 device is hermetically sealed so an aqueous wash is not an issue.



Standard Frequencies (MHz)

18.7500	EE	39.0625	HH	80.0000	K9	166.6286	M5	353.6763	RD	693.4830	R6
19.4400	D6	39.8437	HJ	80.5664	KJ	167.3316	N2	491.5200	PM	707.3527	TC
19.5312	DZ	40.0000	JF	82.1777	KL	168.0406	N3	531.2500	P8	716.5732	T1
19.9218	ED	40.2830	KK	83.3142	KN	176.8381	NA	569.1964	P9	718.7500	T5
20.0000	E2	41.0888	KM	83.6658	KR	201.4160	N1	600.0000	PR	719.7344	T3
20.5444	EF	41.6571	KP	84.0203	KU	300.0000	PT	622.0800	P2	748.0709	T6
20.8285	EG	41.8329	KT	88.4190	KW	311.0400	P1	625.0000	P3	750.0000	T7
20.9165	EH	42.0101	KV	125.0000	L4	312.5000	PU	637.5000	PG	777.6000	T4
21.0050	EJ	44.2095	KX	150.0000	MB	318.7500	PV	640.0000	PN	779.5686	T8
21.1047	EK	51.8400	J4	155.5200	M2	320.0000	PP	644.5313	P4	780.8810	TD
21.1416	E3	61.4400	J5	156.2500	M3	322.2656	PW	657.4219	PB	781.2500	T9
30.7200	H1	75.0000	KH	159.3750	M7	328.7109	PX	666.5143	P5	796.8750	TB
31.2500	H8	77.7600	K2	160.0000	M1	333.2571	PY	669.3266	R3	805.6641	TA
37.5000	HK	78.1250	K3	161.1328	M4	334.6633	RB	672.1627	R5	809.0635	TE
38.8800	H5	79.6875	KG	164.3554	M9	336.0813	RC	690.5692	R4		

Ordering Information

FX-730 - X X X - X X X - XX-XX

Product Family
FX: Frequency Translator

Package
730: 5.0 x 7.5 x 2.2 mm

Supply Voltage
L: 3.3 Vdc

Output
F: LVPECL (45/55% symmetry)
P: LVDS (45/55% symmetry)

Operating Temperature
C: 0 to 70°C
F: -40 to 85°C

Lock(APR) Range
F: ± 32 ppm
G: ± 50 ppm

Feedback Divider[2]
A: Factory set
B: External divider, prescaler = 1

Output Divider[2,3]
A: Factory set
B: Divide by 1
C: Divide by 2
D: Divide by 4

Input Frequency[1,2]
See Above

Output Frequency[1,3]
See Above

1. Not all combinations are possible. Please consult with your Vectron marketing representative for application assistance. Other frequencies available upon request.
2. When ordering the FX-730 with the external divider option, the feedback and output dividers must be specified. Please note that specifying the input frequency is optional for the external divider configuration. The "XX" place holder will be used when the input frequency is non-specified.
3. Note that the the Output Frequency = Internal VCSO/Output Divider. 500 MHz ≤ VSCO Frequency ≤ 850 MHz.

For Additional Information, Please Contact:

VECTRON INTERNATIONAL A DOVER COMPANY

USA: Vectron International • 267 Lowell Rd. Hudson, NH 03051 •
Tel: 1-88-VECTRON-1 • Fax: 1-888-FAX-VECTRON
EUROPE: Landstrasse, D-74924, Neckarbischofsheim, Germany •
Tel: 49 (0) 7268 8010 • Fax: 49 (0) 7268 801281
ASIA: 1F-2F, No 8 Workshop, No. 308 Fenju Road, WaiGaoQiao Free Trade Zone, Pudong, Shanghai, China 200131
Tel: 86 21 5048 0777 • Fax: 86 21 5048 1881