



RF Power Field Effect Transistor LDMOS, 865 — 960 MHz, 30W, 26V

5/14/04

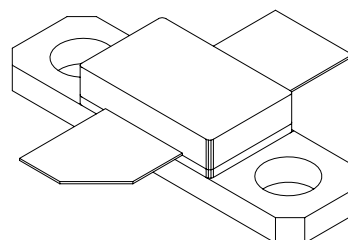
Preliminary

MAPLST0810-030CF

Features

- Designed for 865 to 960 MHz Broadband Commercial and Base Station Applications.
- Typical CW RF Performance at 960MHz, 26V_{DC}:
 - P_{OUT}: 30W (P_{1dB})
 - Gain: 18dB
 - Efficiency: 50%
- Ruggedness: 10:1 VSWR @ 30W CW, 26V, 925MHz
- High Gain, High Efficiency and High Linearity
- Excellent Thermal Stability

Package Style



P-239

Maximum Ratings

Parameter	Symbol	Rating	Units
Drain—Source Voltage	V _{DSS}	65	V _{dc}
Gate—Source Voltage	V _{GS}	20	V _{dc}
Total Power Dissipation @ T _C = 25 °C	P _D	97	W
Storage Temperature	T _{STG}	-40 to +150	°C
Junction Temperature	T _J	+200	°C

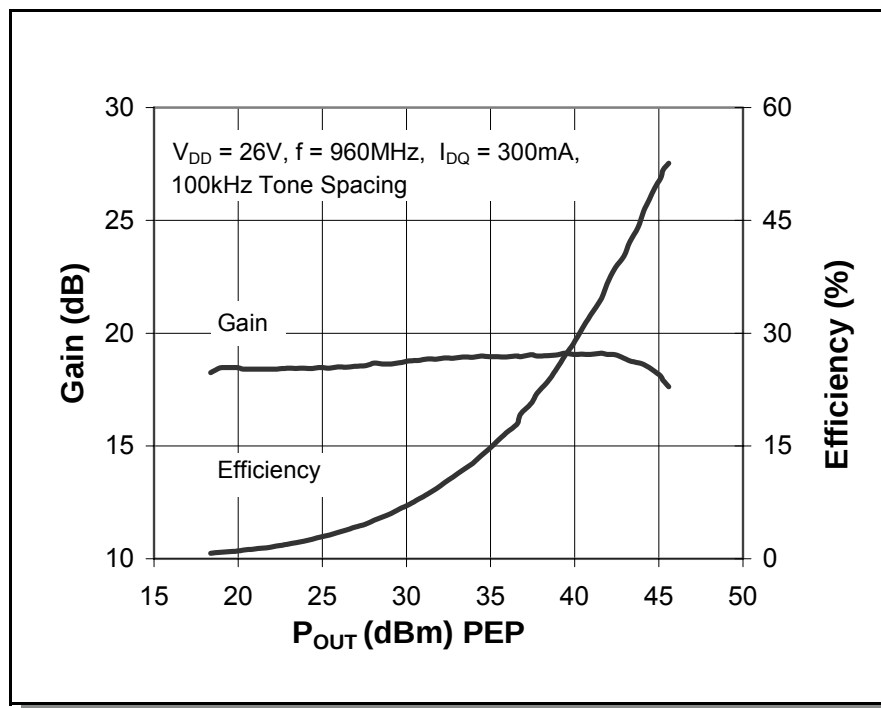
Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	R _{θJC}	1.8	°C/W

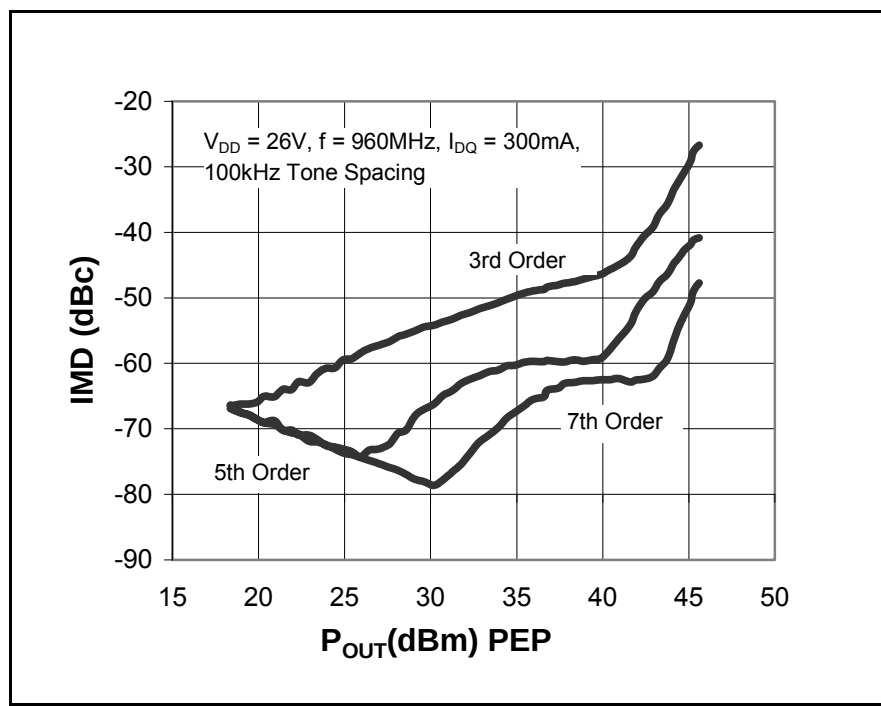
NOTE—CAUTION—MOS devices are susceptible to damage from electrostatic charge. Precautions in handling and packaging MOS devices should be observed.

Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS @ 25°C					
Drain-Source Breakdown Voltage ($V_{GS} = 0$ Vdc, $I_D = 20$ μ Adc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 26$ Vdc, $V_{GS} = 0$)	I_{DSS}	—	—	1	μ Adc
Gate—Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$)	I_{GSS}	—	—	3	μ Adc
Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 100$ μ A)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26$ Vdc, $I_D = 300$ mA)	$V_{DS(Q)}$	—	4.0	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1$ A)	$V_{DS(on)}$	—	0.20	—	Vdc
Forward Transconductance ($V_{GS} = 10$ Vdc, $I_D = 1$ A)	Gm	—	2.0	—	S
DYNAMIC CHARACTERISTICS @ 25°C					
Input Capacitance ($V_{DS} = 26$ Vdc, $V_{GS} = 0$, $f = 1$ MHz)	C_{iss}	—	50	—	pF
Output Capacitance ($V_{DS} = 26$ Vdc, $V_{GS} = 0$, $f = 1$ MHz)	C_{oss}	—	32	—	pF
Reverse Transfer Capacitance ($V_{DS} = 26$ Vdc, $V_{GS} = 0$, $f = 1$ MHz)	C_{rss}	—	1.4	—	pF
RF FUNCTIONAL TESTS @ 25°C (In M/A-COM Test Fixture)					
Common Source Amplifier Gain ($V_{DD} = 26$ Vdc, $I_{DQ} = 300$ mA, $f = 920$ & 960 MHz, $P_{OUT} = 30$ W)	G_P	—	18	—	dB
Drain Efficiency ($V_{DD} = 26$ Vdc, $I_{DQ} = 300$ mA, $f = 920$ & 960 MHz, $P_{OUT} = 30$ W)	EFF (η)	—	50	—	%
Input Return Loss ($V_{DD} = 26$ Vdc, $I_{DQ} = 300$ mA, $f = 920$ & 960 MHz, $P_{OUT} = 30$ W)	IRL	—	12	—	dB
Output VSWR Tolerance ($V_{DD} = 26$ Vdc, $I_{DQ} = 300$ mA, $f = 920$ & 960 MHz, $P_{OUT} = 30$ W, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

Preliminary



Graph 1. Power Gain and Drain Efficiency vs. Output Power



Graph 2. Intermodulation Distortion vs. Output Power

Preliminary

Technical drawing of a microfluidic chip, showing top and side views with dimensions and labels.

Top View Dimensions:

- Overall width: .800 [20.32]
- Distance from left edge to center of left well: .562 [14.27]
- Distance between centers of wells: .360 [9.14]
- Distance from center of right well to right edge: .230 [5.84]
- Well diameter: 2X ϕ .130 [ϕ 3.30]
- Well depth: .235 $\pm$.010 [5.97 $\pm$ 0.25]
- Gate width: 2X .215 [5.46]
- Gate height: .157 $\pm$.010 [3.99 $\pm$ 0.25]
- Gate thickness: .082 $\pm$.010 [2.08 $\pm$ 0.25]
- Channel width: 2X .005 $\pm$.001 [0.13 $\pm$ 0.03]
- Channel height: .060 [1.52]

Labels:

- DRAIN
- SOURCE
- GATE
- 4X 45° X .040

UNLESS OTHERWISE NOTED, TOLERANCES ARE INCHES $\pm$.005" [MILLIMETERS $\pm$ 0.13MM]

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