SAMSUNG
Semiconductor

KS84EC30

DYNAMIC RAM CONTROLLER

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FEATURES

- 40 MHz operation
- Easy interface to Motorola and Intel CPUs
- 68040/68EC030 burst mode operation
- I486 burst mode operation
- Page, static column and nibble mode accesses
- Interleaved and non-interleaved accesses
- Synchronous and asynchronous operation
- Direct drive for 256K, 1Mbit and 4Mbit DRAMs
- Page switch detection logic
- Built in precision delay line
- Four independent $\overline{RAS}$ and $\overline{CAS}$ outputs
- Programmable wait state generation logic
- Single or burst refresh
- Error scrubbing during refresh
- CMOS technology for low power consumption
- TTL compatible inputs
- 68-pin PLCC package

PRODUCT OVERVIEW

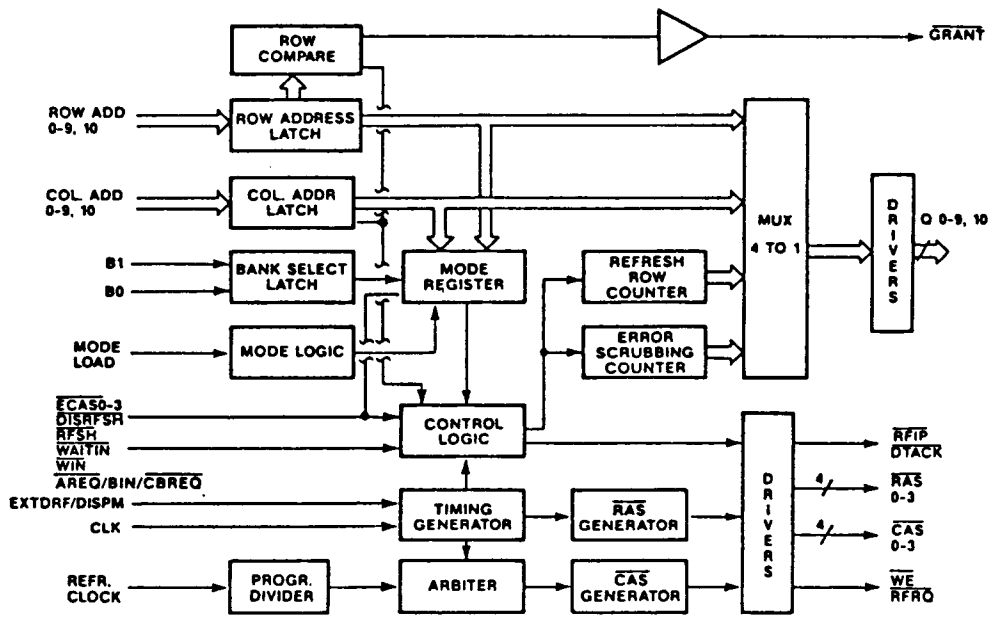
The Samsung KS84EC30 is a high performance DRAM controller designed for high speed DRAM arrays up to 4Mbytes in size. It simplifies the interface between the microprocessor and DRAM array, while also significantly reducing the required design time.

The KS84EC30 is an enhanced version of its KS84C31 counterpart. Like the KS84C31, this user programmable device is an economical and flexible design solution. The 26-bit programmable Mode Register allows the selection of various options and features.

The MC68EC030™, MC68040™ and i486™ microprocessors are supported by special programming modes specifically tailored to their bus operations.

Figure 1 shows a block diagram of the KS84EC30.

Figure 1. KS84EC30 Block Diagram



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™ i486 is a registered trademark of Intel, Inc.

INTRODUCTION

The KS84EC30 is a dynamic RAM controller (hereafter referred to as DRC) which is built upon the proven KS84C31 architecture with enhancements that improve memory access time. The DRC contains all of the advanced features of the KS84C31 including the capabilities of address latches, refresh counter, refresh clock, address multiplexor, precision delay line, and refresh/access arbitration logic.

Improvements in the $\overline{RAS}$, $\overline{CAS}$ and address drivers reduce propagation delays by up to 42% over the KS84C31. A programmable system interface allows any manufacturer's CPU to be easily interfaced to DRAM arrays up to 4Mbytes in size.

The incorporation of on-chip page detection logic enables the DRC to support random accesses within a page for use with page and static column mode DRAMs. A 2-bit wrap around column counter may be used during burst accesses. On-chip $\overline{RAS}$ timeout circuitry enables the DRC to maintain an active $\overline{RAS}$ signal while EPROM or I/O is referenced, greatly improving system performance in embedded control applications and during data transfers between memory and I/O.

The MC68EC030, MC68040 and i486 burst cache fill accesses are supported. The special 68030 programming mode supports a burst memory access which doubles the 68EC030's cache hit ratio when compared against memory controllers that inhibit bursting.

The DRC must be programmed after power up before the DRAM array is referenced. The DRC is programmed through the address bus.

There are two methods of programming the chip. The first method, Mode Load , is performed by first asserting the mode load ($\overline{ML}$) signal and presenting the programming selection on the row, column, bank and $\overline{ECAS}$ inputs. The programming selection is loaded into the Mode Register when $\overline{ML}$ is negated.

The second method, Fake Access, is performed by first asserting $\overline{ML}$, then performing a chip selected access. The programming value present on the address bus when $\overline{AREQ}$ is asserted is loaded into the Mode Register. The DRC then asserts the appropriate control signals to terminate the chip selected access.

The DRC supports two access modes, synchronous (Access Mode 0) and asynchronous (Access Mode 1). To access the DRAM in Mode 0, the address latch enable (ALE) signal is asserted. $\overline{RAS}$ will be asserted on the next rising clock edge. To access the DRAM in Mode 1, the address strobe ($\overline{ADS}$) signal is asserted causing $\overline{RAS}$ to be asserted immediately.

The KS84EC30 DRC offers four refreshing control modes:

1) internal automatic refreshing

2) internal automatic burst refreshing

3) externally controlled/burst refreshing

4) refresh request/acknowledge refreshing

When using internal automatic refreshing, the DRC's refresh request clock generates internal refresh requests. The DRC arbitrates between refresh requests and accesses. If an access is not currently in progress, the DRC will assert the refresh in progress signal ($\overline{RFIP}$). The refresh will start on the next rising clock edge. If an access had been in progress, the refresh would be delayed until the access is terminated.

Internal automatic burst refreshing is available when Page Mode is programmed. After the refresh request clock has generated the fifth internal refresh request, the DRC will arbitrate between the refresh request and any accesses in progress. The DRC will assert $\overline{RFIP}$ and perform a five refresh burst.

To use externally controlled burst/refreshing, the internally requested refreshes are disabled by asserting the disable refresh ($\overline{DISFRSH}$) signal. A refresh can now be requested externally by asserting the refresh ($\overline{RFSH}$) signal. The DRC will arbitrate between accesses and external refresh requests, assert $\overline{RFIP}$ and perform the refresh.

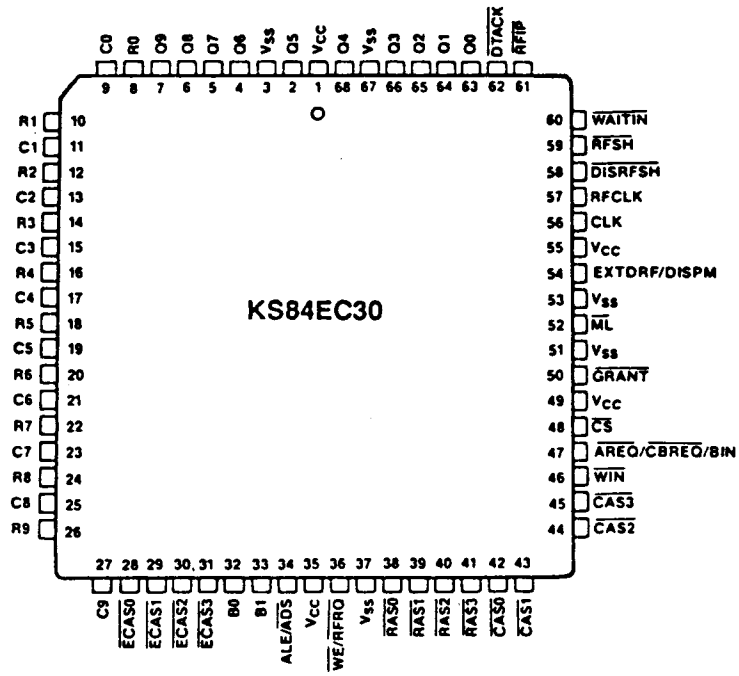
When refresh request/acknowledge refreshing is used, the DRC broadcasts the internal refresh request by asserting the refresh request ($\overline{RFRQ}$) signal. External circuitry can determine when to enable the refresh by asserting $\overline{RFSH}$. When $\overline{RFSH}$ is asserted, the DRC will perform an externally controlled/burst refresh.

The DRC supports two types of refreshing

1) $\overline{RAS}$ Only

2) $\overline{RAS}$ Only with Error Scrubbing

Figure 2. Pin Configuration of the KS84EC30 DRAM Controller



In a $\overline{RAS}$ only refresh, all the $\overline{RAS}$ outputs will be asserted and negated at once. Error scrubbing is the same as $\overline{RAS}$ only refresh except that a $\overline{CAS}$ and column address will be asserted during refresh, allowing the system to run the data through an error detection/correction chip and write it back to memory if an error has occured.

The DRC provides wait state support through its $\overline{DTACK}$ and $\overline{GRANT}$ output signals. Both signals may be used during Modes 0 and 1. $\overline{DTACK}$ is asserted by the on-chip wait state logic after a pre-programmed number of clock cycles to terminate the access. $\overline{GRANT}$ is asserted by the DRC to inform external circuitry that the DRC has begun an access. $\overline{DTACK}$ can be dynamically delayed by asserting the $\overline{WAITIN}$ input.

When a page miss is detected, the DRC will insert wait states during the access and precharge the memory.

The DRC has address latches, used to latch the row, column, and bank address inputs. The latches may also be used in fall through mode, even when the DRC is programmed for page mode operation. (The page address is latched in a separate page register).

The $\overline{RAS}$ and $\overline{CAS}$ drivers can be configured to drive a 1, 2, 3 or 4 bank memory array up to 36 bits in width (32 data, 4 parity). The $\overline{CAS}$ enable ($\overline{ECAS}$) signals can then be used to selectively enable the $\overline{CAS}$ drivers for byte writing without requiring external logic. The DRC contains internal logic that ensures that the $\overline{CAS}$ outputs will not be asserted in case of a page miss, thus preventing spurious data writes to an incorrect page.

When configuring the DRC for more than one bank, memory interleaving can be used. The DRC can perform 2 or 4 way interleaving to eliminate wait states due to $\overline{RAS}$ precharge time.

The KS84EC30, as shown in Figure 2, is available in a 68 pin PLCC and supports 256K, 1M and 4Mbit (1M · 4) DRAMs. The logic symbol is shown in Figure 3.

Figure 3. Logic Symbol

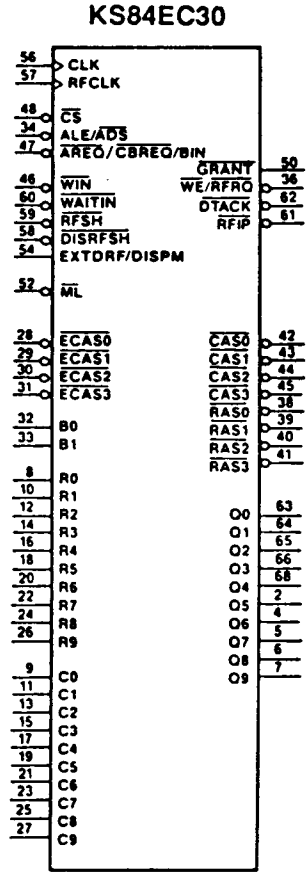


Table 1 shows detailed pin allocations for the KS84EC30.

Table 1. KS84EC30 Pin Allocations

Pin No.	Signal Abbrev.	Signal Name
1	V_{CC}	V_{CC}
2	Q5	Multiplexed Address 5
3	V_{SS}	V_{SS}
4	Q6	Multiplexed Address 6
5	Q7	Multiplexed Address 7
6	Q8	Multiplexed Address 8
7	Q9	Multiplexed Address 9
8	R0	Row Address 0
9	C0	Column Address 0
10	R1	Row Address 1
11	C1	Column Address 1
12	R2	Row Address 2
13	C2	Column Address 2
14	R3	Row Address 3
15	C3	Column Address 3
16	R4	Row Address 4
17	C4	Column Address 4
18	R5	Row Address 5
19	C5	Column Address 5
20	R6	Row Address 6
21	C6	Column Address 6
22	R7	Row Address 7
23	C7	Column Address 7
24	R8	Row Address 8
25	C8	Column Address 8
26	R9	Row Address 9
27	C9	Column Address 9
28	$\overline{ECAS0}$	Enable $\overline{CAS0}$
29	$\overline{ECAS1}$	Enable $\overline{CAS1}$
30	$\overline{ECAS2}$	Enable $\overline{CAS2}$
31	$\overline{ECAS3}$	Enable $\overline{CAS3}$
32	B0	Bank Select 0
33	B1	Bank Select 1
34	ALE/$\overline{ADS}$	Address Latch Enable/ Address Strobe
35	V_{CC}	V_{CC}
36	$\overline{RFRQ/WE}$	Refresh Request/Write Enable
37	V_{SS}	V_{SS}
38	$\overline{RAS0}$	Row Address Strobe 0
39	$\overline{RAS1}$	Row Address Strobe 1
40	$\overline{RAS2}$	Row Address Strobe 2
41	$\overline{RAS3}$	Row Address Strobe 3
42	$\overline{CAS0}$	Column Address Strobe 0
43	$\overline{CAS1}$	Column Address Strobe 1
44	$\overline{CAS2}$	Column Address Strobe 2
45	$\overline{CAS3}$	Column Address Strobe 3
46	$\overline{WIN}$	Write Enable Input
47	$\overline{AREQ}$	Access Request
	$\overline{CBREQ}$	Cache Burst Request
	BIN	Burst Inhibit
48	$\overline{CS}$	Chip Select
49	V_{CC}	V_{CC}
50	$\overline{GRANT}$	Access Grant
51	V_{SS}	V_{SS}
52	$\overline{ML}$	Mode Load
53	V_{SS}	V_{SS}
54	EXTDRF	Extend Refresh
	DISPM	Disable Page Mode
55	V_{CC}	V_{CC}
56	CLK	Clock
57	RFCLK	Refresh Clock
58	$\overline{DISRFSH}$	Disable Internal Refresh
59	$\overline{RFSH}$	External Refresh Request
60	$\overline{WAITIN}$	Add Wait State
61	$\overline{RFIP}$	Refresh in Progress
62	$\overline{DTACK}$	Data Transfer Acknowledge
63	Q0	Multiplexed Address 0
64	Q1	Multiplexed Address 1
65	Q2	Multiplexed Address 2
66	Q3	Multiplexed Address 3
67	V_{SS}	V_{SS}
68	Q4	Multiplexed Address 4

Table 2. Interface Signal Descriptions

Symbol	Type	Descriptions
Access Signals		
$\overline{ADS}$ (ALE)	I	**Address Strobe (Address Latch Enable)**: This input latches row, column and bank addresses, and initiates the DRAM access. $\overline{ADS}$ (ALE) must be invoked for every non-burst access. $\overline{ADS}$ (ALE) need only be invoked for the opening cycle of a burst access when used with microprocessors that only assert $\overline{ADS}$ (ALE) during the opening cycle. In Access Mode 0, this input functions as Address Latch Enable (ALE). In Access Mode 1, this input functions as Address Strobe ($\overline{ADS}$).
$\overline{CS}$	I	**Chip Select**: The $\overline{CS}$ input must be active to enable a DRAM access. $\overline{CS}$ must enable every non-burst access. $\overline{CS}$ need only be invoked for the opening cycle of a burst access when used with microprocessors that only assert $\overline{ADS}$ (ALE) during the opening access.
$\overline{AREQ}$ ($\overline{CBREQ}$) (BIN)	I	**Access Request (Cache Burst Request) (Burst Inhibit)**: This input terminates an access. $\overline{AREQ}$: In Single Access Mode, this input functions as Access Request. It brings $\overline{RAS}$ and $\overline{CAS}$ high to terminate the access. In Page Access Mode, $\overline{AREQ}$ only brings $\overline{CAS}$ high. $\overline{CBREQ}$: In 68030 Burst Mode, this signal functions as Cache Burst Request. $\overline{CBREQ}$ is sampled on the rising edge of CLK that negates $\overline{DTACK}$. Directly compatible with the MC68EC030's $\overline{CBREQ}$ signal, it controls the termination of the DRC's burst access. It brings $\overline{RAS}$ and $\overline{CAS}$ high to terminate the burst. When combined with Page Mode, only $\overline{CAS}$ is brought high. BIN: When programmed for 68040 Burst Mode, this signal functions as Burst Inhibit. Burst Inhibit is sampled on the rising edge of CLK that negates $\overline{DTACK}$. BIN prevents the DRC from bursting if the CPU aborts the burst or is performing a single access. It brings $\overline{RAS}$ and $\overline{CAS}$ high to terminate the burst. When combined with Page Mode, only $\overline{CAS}$ is brought high.
$\overline{DTACK}$	O	**Data Transfer Acknowledge**: This output is asserted to terminate the CPU access. In Single Access Mode and Page Mode, it is negated when the access is terminated by $\overline{AREQ}$. In both burst modes, $\overline{DTACK}$ is negated on the first rising clock edge after it has been asserted.
$\overline{WAITIN}$	I	**Wait State Insert**: This input is used to dynamically add wait states during a bus cycle. If R6=0 during programming, $\overline{WAITIN}$ is used to add one wait state during the access. $\overline{WAITIN}$ is sampled once during the access, when $\overline{DTACK}$ is to be asserted by the DRC. $\overline{DTACK}$ will remain negated for one more rising CLK edge if $\overline{DTACK}$ is rising edge triggered or one more falling CLK edge if $\overline{DTACK}$ is falling edge triggered. $\overline{WAITIN}$ will not be sampled again, until the next access. If R6=1 during programming, $\overline{WAITIN}$ may be used to defer $\overline{DTACK}$ indefinitely. $\overline{WAITIN}$ is sampled at the access start. If $\overline{WAITIN}$ is inactive, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges. If $\overline{WAITIN}$ was active, the $\overline{DTACK}$ CLK edge count is deferred. $\overline{WAITIN}$ will be continually sampled on the rising edge of CLK if $\overline{DTACK}$ is rising edge triggered or on the falling edge of CLK if $\overline{DTACK}$ is falling edge triggered. Once $\overline{WAITIN}$ is negated, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges and will not sample $\overline{WAITIN}$ again until the next access.

Table 2. Interface Signal Descriptions (Continued)

Symbol	Type	Descriptions
Access Signals (Continued)		
$\overline{GRANT}$	O	**Access Grant**: This output is asserted only when $\overline{RAS}$ is asserted for a DRAM access. It is asserted at the beginning of an access to indicate that the access has begun. If an access is deferred due to a refresh cycle, page miss, or to satisfy $\overline{RAS}$ precharge time, $\overline{GRANT}$ will not be asserted until the access has begun. $\overline{GRANT}$ will remain asserted until the access $\overline{RAS}$ is negated.
Address, R/$\overline{W}$ and Programming Signals		
C0-9	I	**Column Address Inputs**: These address bits are connected to the CPU's address bus. When the DRC is programmed for use with page mode or static column DRAMs, they should be connected to the low order address bits.
R0-9	I	**Row Address Inputs**: Theses address bits are connected to the CPU's address bus. When the DRC is programmed for use with page or static column mode DRAMs, they should be connected to the higher order address bits.
B0, B1	I	**Bank Select**: These inputs select the memory bank to be addressed. Up to four banks are supported by the DRC.
$\overline{ECAS0\text{-}3}$	I	**Enable $\overline{CAS0\text{-}3}$**: These inputs are used to enable or disable individual $\overline{CAS}$ outputs when accessing bytes, words or doublewords. They can also be used to delay the falling edge of $\overline{CAS}$.
$\overline{WIN}$	I	**Write Enable Input**: This input controls the Write Enable ($\overline{WE}$) output. If programmed to do so, it also delays the falling edge of $\overline{CAS}$ by one rising CLK edge during page hits and one CLK period during burst accesses. It does not delay the falling edge of $\overline{CAS}$ in Single Access Mode or the opening cycle of a burst access that results in a page miss. When the leading edge of $\overline{CAS}$ is delayed by $\overline{WIN}$, one wait state is automatically added to the access cycle. $\overline{WIN}$ is sampled when a burst or page hit access starts in all operating modes and also on the rising edge of CLK that negates $\overline{DTACK}$ when the DRC is bursting.
$\overline{ML}$	I	**Mode Load**: This input strobes the row, column, bank and $\overline{ECAS0\text{-}3}$ inputs into the Mode Register.
DRAM Control Signals		
Q0-9	O	**Address Outputs**: These outputs are the multiplexed address bits (R0-9, C0-9). They access the memory for read, write and refresh operations. The output loading is rated at 50 pF. 22 ohm series damping resistors are suggested for the Q outputs.
$\overline{RAS0\text{-}3}$	O	**Row Address Strobe**: These output signals are used to strobe the row address into the DRAM.
$\overline{CAS0\text{-}3}$	O	**Column Address Strobe**:These output signals are used to strobe the column address into the DRAM.
$\overline{WE}$ ($\overline{RFRQ}$)	O	**Write Enable (Refresh Request)**: After power up and when the DRC is programmed for interleaved operation, this output functions as Refresh Request. When the DRC is not programmed for interleaved operation, this output may be programmed as Write Enable or Refresh Request. When programmed as $\overline{WE}$, this output is controlled by the $\overline{WIN}$ input. The output loading is rated at 50 pF. When programmed as $\overline{RFRQ}$, the DRC asserts this output whenever a refresh request has been generated by the internal refresh interval timer. $\overline{RFRQ}$ is negated when the refresh begins.

Table 2. Interface Signal Descriptions (Continued)

Symbol	Type	Descriptions
Refresh Control Signals		
EXTDRF (DISPM)	I	**Extend Refresh (Disable Page Mode)**: When the DRC is programmed to support error scrubbing, this pin is time multiplexed. During refresh, this input extends the refresh cycle to allow a read-modify-write cycle to be performed in a system with error scrubbing. During accesses, this pin is used to terminate $\overline{RAS}$ when the DRC is programmed for Page Mode. When the DRC is not programmed to support error scrubbing, this pin only functions as Disable Page Mode and does not affect refresh cycles.
$\overline{DISRFSH}$	I	**Disable Internal Refresh**: This input prevents the DRC from performing internally requested refreshes. This signal could be asserted to prevent the DRC from performing refreshes during DMA transfers, while the CPU is executing time critical code or if refreshes are going to be controlled externally.
$\overline{RFIP}$	O	**Refresh In Progress**: This output indicates that a refresh cycle is in progress. $\overline{RFIP}$ is asserted one clock cycle prior to the start of a refresh cycle.
$\overline{RFSH}$	I	**External Refresh**: Refresh requests can be generated externally by asserting this input when $\overline{DISRFSH}$ is low.
Clock Inputs		
CLK	I	**Sytem Clock**: This input should be connected to the system bus clock. It is used for access arbitration and timing.
RFCLK	I	**Refresh Clock**: This input determines the interval between internally requested refreshes. RFCLK must be synchronous to CLK, but need not be the same frequency as CLK. It is divided internally, according to the value in the Mode Register, so that refresh requests are generated at 15 μs or 13 μs intervals.

ACCESS START AND TERMINATION MODES

The KS84EC30 supports both synchronous and asynchronous access modes. The user selects the mode best suited to the microprocessor by programming bit B1 of the Mode Register.

Mode 0 — Synchronous Access Start and Termination

Mode 0 is selected when B1 = 0 during programming. To initiate a Mode 0 access, ALE is pulsed high and a valid $\overline{CS}$ signal is asserted before the input clock's (CLK) rising edge. The access will start on the rising edge of CLK as shown in Figure 4, provided that the ALE and $\overline{CS}$ setup times were observed, the $\overline{RAS}$ precharge time was met and a refresh was not currently in progress. If the $\overline{RAS}$ precharge time was not met from the previous access or a refresh was in progress, the DRC will wait until these events have taken place before asserting $\overline{RAS}$ on the rising edge of CLK.

The DRC will begin sampling $\overline{AREQ}$ on the rising edge of CLK after $\overline{DTACK}$ is asserted. The access will continue until $\overline{AREQ}$ is negated.

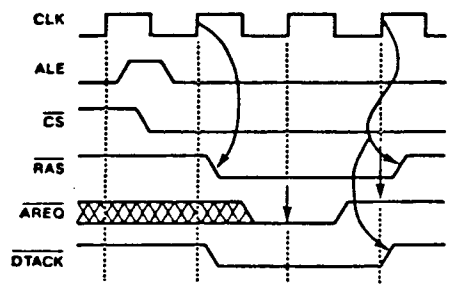
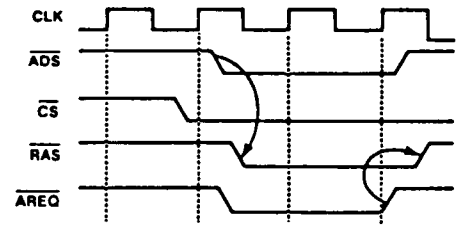


Figure 4. Synchronous Access Start and Termination

Mode 1 — Asynchronous Access Start and Termination

Mode 1 is selected when B1 = 1 during programming. To initiate a Mode 1 access, $\overline{CS}$ is asserted, followed by $\overline{ADS}$. The access will start when $\overline{ADS}$ is asserted as shown in Figure 5, provided that the $\overline{RAS}$ precharge time was met and a refresh was not currently in progress. If the $\overline{RAS}$ precharge time was not met from the previous access or a refresh was in progress, the DRC will wait until these events have taken place before asserting $\overline{RAS}$ on the rising edge of CLK. The access will be terminated when $\overline{AREQ}$ is negated.

Figure 5. Asynchronous Access Start and Termination



OPERATING MODES

The KS84EC30 may be programmed to operate in several different modes, depending on the CPU characteristics and type of DRAM used. The Single Access Mode is recommended for use in slower speed systems in which there is no advantage to be gained from a $\overline{CAS}$ only access and where the $\overline{RAS}$ precharge time is hidden between back to back accesses. For higher performance systems, Page Mode operation is provided and may be used with page or static column DRAMs. Two versions of burst mode operation, 68030 Burst Mode and 68040 Burst Mode are provided to support CPUs that are capable of performing burst accesses. Both burst modes may be used with nibble, page or static column DRAMs.

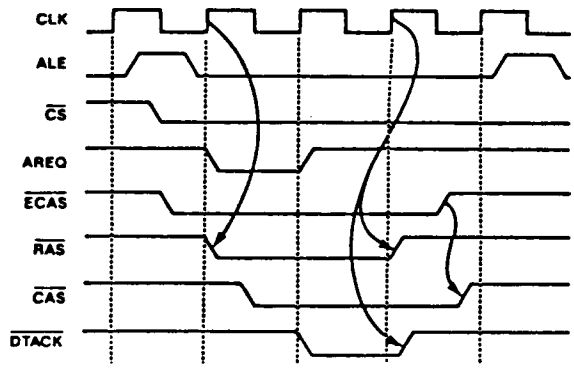
Interleaved Access Mode can provide a performance advantage when used in systems that support address pipelining. The user selects the operating mode best suited to the system's requirements by programming bits C4, C5, C6 and $\overline{ECAS1}$-$\overline{3}$ in the Mode Load Register.

Single Access Mode

Single Access Mode is selected when $\overline{ECAS1}$, $\overline{ECAS2}$, $\overline{ECAS3}$ = 0,0,0 during programming. The access is initiated by two signals, $\overline{ADS}$(ALE) and $\overline{CS}$, and is terminated by one signal, $\overline{AREQ}$. Both $\overline{RAS}$ and $\overline{DTACK}$ are negated when the access is terminated.

The user has the option of negating $\overline{CAS}$ when the access is terminated or up to one clock period later. If $\overline{ECAS0}$ = 0 during programming, $\overline{CAS}$ will be negated with $\overline{RAS}$ and $\overline{DTACK}$. If $\overline{ECAS0}$ = 1 during programming, $\overline{CAS}$ will remain asserted until the next rising CLK edge or the rising edge of $\overline{ECAS}$, whichever occurs first. This allows the DRAM to continue to drive the data bus while $\overline{RAS}$ is precharging. See Figure 6.

Figure 6. Single Access Mode with Synchronous Access Start and Extended $\overline{CAS}$



Page Mode Access

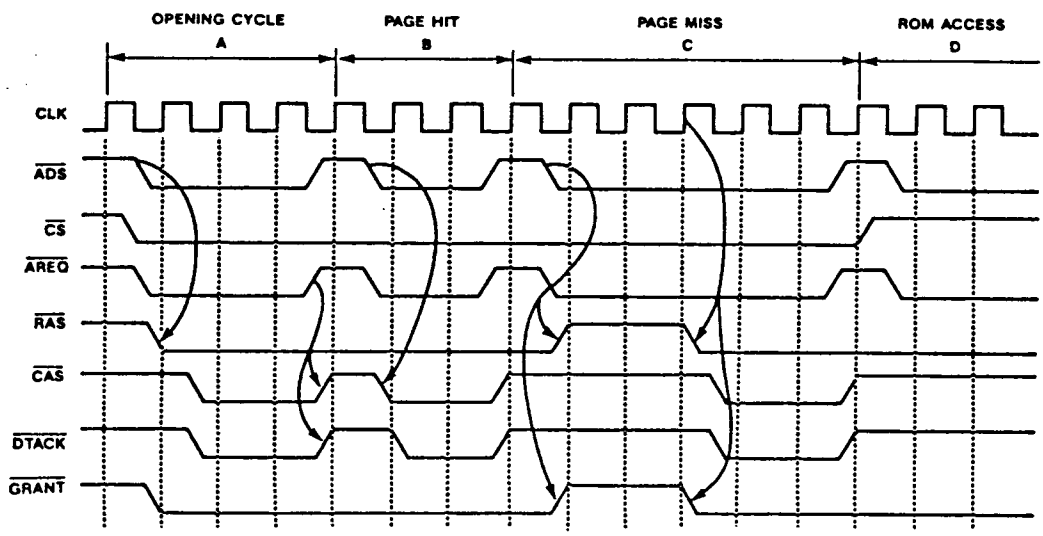
Page Mode is selected when $\overline{ECAS1}$, $\overline{ECAS2}$, $\overline{ECAS3}$ = 0,1,0 during programming. Page Mode allows the CPU to access random columns within a page without having to pay the penalties associated with $\overline{RAS}$ access and precharge time. Both page and static column mode DRAMs may be used. It is very similar in operation to the Single Access Mode, with only two notable exceptions:

1) Only $\overline{CAS}$ and $\overline{DTACK}$ are negated when $\overline{AREQ}$ terminates the access.
2) The DRC maintains $\overline{RAS}$ low even when the CPU is not accessing DRAM.

On-chip page detection logic detects page hits and misses. The DRC's on-chip wait state logic delays the assertion of $\overline{DTACK}$ in case of a page miss to allow for $\overline{RAS}$ precharge and $\overline{RAS}$ access time. An external signal, $\overline{GRANT}$, is asserted to indicate to external circuitry when the access has begun.

Several Page Mode accesses are shown in Figure 7. Access A occurred after a refresh cycle. The access was not delayed due to $\overline{RAS}$ precharge since the CPU initiated the access after the $\overline{RAS}$ was already precharged. Access B is a page hit. Access C is a page miss. Access D is an access to a memory location other than DRAM.

Figure 7. Page Mode Accesses



When programmed for Page Mode operation ($\overline{ECAS2}$ = 1), the DRC maintains $\overline{RAS}$ and $\overline{GRANT}$ low for 5 internal refresh requests (75 µs). After the 5th internal refresh request, both signals will be negated when $\overline{AREQ}$ terminates the access. The DRC will then perform a 5 refresh burst.

Certain applications may require that, at certain times, the DRAM is precharged prior to an access start. Since it is impossible to ensure that a given access will result in a page hit, and if the penalty of a page miss is intolerable, DISPM may be used to negate $\overline{RAS}$ when an access is completed.

If DISPM is asserted when there is no access or refresh in progress, $\overline{RAS}$ is negated immediately. If DISPM is asserted during an access, $\overline{AREQ}$ will negate both $\overline{RAS}$ and $\overline{CAS}$ when the access is completed. The DRC will continue to function as though it were programmed for Single Access Mode operation as long as DISPM is asserted. After DISPM is negated, all pending refreshes (up to 5) will be performed in a burst refresh.

When the DRC is not programmed to support error scrubbing, DISPM has no effect on $\overline{RAS}$ during refreshes. When the DRC is programmed to support error scrubbing, DISPM is time multiplexed with EXTDRF. EXTDRF will cause the refresh $\overline{RAS}$ to be extended when it is sampled active on the rising edge of CLK that was programmed to negate $\overline{RAS}$.

Burst Mode Accesses

In order to support high performance CPUs that can perform up to 4 memory accesses in a single burst, the MC68EC030 is capable of performing 4 accesses when provided with the starting address of the burst. The DRC supports two forms of burst mode operation. When programmed for 68040 Burst Mode, $\overline{CAS}$ is asserted on the falling edge of CLK and is negated on the rising edge of CLK. This mode should be used when the data is to be sampled on the rising edge of CLK such as with the MC68040 and i486 CPUs. To accomodate CPU's that sample data on the falling edge of CLK, such as the MC68EC030, 68030 Burst Mode should be used. In 68030 Burst Mode, $\overline{CAS}$ is asserted on the rising edge of CLK and is negated on the falling edge of CLK.

The user has the choice of using nibble, page or static column DRAMs in both burst modes. An on-chip address counter may be used while bursting, if desired. The 2-bit address counter wraps around to support CPU's that wrap around when filling their cache lines. The user can choose when to increment the address counter depending on whether page or static column DRAMs are used. The DRC's burst access can be terminated early if the CPU is performing a single access or aborts the burst.

Either burst mode may be combined with Page Mode operation to reduce the number of clock cycles required for the opening access of the burst by programming $\overline{ECAS2}$ = 1. When programmed in combination with Page Mode, $\overline{CAS}$ will be negated, but $\overline{RAS}$ will remain asserted after the last access of the burst.

If DISPM is asserted during an access, both $\overline{RAS}$ and $\overline{CAS}$ are negated when the access is completed. The DRC will continue to function as though it were not programmed for Page Mode ($\overline{ECAS2}$ = 0) as long as DISPM is asserted. After DISPM is negated, all pending refreshes (up to 5) will be performed in a burst refresh.

The on-chip address counter is enabled when the address latches are programmed to latch the address on the falling edge of $\overline{ADS}$(ALE). If the latches are transparent, the counter is disabled. When the latches are transparent, external circuitry may be used to provide a new column address to the DRC.

If the on-chip address counter is used, the user needs to select when the counter is incremented. If static column DRAMs are used, R6 = 0 should be programmed. If page mode DRAMs are used, R6 = 1 may be programmed. When R6 = 0, the column address will be incremented when $\overline{CAS}$ is negated. When R6 = 1, the column address is incremented before the access is completed, on the CLK edge that asserts $\overline{DTACK}$.

The $\overline{CAS}$ strobe is negated when the DRAM access is completed, even when static column DRAMs are used. This insures that data is not strobed into the incorrect page if a page miss occurs during a write access.

Since the $\overline{CAS}$ propagtion delay and precharge time is matched to the DRC's column address increment propagation delay, there is no performance penalty associated with bringing $\overline{CAS}$ high.

68040 Burst Access Mode

68040 Burst Mode operation is selected when $\overline{ECAS1}$, $\overline{ECAS3}$ = 0,1 during programming.

When programmed for 68040 Burst Mode, $\overline{CAS}$ is always negated by the same rising CLK edge that negates $\overline{DTACK}$. $\overline{CAS}$ is always asserted on the next falling CLK edge unless the DRC has completed the burst or if the burst was aborted.

The DRC's burst can be aborted by asserting the DRC's Burst Inhibit (BIN) input. BIN is sampled on the rising edge of CLK that negates $\overline{CAS}$ and $\overline{DTACK}$, and if asserted, the burst is aborted. Once aborted, the next access must be initiated with $\overline{ADS}$(ALE) and $\overline{CS}$.

Two 68040 Burst Mode accesses are shown in Figure 8. During the first access, the DRC is allowed to complete the burst normally. The second access was deferred due to $\overline{RAS}$ precharge. The burst was aborted during the second access by asserting BIN.

Figures 9 and 10 show the same accesses when 68040 Burst Mode is combined with Page Mode. In the case of Figures 9 and 10, the $\overline{RAS}$ precharge is due to a page miss.

Figure 8. 68040 Burst Mode Access ($\overline{ECAS2}$ = 0 Programmed)

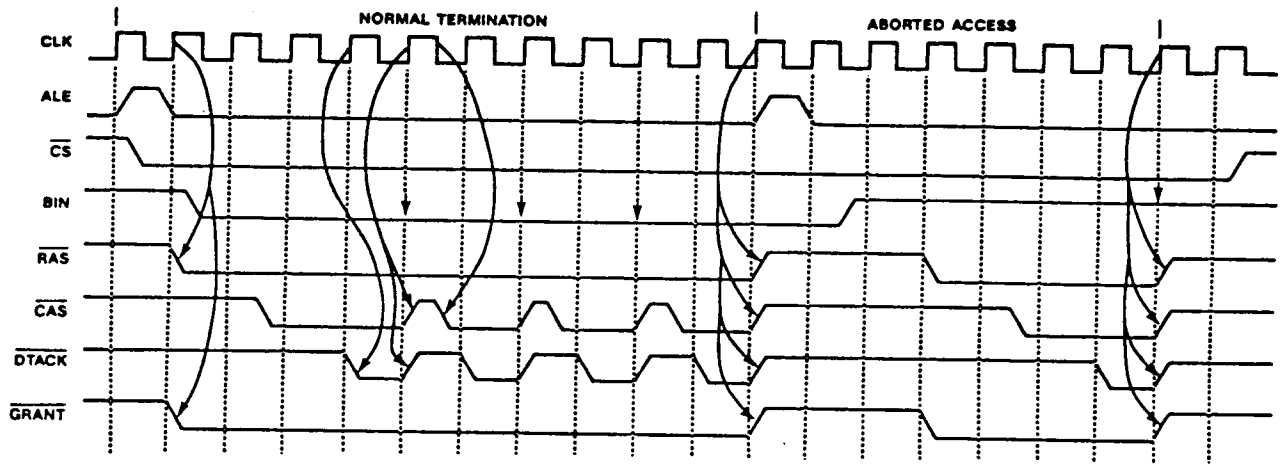


Figure 9. Burst Mode Access with Page Mode ($\overline{ECAS2}$ = 1, R6 = 0 Programmed)

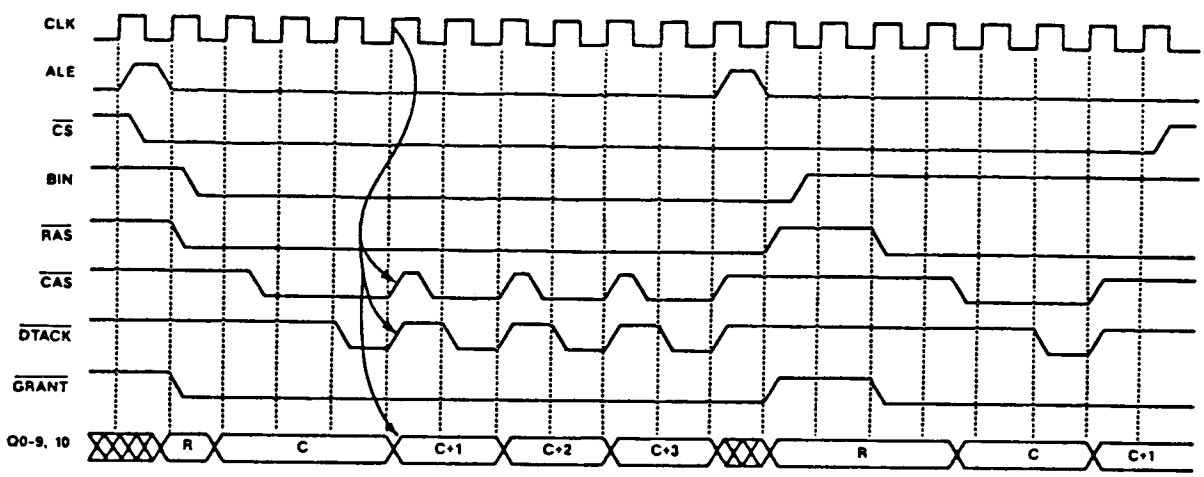
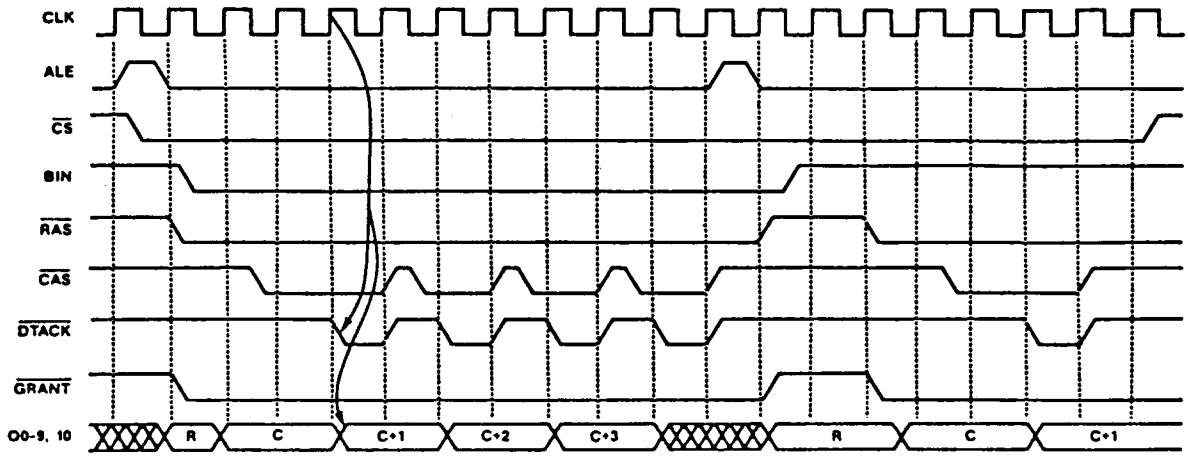


Figure 10. Burst Mode Access with Page Mode ($\overline{ECAS2}$ = 1, R6 = 1 Programmed)



68030 Burst Access Mode

The MC68EC030's synchronous burst cache fill operation is supported by programming the DRC for 68030 Burst Mode operation. 68030 Burst Mode operation is very similar to 68040 Burst Mode operation, with only two notable exceptions:

1) $\overline{CAS}$ is asserted on the rising edge of CLK and negated on the falling edge.
2) The handshake input $\overline{CBREQ}$ is provided and is sampled on the rising edge of CLK that negates $\overline{DTACK}$.

The DRC's $\overline{DTACK}$ output drives the MC68EC030's $\overline{STERM}$ and $\overline{CBACK}$ inputs.

68030 Burst Mode operation is selected when $\overline{ECAS1}$, $\overline{ECAS3}$ = 1,0 during programming.

Two 68030 Burst Mode accesses are shown in Figure 11. During the first access, the DRC is allowed to complete the burst normally. The second access was deferred due to $\overline{RAS}$ precharge. The burst was aborted during the second access by negating $\overline{CBREQ}$.

Figures 12 and 13 show the same accesses when 68030 Burst Mode is combined Page Mode. In the case of Figures 12 and 13, the $\overline{RAS}$ precharge is due to a page miss.

Figure 11. 68030 Burst Mode Access ($\overline{ECAS2}$ = 0 Programmed)

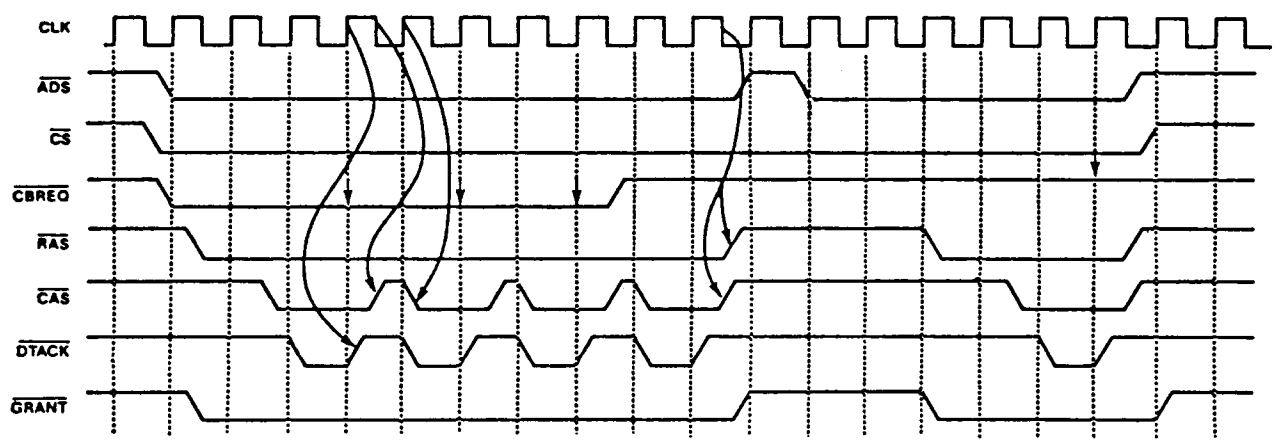


Figure 12. 68030 Burst Mode with Page Mode ($\overline{ECAS2}$ = 1, R6 = 0 Programmed)

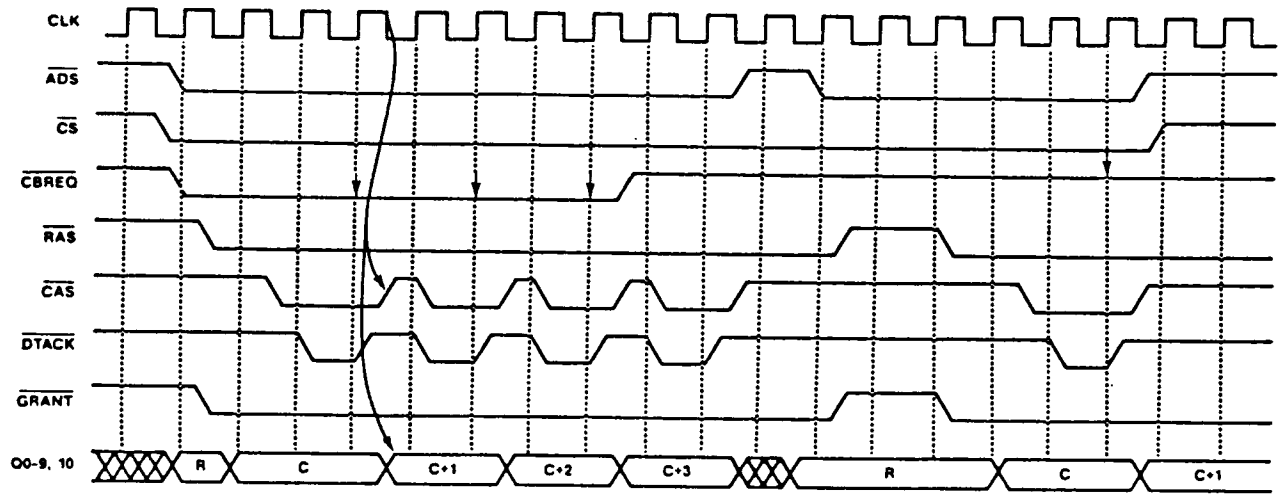
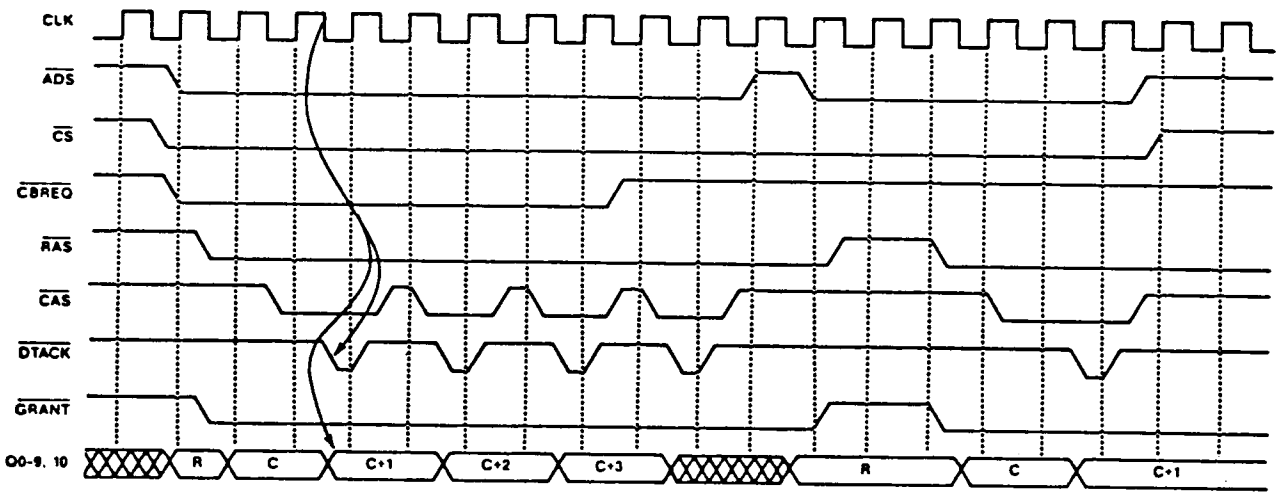


Figure 13. 68030 Burst Mode with Page Mode ($\overline{ECAS2}$ = 1, R6 = 1 Programmed)



Interleaved Access Modes

The KS84EC30 supports 2 or 4-way interleaved accesses between memory banks. By interleaving accesses, performance degradation due to $\overline{RAS}$ access and precharge time is minimized.

Interleaved Access Mode may be used in systems that support address pipelining. When interleaving accesses, the DRC supplies the next row address after the column address hold time is satisfied for the current access. If the next access is to a different bank of memory than the current access. $\overline{RAS}$ will be asserted for the next access by ALE($\overline{ADS}$).

Interleaved Access Mode is selected by programming the $\overline{RAS}$ and $\overline{CAS}$ configuration bits C4, C5 and C6. These bits enable the DRC to initiate an access to one bank with ALE($\overline{ADS}$) while maintaining an access to another bank with $\overline{AREQ}$. *The $\overline{GRANT}$ output should not be used in this mode.*

The ECASn bits should be programmed for Single Access Mode for proper interleaved operation. R8 = 0 should be programmed so that the DRAM controller will drive the new row address onto the bus after the column address hold time for the current access is satisfied.

Interleaved Access Mode should not be used in conjunction with page or burst mode operation. However, the $\overline{RAS}$ precharge time is hidden in these modes if consecutive accesses hit different banks. Only one CLK of precharge will be incurred when switching banks. The programmed number of precharge clock cycles will be observed if consecutive access hit the same memory bank.

Wait State Support

Wait states are required when a relatively slow DRAM is operating with a fast CPU. Wait states allow the CPU's bus cycle to be extended by one or more CPU clock periods. The KS84EC30 will insert wait states during the CPU's DRAM bus access in order to:

a) insert the desired number of wait states during the access,

b) delay the access until the refresh in progress is complete, or

c) delay the access to guarantee $\overline{RAS}$ precharge time.

The DRC generates two output signals to support the insertion of wait states. $\overline{GRANT}$ is asserted to inform external logic that the DRC has begun an access. $\overline{DTACK}$ is asserted to terminate the access. An input signal, $\overline{WAITIN}$, is provided to allow the user to add wait states dynamically during the access.

$\overline{GRANT}$ mimics the operation of $\overline{RAS}$ during an access. Like $\overline{RAS}$, it is asserted synchronous to CLK in Mode 0 and asynchronous to CLK in Mode 1 and remains active until $\overline{RAS}$ is negated. In case of a page miss, both $\overline{GRANT}$ and $\overline{RAS}$ will remain negated for at least 1T so that $\overline{GRANT}$ may be sampled by external circuitry to determine if a page miss has occured. $\overline{GRANT}$ is deasserted during refresh operations.

When programmed for Page Mode operation, $\overline{GRANT}$ will remain asserted for two rising edges of CLK after $\overline{ADS}$ is asserted while the DRC is arbitrating between the access and the 5th internal refresh request (See Automatic Internal Burst Refreshing).

$\overline{DTACK}$ may be programmed (via R7) to be asserted on the rising or falling CLK edge. The number of CLK edges that $\overline{DTACK}$ is delayed, is programmable. $\overline{DTACK}$ is controlled by programming bits R2 and R3 for any access during which $\overline{RAS}$ is initially asserted (i.e. single accesses, page misses, etc). Programming bits R4 and R5 control $\overline{DTACK}$ during page hits and while bursting.

Figures 15 and 16 show how $\overline{DTACK}$ behaves in Mode 0 and 1 accesses during which $\overline{RAS}$ is initially asserted. Figures 17 and 18 shows how $\overline{DTACK}$ behaves during page hits.

Figure 14. 2-Way Interleaved Access Mode Operation ($\overline{ECAS0}$ = 1 Programmed)

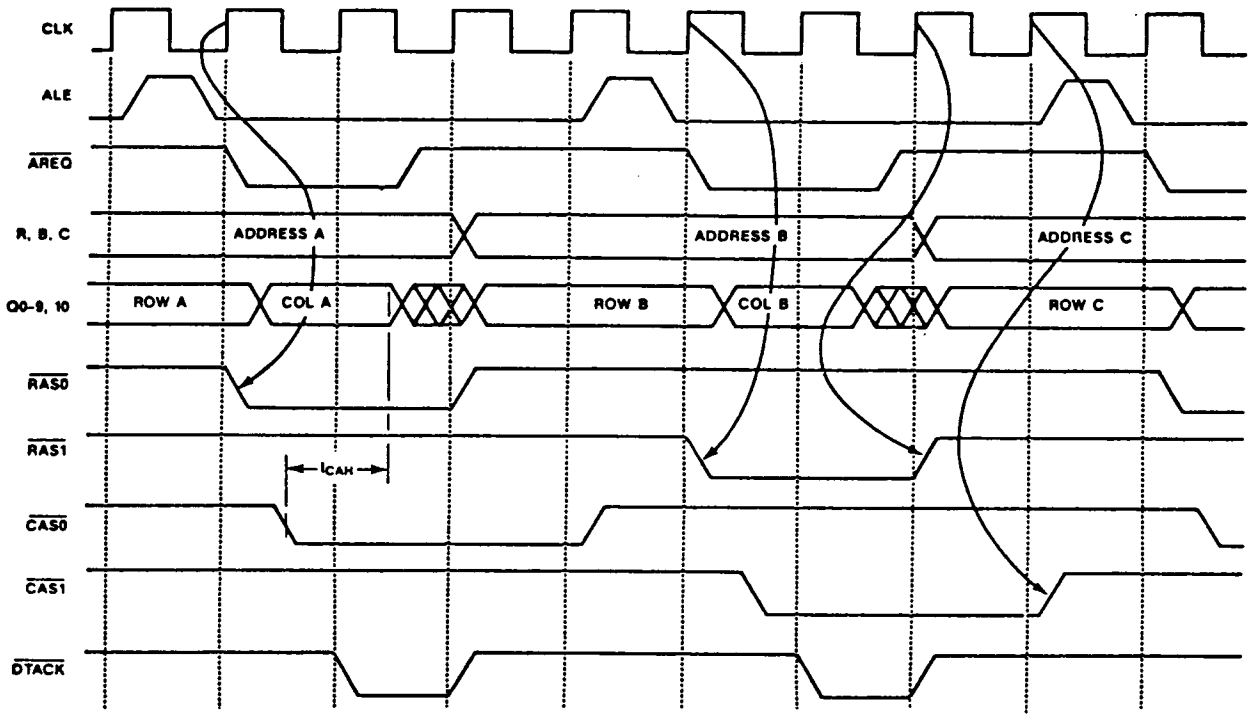


Figure 15. $\overline{DTACK}$ During Mode 0 Accesses, $\overline{RAS}$ Initially Asserted

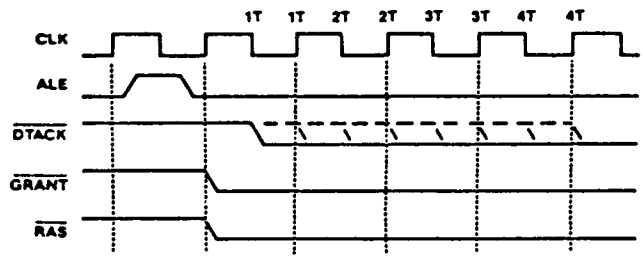


Figure 16. $\overline{DTACK}$ During Mode 1 Accesses, $\overline{RAS}$ Initially Asserted

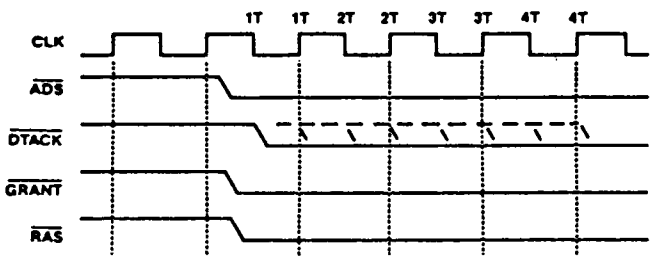


Figure 17. $\overline{DTACK}$ During Mode 0 Page Hits

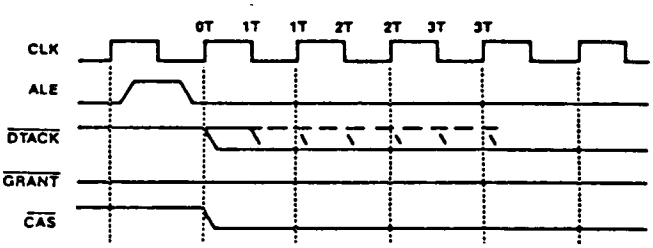
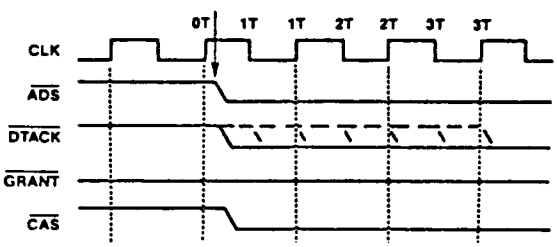


Figure 18. $\overline{DTACK}$ During Mode 1 Page Hits



When used in 68040 Burst Mode or 68030 Burst Mode, the DRC should not be programmed for 0T operation for page hits and subsequent burst cycles. This will not impact memory performance, since the opening cycle of a burst access would be expected to have at least one wait state. Regardless of when $\overline{DTACK}$ is asserted, it is always negated on the next rising CLK edge in both burst modes, as shown in Figures 19 and 20.

Figure 19. $\overline{DTACK}$ While Bursting 68040 In Burst Mode

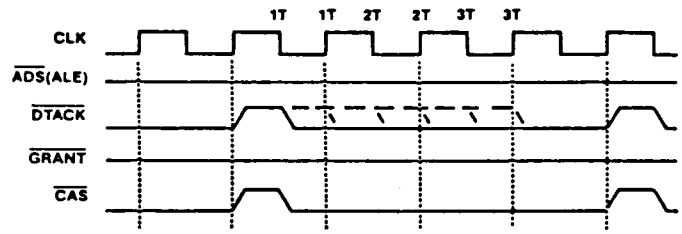
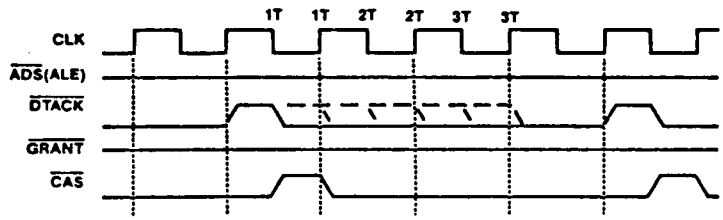


Figure 20. $\overline{DTACK}$ While Bursting In 68030 Burst Mode



Any access may be extended on the fly by asserting the $\overline{WAITIN}$ input. If R6 = 0 during programming, $\overline{WAITIN}$ is used to add one wait state during the access as shown in Figure 21. $\overline{WAITIN}$ is sampled once during the access, when $\overline{DTACK}$ is to be asserted by the DRC. $\overline{DTACK}$ will remain negated for one more rising CLK edge if $\overline{DTACK}$ is rising edge triggered or one more falling CLK edge if $\overline{DTACK}$ is falling edge trigered. $\overline{WAITIN}$ will not be sampled again, until the next access.

If R6 = 1 during programming, $\overline{WAITIN}$ may be used to defer $\overline{DTACK}$ indefinitely as shown in Figure 22. $\overline{WAITIN}$ is first sampled on:

- The falling edge of $\overline{ADS}$ (Mode 1)
- The first rising edge of CLK after ALE is pulsed high (Mode 0)
- The CLK edge that negates $\overline{DTACK}$ while bursting

If the access start is deferred due to $\overline{RAS}$ precharge, page hit writes or burst writes $\overline{WAITIN}$ is sampled again on:

- The rising edge of CLK that asserts $\overline{RAS}$ during a deferred access
- The rising edge of CLK that asserts $\overline{CAS}$ if $\overline{CAS}$ is delayed during page hit writes (C9 = 1 programmed)
- The next rising CLK edge after the CLK edge that negates $\overline{DTACK}$ during burst writes (C9 = 1 programmed)

The status of $\overline{WAITIN}$ when it was last sampled takes precedence for that access.

If $\overline{WAITIN}$ is inactive, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges. If $\overline{WAITIN}$ was active, the $\overline{DTACK}$ CLK edge count is deferred. $\overline{WAITIN}$ will be continually sampled on the rising edge of CLK if $\overline{DTACK}$ is rising edge triggered or on the falling edge of CLK if $\overline{DTACK}$ is falling edge triggered. Once $\overline{WAITIN}$ is negated, the DRC will assert $\overline{DTACK}$ after the programmed number of CLK edges and will not sample $\overline{WAITIN}$ again until the next access.

Programming bit R6 also determines when the column address is incremented in both burst modes. If R6 = 0 during programming, the column address is incremented when $\overline{CAS}$ is negated. If R6 = 1 during programming, the column address is incremented when $\overline{DTACK}$ is asserted.

Figure 21 shows a 68030 Burst Mode burst cycle. The DRC has been programmed to assert $\overline{DTACK}$ on the second falling CLK edge after $\overline{CAS}$ is asserted. $\overline{DTACK}$ was held negated for 1 extra CLK period due to $\overline{WAITIN}$. Since R6 = 0, the column address is incremented when $\overline{CAS}$ is negated.

Figure 21. $\overline{\text{WAITIN}}$, R6 = 0 Programmed

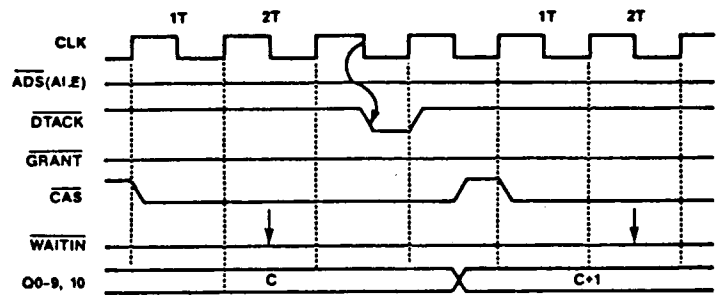


Figure 22 shows two 68040 Burst Mode burst cycles. The DRC has been programmed to assert $\overline{\text{DTACK}}$ on the first rising CLK edge after $\overline{\text{CAS}}$ is asserted. In the first cycle, $\overline{\text{WAITIN}}$ was sampled active on the clock edge that negated $\overline{\text{DTACK}}$. $\overline{\text{DTACK}}$ is rising edge triggered, so $\overline{\text{WAITIN}}$ is continually sampled on rising CLK edges until it is negated. Since the DRC was programmed to assert $\overline{\text{DTACK}}$ one rising CLK edge after $\overline{\text{CAS}}$ was asserted, $\overline{\text{DTACK}}$ is asserted one rising CLK edge after $\overline{\text{WAITIN}}$ is negated. Since $\overline{\text{WAITIN}}$ is negated during the second burst cycle, $\overline{\text{DTACK}}$ is asserted on the first rising CLK edge after $\overline{\text{CAS}}$ is asserted.

Since R6 = 1, the column address is incremented when $\overline{\text{DTACK}}$ is asserted.

Figures 23 through 25 show when $\overline{\text{WAITIN}}$ is sampled during deferred accesses, page hit writes, and burst writes, respectively.

Figure 22. $\overline{\text{WAITIN}}$, R6 = 1 Programmed

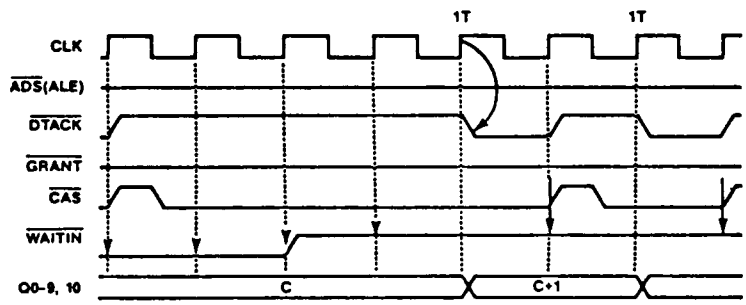


Figure 23. $\overline{\text{WAITIN}}$, R6 = 1 During Programming, Deferred Access Start

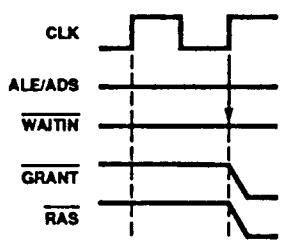


Figure 24. $\overline{\text{WAITIN}}$, R6 = 1 During Programming, Delay $\overline{\text{CAS}}$ During Page Hit Writes

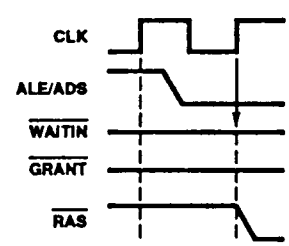
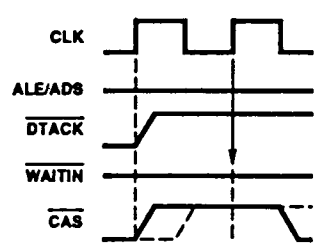


Figure 25. $\overline{\text{WAITIN}}$, R6 = 1 During Programming, Delay $\overline{\text{CAS}}$ During Burst Writes



REFRESH OPERATIONS

The DRC supports four refresh control mode options:

1) internal automatic refreshing

2) internal automatic burst refreshing

3) externally controlled/burst refreshing

4) refresh request/acknowledge burst refreshing

With each of the control modes above, $\overline{RAS}$ only refresh, or error scrubbing with $\overline{RAS}$ only refresh may be performed.

Three inputs, extend refresh (EXTDRF), refresh ($\overline{RFSH}$) and disable refresh ($\overline{DISRFSH}$), along with two outputs, refresh in progress ($\overline{RFIP}$) and refresh request ($\overline{RFRQ}$) are associated with refreshing.

$\overline{DISRFSH}$ and $\overline{RFSH}$ are used in the externally controlled/burst refresh mode and the refresh request/acknowledge mode. External circuitry asserts $\overline{DISRFSH}$ to inhibit internally requested refreshes and requests refreshes by asserting $\overline{RFSH}$.

$\overline{RFRQ}$ is used in the refresh request/acknowledge mode. The DRC asserts $\overline{RFRQ}$ to request a refresh cycle but will not perform the refresh until external circuitry acknowledges the request by asserting $\overline{RFSH}$ as long as $\overline{DISRFSH}$ is asserted.

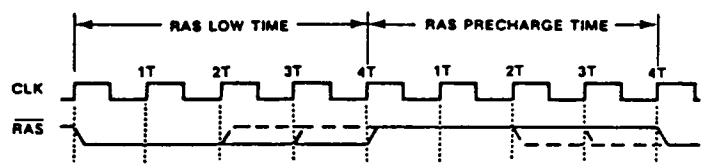
$\overline{RFIP}$ is used in all refresh modes. The DRC asserts $\overline{RFIP}$ to indicate to external circuitry that a refresh is in progress.

EXTDRF is used when the DRC is programmed for error scrubbing. External circuitry asserts EXTDRF to extend the refresh cycle.

The internal refresh row counter will be incremented automatically, regardless of the refresh control mode used. The refresh address counter will be incremented once all of the refresh RASs have been negated. The refresh counter may be reset by asserting $\overline{RFSH}$ while $\overline{DISRFSH}$ is high.

In every combination of refresh control mode and type, the DRC will assert the refresh RASs for a programmed number of CLK periods. CLK edges for $\overline{RAS}$ low time during refresh and $\overline{RAS}$ precharge time are counted as shown in Figure 26.

Figure 26. $\overline{RAS}$ Low and Precharge Time



REFRESH CONTROL MODES

Automatic Internal Refresh

The DRC has an internal refresh clock to generate internal refresh requests. An internal refresh request is generated every period of the refresh clock. $\overline{RFRQ}$ is pulsed once every period of the refresh clock. The refresh clock period is programmed according to the value of address bits C0-C3. The internal refresh request will generate an automatic internal refresh as long as a DRAM access is not currently in progress and the $\overline{RAS}$ precharge time has been met. If a DRAM access is in progress when the refresh timer requests a refresh, the on-chip arbitration logic will allow the access to finish before the refresh is initiated. The next DRAM access is deferred until the refresh cycle is complete.

The refresh period for most DRAMs is 15 µs. This means that a 1 Mbit DRAM has to be refreshed every 8 ms, during which time, 512 rows must be accessed. This requires a 9-bit row address refresh counter. The KS84EC30 has a 10-bit counter and the KS84C32, an 11-bit counter. The extra bits are used for error scrubbing over the entire address range.

Automatic internal refresh is possible in Single Access, Interleaved Access and both burst modes. When the DRC is operated in Page Mode or either burst mode with Page Mode, an enhanced version of automatic internal refreshing is available as shown in the next section.

$\overline{DISRFSH}$ must be negated to enable automatic internal refreshes.

Automatic Internal Burst Refreshing

The $\overline{RAS}$ pulse width, t_{RASP} and t_{RASC}, of most page and static column DRAMs is limited to 100 µs. The DRC takes advantage of this characteristic by supporting automatic internal burst refreshing. When operating in automatic internal burst refresh control mode, the DRC will perform a 5-refresh burst after the 5th internal refresh request (approximately every 75 µs) instead of performing a refresh after every internal request, as in the automatic internal refresh control mode.

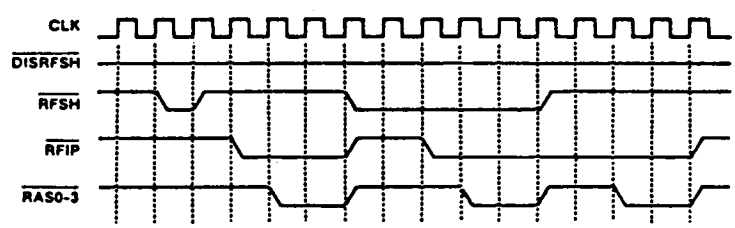
$\overline{DISRFSH}$ must be negated to enable automatic internal burst refreshes. However, if $\overline{DISRFSH}$ is asserted for any reason, all pending refreshes (up to 5) will be performed when $\overline{DISRFSH}$ is again negated. While $\overline{DISRFSH}$ is asserted, no internal refresh requests will accumulate.

Externally Controlled/Burst Refresh

When using externally controlled/burst refresh, internally generated refresh requests are ignored. Instead, external circuitry is used to pulse the refresh ($\overline{RFSH}$) signal low to generate a refresh request. The refresh cycle will take place on the next positive edge of CLK. If a DRAM access is in progress or the $\overline{RAS}$ precharge time has not been satisfied, the refresh will be delayed. This means that the access $\overline{RAS}$ must be negated with DISPM if $\overline{ECAS2}$ = 1 is programmed in order to precharge $\overline{RAS}$ before the refresh can take place. If $\overline{RFSH}$ is asserted when the refresh $\overline{RAS}$ is negated, $\overline{RFIP}$ will remain asserted and another refresh cycle will be performed after $\overline{RAS}$ has been precharged.

Figure 27 shows how $\overline{DISRFSH}$ and $\overline{RFSH}$ are used to control single and burst refreshes. The DRC is performing a $\overline{RAS}$ only refresh under external control and has been programmed to assert the refresh $\overline{RAS}$ for 2T and to precharge $\overline{RAS}$ for 2T.

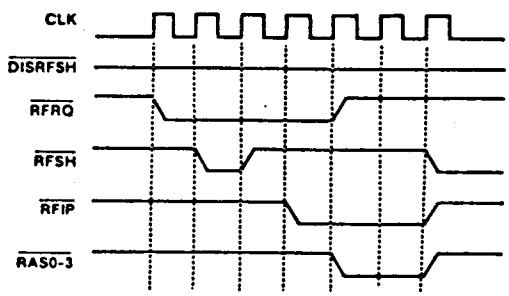
Figure 27. Externally Controlled/Burst Refresh



Refresh Request/Acknowledge Burst Refreshing

In this refresh control mode, internally generated refresh requests are ignored by the DRC. Instead, external circuitry monitors the the DRC's $\overline{RFRQ}$ output and generates a refresh request at the appropriate time by pulsing $\overline{RFSH}$. The refresh is then performed as shown in Figure 28.

Figure 28. Refresh Request/Acknowledge Refresh



REFRESH TYPES

The DRC supports two types of refreshing:

1) $\overline{RAS}$ only

2) $\overline{RAS}$ only with Error Scrubbing

Each refreshing type may be controlled by any refresh control mode. The DRC asserts all RASs at the same time when performing $\overline{RAS}$ only refreshing as shown in Figure 27.

$\overline{RAS}$ and $\overline{CAS}$ are asserted during refresh when Error Scrubbing refresh is programmed as shown in Figure 48. *The $\overline{ECAS}$ inputs do not enable or disable $\overline{CAS}$ during the refresh. The EDAC circuit should control the DRAMs' output enable lines to avoid bus contention if the DRAM has common I/O.*

RESET

The KS84EC30 on-chip power-up reset logic generates a reset pulse:

- At power up
- If V_{CC} falls well below 3V and reaches V_{CC} min.

When the chip is reset, the Mode Register (with the exception of bit C6, which is set) and all internal counters are reset. All of the output signals are inactive; $\overline{RAS0\text{-}3}$, $\overline{CAS0\text{-}3}$, $\overline{DTACK}$, $\overline{RFIP}$, $\overline{WE}$, $\overline{RFRQ}$ and $\overline{GRANT}$ are high while Q0-9 are low.

After power-up, the DRC is operable after 200 µs and the Mode Register can be programmed if the programmable version of the chip is being used.

The Mode Load signal ($\overline{ML}$) can be used to reset the chip at any time after power-up. When $\overline{ML}$ is driven low, all internal counters are reset and the Mode Register is enabled to receive the mode bit inputs.

The internal refresh interval counter may be reset at any time by asserting $\overline{RFSH}$ while $\overline{DISRFSH}$ is high.

PROGRAMMING THE KS84EC30

The KS84EC30 has a Mode Register that is programmed by the user. The Mode Register controls the internal operating modes of the DRC.

The DRC is programmed via the system's address bus, not the data bus. The Mode Register receives inputs from the CPU on address lines R0-9 and C0-9, the bank select lines B0 and B1, and the $\overline{CAS}$ enable lines $\overline{ECAS0\text{-}3}$. The Mode Register is enabled by the falling edge of $\overline{ML}$. The inputs are then strobed in on the rising edge of $\overline{ML}$ as show in Figure 29.

Alternatively, the Mode Register may be programmed by initiating a "fake" access as shown in Figure 30. When programmed in this fashion, $\overline{ML}$ and $\overline{CS}$ are asserted, followed by $\overline{AREQ}$. The programming inputs are strobed into the Moad Load Register on the falling edge of $\overline{AREQ}$. $\overline{DTACK}$ is asserted on the falling edge of $\overline{AREQ}$ to terminate the bus access and is negated by the rising edge of $\overline{ML}$ or $\overline{AREQ}$ (whichever occurs first).

Figure 29. Mode Load Only Programming

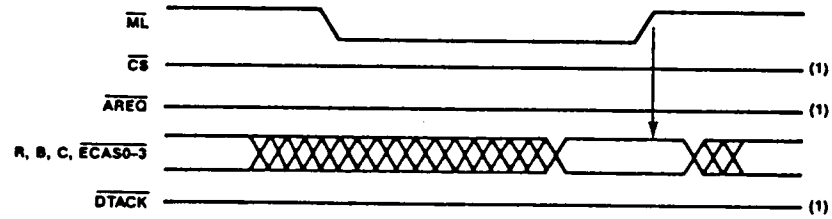


Figure 30. Fake Access Programming

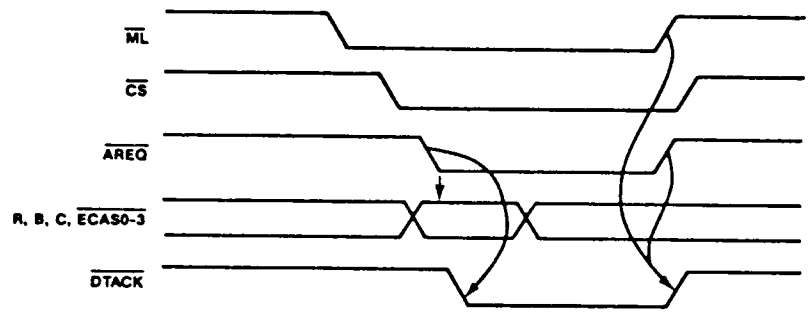


Table 3. Programming the Mode Register

OPERATING MODES

$\overline{ECAS1}$-$\overline{3}$

These bits program the DRCs operating mode. The user has the choice of Single Access Mode, Interleaved Access Mode, Page Access Mode, 68040 Burst Access Mode with or without Page Mode or 68030 Burst Access Mode with or without Page Mode. Interleaved Access Mode is selected by the $\overline{RAS}$ and $\overline{CAS}$ configuration bits C4, C5, and C6.

$\overline{ECAS1}$	$\overline{ECAS2}$	$\overline{ECAS3}$	Operating Mode
0	0	0	Single Access Mode
0	1	0	Page Access Mode
0	0	1	68040 Burst Access Mode
0	1	1	68040 Burst Access Mode with Page Mode
1	0	0	68030 Burst Access Mode
1	1	0	68030 Burst Access Mode with Page Mode

ADDRESS LATCH/AUTOMATIC COLUMN INCREMENT WHILE BURSTING

B0

B0 allows the user to specify whether the on-chip latches should latch the address inputs on the falling edge of $\overline{ADS}$(ALE) or whether they should remain tranparent. If $\overline{ECAS2}$ = 1 during programming the row address is always latched by the on-chip page detect logic regardless of how B0 is programmed.

The user also specifies whether the DRC automatically increments the column address while bursting or if external circuitry is required to change the column address. If B0 = 0 during programming, then the column address is automatically incremented while bursting. If B0 = 1, the address latches will remain tranparent, disabling the automatic column increment.

B0		Automatic Column Increment
0	Address Bits Latched	Enabled
1	Address Latches Transparent	Disabled

ACCESS START AND TERMINATION MODES

B1

B1 allows the user to specify either synchronous or asynchronous access start and termination modes.

A synchronous (Mode 0) access is controlled by the system clock. The access is initiated on the first rising CLK edge after ALE goes high. $\overline{AREQ}$ is sampled on rising CLK edges and terminates the access when it is negated.

An asynchronous (Mode1) access is initiated immediately by the falling edge of $\overline{ADS}$ and is immediately terminated by the rising edge of $\overline{AREQ}$.

B1	
0	Mode 0
1	Mode 1

Table 3. Programming the Mode Register (Continued)

$\overline{RAS}$ LOW AND $\overline{RAS}$ PRECHARGE TIME

R0, R1

These bits control the time that $\overline{RAS}$ is low during refresh operations and also determine the $\overline{RAS}$ precharge time. The time interval shown (T) is equivalent to one rising CLK edge. The user should take into account $\overline{RAS}$ rise and fall time when programming these bits.

R0	R1	$\overline{RAS}$ Low Time	$\overline{RAS}$ Precharge Time
0	0	2T	2T
0	1	2T	3T
1	0	3T	3T
1	1	4T	4T

$\overline{DTACK}$ GENERATION FOR ACCESSES THAT INITIALY ASSERT $\overline{RAS}$

R2, R3

These bits control $\overline{DTACK}$ generation for any access during which $\overline{RAS}$ is initiated. R2 and R3 determine the number of CLK edges that $\overline{DTACK}$ remains negated under the following conditions:

- All accesses when the DRC is programmed for Single or Interleaved Access Modes
- During page misses and deferred accesses when the DRC is programmed for Page Mode
- During the opening cycle of a burst access when the DRC is programmed for 68040 Burst or 68030 Burst Access Modes or if a page miss occurs during the opening access when they are combined with Page Mode.

The time interval shown (T) refers to one rising or falling CLK edge. Bit R7 determines whether $\overline{DTACK}$ is asserted on rising or falling CLK edges.

R2	R3	$\overline{DTACK}$ Low From Access Start
0	0	1T
0	1	2T
1	0	3T
1	1	4T

$\overline{DTACK}$ GENERATION FOR PAGE HITS AND BURST ACCESSES

R4, R5

These bits control $\overline{DTACK}$ generation for any access during which only $\overline{CAS}$ is initiated. R4 and R5 determine the number of CLK edges that $\overline{DTACK}$ remains negated under the following conditions:

- During page hits when the DRC is programmed for Page Mode
- During the opening cycle of a burst access that results in a page hit when the DRC is programmed for 68040 Burst or 68030 Burst Access Modes and Page Mode is used.
- While Bursting

The time interval shown (T) refers to one rising or falling CLK edge. Bit R7 determines whether $\overline{DTACK}$ is asserted on rising or falling CLK edges.

R4	R5	$\overline{DTACK}$ Low From Access Start
0	0	0T
0	1	1T
1	0	2T
1	1	3T

Table 3. Programming the Mode Register (Continued).

PROGRAMMING $\overline{\text{WAITIN}}$ FOR WAIT STATE INSERTION AND COLUMN INCREMENT

R6 controls the functionality of $\overline{\text{WAITIN}}$ in all operating modes. It also determines when the column address will be incremented when the DRC is operated in 68040 Burst and 68030 Burst Modes.

R6	$\overline{\text{WAITIN}}$ Functionality	Column Address Increment
0	Add 1 wait state if active.	Increment when $\overline{\text{CAS}}$ is negated
1	Continually add wait states.	Increment when $\overline{\text{DTACK}}$ is asserted

PROGRAMMING $\overline{\text{DTACK}}$ FOR RISING OR FALLING CLK EDGES

R7 — This bit controls whether $\overline{\text{DTACK}}$ is asserted (and $\overline{\text{WAITIN}}$ is sampled) on rising or falling CLK edges.

R7	$\overline{\text{DTACK}}$
0	Rising Edge Triggered
1	Falling Edge Triggered

INTERLEAVING

R8 determines whether the Q outputs are driven in interleaved or non-interleaved mode.

In interleaved mode, the row addresses are multiplexed to the DRAM controller address outputs, after the column addresses have been held for a sufficient time (25ns minimum) after $\overline{\text{CAS}}$ has gone low.

In non-interleaved mode, the column addresses are held on the DRAM controller address outputs until $\overline{\text{CAS}}$ goes high.

R8	
0	Interleaved mode
1	Non-interleaved mode

RESERVED BIT

R9 — This bit should be programmed = 0. If programmed = 1, Error Scrubbing is not supported.

RFCLK DIVISOR

C0, C1, C2 — These bits allow the user to select the divisor for the refresh clock (RFCLK) input, from which the internal refresh clock is generated. Select the divisor such that the internal refresh clock frequency is approximately 2 MHz.

C0	C1	C2	Divisor
0	0	0	10
0	0	1	6
0	1	0	8
0	1	1	4
1	0	0	9
1	0	1	5
1	1	0	7
1	1	1	3

Table 3. Programming the Mode Register (Continued)

INTERNAL REFRESH CLOCK DIVISOR

C3

C3 allows the user to divide the internal refresh clock to achieve the desired interval between internally generated refresh requests.

C3	Divisor	Refresh Interval If Internal Refresh Clock Freqency Is 2 MHz
0	30	15 μs
1	26	13 μs

$\overline{RAS}$ AND $\overline{CAS}$ CONFIGURATIONS

C4, C5, C6

These bits control the $\overline{RAS}$ and $\overline{CAS}$ configurations. There are 4 $\overline{RAS}$ and 4 $\overline{CAS}$ outputs. They can always be grouped such that each $\overline{RAS}$ and $\overline{CAS}$ will drive one fourth of the memory array, regardless of whether the array is arranged in 1, 2 or 4 banks. The setting of these bits also determines whether error scrubbing and Interleaved Access Mode are selected.

C4	C5	C6	$\overline{RAS}$ and Configuration Modes	Error Scrubbing	Interleaved Access Mode
0	0	0	$\overline{RAS0-3}$ are brought low during an access. $\overline{CAS0-3}$ are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low. B0 and B1 are not used.	Yes	No
0	0	1	$\overline{RAS}$ pairs are selected by B1. $\overline{CAS0-3}$ are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low.	No	No
0	1	0	$\overline{RAS}$, $\overline{CAS}$ pairs are selected by B0 and B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	Yes	Yes
0	1	1	$\overline{RAS}$ is selected by B0 and B1. $\overline{CAS0-3}$ are all selected during an access but only those enabled by the corresonding $\overline{ECAS}$ can go low.	No	No
1	0	0	$\overline{RAS}$, $\overline{CAS}$ pairs are selected by B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	Yes	Yes
1	0	1	$\overline{RAS}$, $\overline{CAS}$ pairs are selected by B1. A selected $\overline{CAS}$ will go low only if enabled by its corresponding $\overline{ECAS}$.	No	Yes
1	1	0	$\overline{RAS0-3}$ are brought low during an access. $\overline{CAS0-3}$ are all selected during an access but only those enabled by the corresponding $\overline{ECAS}$ can go low. B0 and B1 are not used.	No	No

For C4, C5, C6 = 0, 0, 1:

B1	B0	
0	X	$\overline{RAS0}$, 1
1	X	$\overline{RAS2}$, 3

For C4, C5, C6 = 0, 1, 0:

B1	B0	
0	0	$\overline{RAS0}$, $\overline{CAS0}$
0	1	$\overline{RAS1}$, $\overline{CAS1}$
1	0	$\overline{RAS2}$, $\overline{CAS2}$
1	1	$\overline{RAS3}$, $\overline{CAS3}$

For C4, C5, C6 = 0, 1, 1:

B1	B0	
0	0	$\overline{RAS0}$
0	1	$\overline{RAS1}$
1	0	$\overline{RAS2}$
1	1	$\overline{RAS3}$

For C4, C5, C6 = 1, 0, 0:

B1	B0	
0	X	$\overline{RAS0}$, 1 and $\overline{CAS0}$, 1
1	X	$\overline{RAS2}$, 3 and $\overline{CAS2}$, 3

For C4, C5, C6 = 1, 0, 1:

B1	B0	
0	X	$\overline{RAS0}$, 1 and $\overline{CAS0}$, 1
1	X	$\overline{RAS2}$, 3 and $\overline{CAS2}$, 3

Table 3. Programming the Mode Register (Continued)

RAS AND CAS CONFIGURATIONS (Continued)

C4	C5	C6	RAS and Configuration Modes	Error Scrubbing	Interleaved Access Mode
1	1	1	RAS pairs are selected by B0 and B1. A selected CAS will go low only if enabled by its corresponding ECAS.	No	Yes

B1	B0	
0	0	RAS0, CAS0
0	1	RAS1, CAS1
1	0	RAS2, CAS2
1	1	RAS3, CAS3

COLUMN ADDRESS SETUP TIME

C7 allows the user to specify the minimum guaranteed column address setup time (t_{ASC}).

C7	t_{ASC}
0	10 ns
1	0 ns

ROW ADDRESS HOLD TIME

C8 allows the user to specify the minimum guaranteed row address hold time (t_{RAH}).

C8	t_{RAH}
0	18 ns
1	12 ns

DELAY CAS DURING WRITE ACCESSES

C9 allows the user to delay CAS during write operations that result in page hits or that occur during a burst cycle. This option allows the user to insure that the data is valid at the DRAM before CAS is asserted. Since the CAS delay would most likely require an additional wait state during the write access, DTACK may be automatically delayed.

During Mode 1 page hits, if DELAY CAS is selected, CAS will be asserted on the first CLK rising edge after ADS is asserted. If DTACK was programmed for 0T operation, DTACK will be asserted on the same CLK rising edge that asserted CAS. If DTACK was programmed for 1T, 2T or 3T operation, the DRC will begin counting CLK edges after CAS is asserted.

During Mode 0 page hits, if DELAY CAS is selected, the assertion of both CAS and DTACK will be delayed one complete CLK period.

During burst accesses, if DELAY CAS is selected, the assertion of both CAS and DTACK will be delayed one complete CLK period.

C9	
0	No Delay
1	Delay CAS

EXTEND CAS AND SPECIFY WE OR RFRQ

ECAS0 allows the user to specify whether CAS is extended when the DRC is programmed for Single Access Mode. This option allows the user to begin precharging RAS before the access is completed. ECAS0 also specifies whether the WE(RFRQ) pin functions as Write Enable or Refresh Request

ECAS0		
0	CAS is negated by AREQ.	Specify WE
1	CAS remains asserted until the next rising CLK edge after RAS is negated.	Specify RFRQ

DC ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

DC Supply Voltage 7V
Temperature Under Bias ..... 0°C to +70°C
Storage Temperature ..... –65°C to 150°C

All Input and Output Voltage ..... V_{SS} – 0.5V to +7V
Power Dissipation at 40MHz 0.75W
E.S.D. 2000V

Note: If the device is used beyond the maximum rating, permanent damage may occur. Operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, V_{SS} = 0V)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage	Tested with limited test pattern	2.0		V_{CC}+0.5	V
V_{IL}	Input Low Voltage	Tested with limited test pattern	–0.5		0.8	V
V_{OH1}	Q and $\overline{WE}$ Outputs	I_{OH} = –3mA	2.4			V
V_{OL1}	Q and $\overline{WE}$ Outputs	I_{OL} = 10mA			0.5	V
V_{OH2}	All outputs except Q and $\overline{WE}$	I_{OH} = –1mA	2.4			V
V_{OL2}	All outputs except Q and $\overline{WE}$	I_{OL} = 3mA			0.5	V
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			±10	µA
I_{ILML}	$\overline{ML}$ Input Current	V_{IN} = V_{SS}			200	µA
I_{CC1}	Quiescent Current	CLK at 40MHz Inputs Inactive			30	mA
I_{CC2}	Supply Current	Inputs Active (I load = 0)		65	125	mA
C_{IN}	Input Capacitance	f_{IN} at 1MHz		5	10	pF

AC SWITCHING CHARACTERISTICS

Figure 31 shows a typical test circuit, while Figure 32 shows the output drive levels. Figures 34 through 53 provide switching characteristics for a number of typical KS84EC30 operations:

Unless otherwise stated V_{CC} = 4.75V to 5.25V, 0 < T_A < 70°C

Load Capacitance: 50pF

All minimum and maximum values are measured in nanoseconds.

CAPACITIVE LOAD SWITCHING

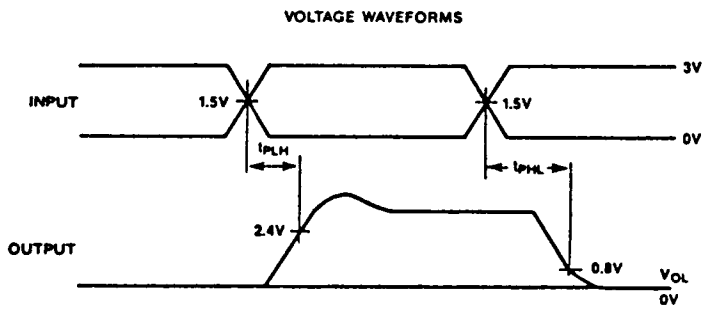
Figure 31. Switching Test Circuits

FOR Q OUTPUTS

ALL OTHER OUTPUTS

TYPICAL SWITCHING CHARACTERISTICS

Figure 32. Output Drive Levels



AC Testing inputs are driven at 3.0V for a logic "1" and 0.0V for a logic "0". Timing measurements are made at 2.4V for a logic "1" and 0.8V for a logic "0" at the outputs.

Figure 33. Simplified Output Driver Schematic

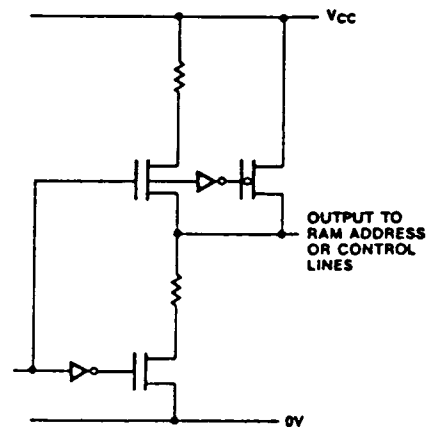


Figure 34. CLK, RFCLK Timing

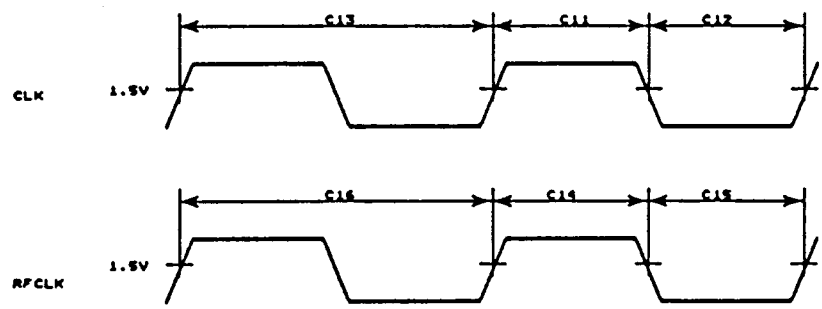


Figure 35. Single Access Mode Mode 0

MODE SETTING		
R0	0	3T 1RP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	X	
R5	X	
R6	X	
R7	0	CLK RISING EDGE
R8	0	INTERLEAVE
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
R0	0	ADDRESS LATCH
R1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	0	
ECAS3	0	

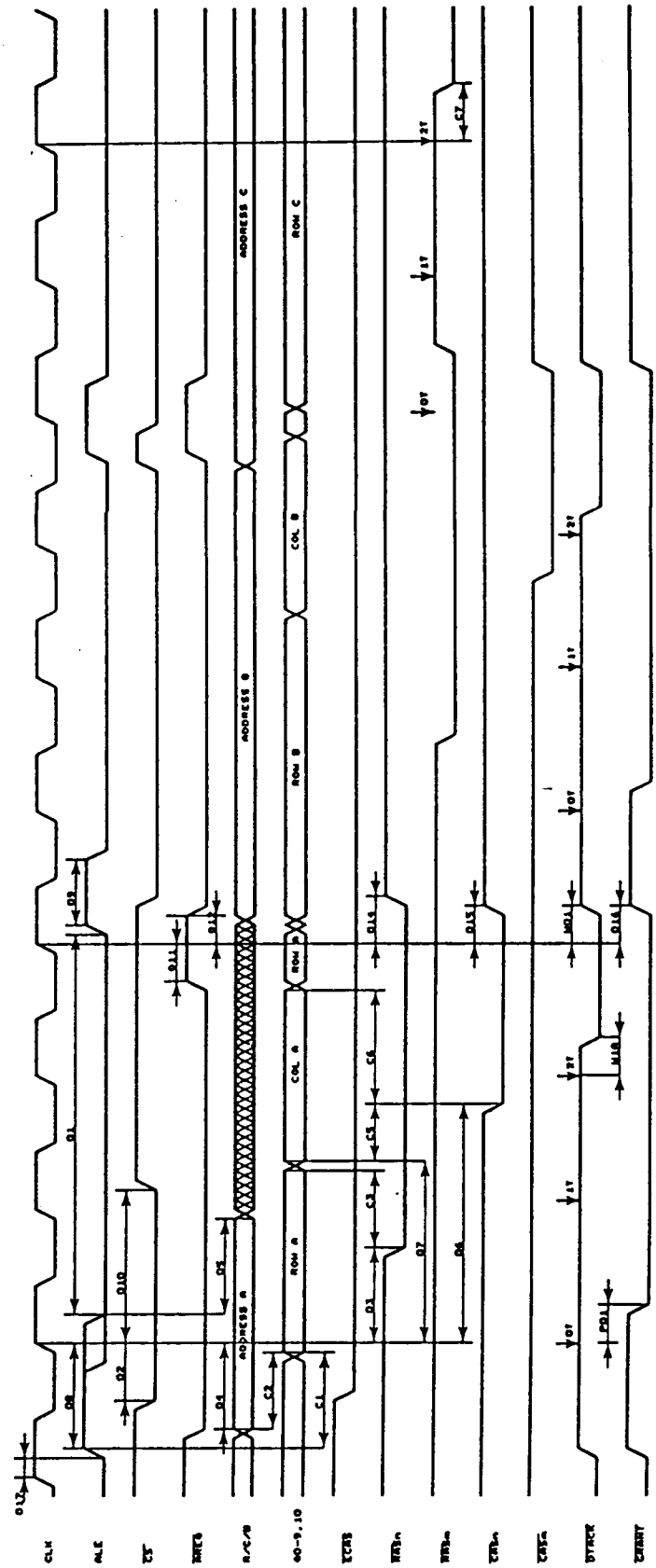


Figure 36. Single Access Mode Mode 1

MODE SETTING		
A0	0	2T LAP
A1	0	
A2	0	2T NON BURST
A3	1	
A4	X	
A5	X	
A6	X	
A7	0	CLK RISING EDGE
A8	0	INTERLEAVE
A9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	0	ADDRESS LATCH
B1	1	ASYN MODE 1
ECAS0	0/1	CAS DELAY
ECAS1	0	
ECAS2	0	
ECAS3	0	

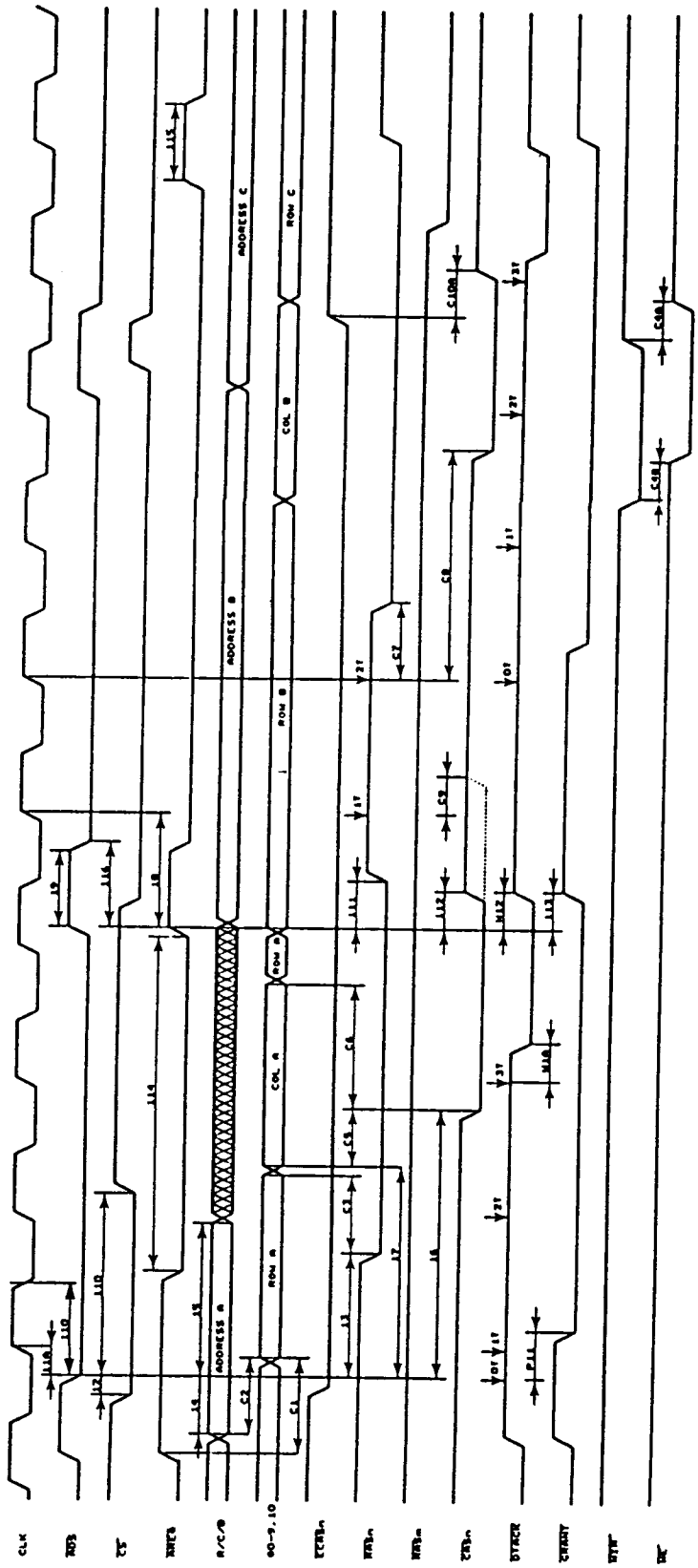


Figure 37. Page Access Mode Mode 0

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	2T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0/1	CLK RISING/FALL
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	X	
B1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	1	PAGE MODE
ECAS3	0	

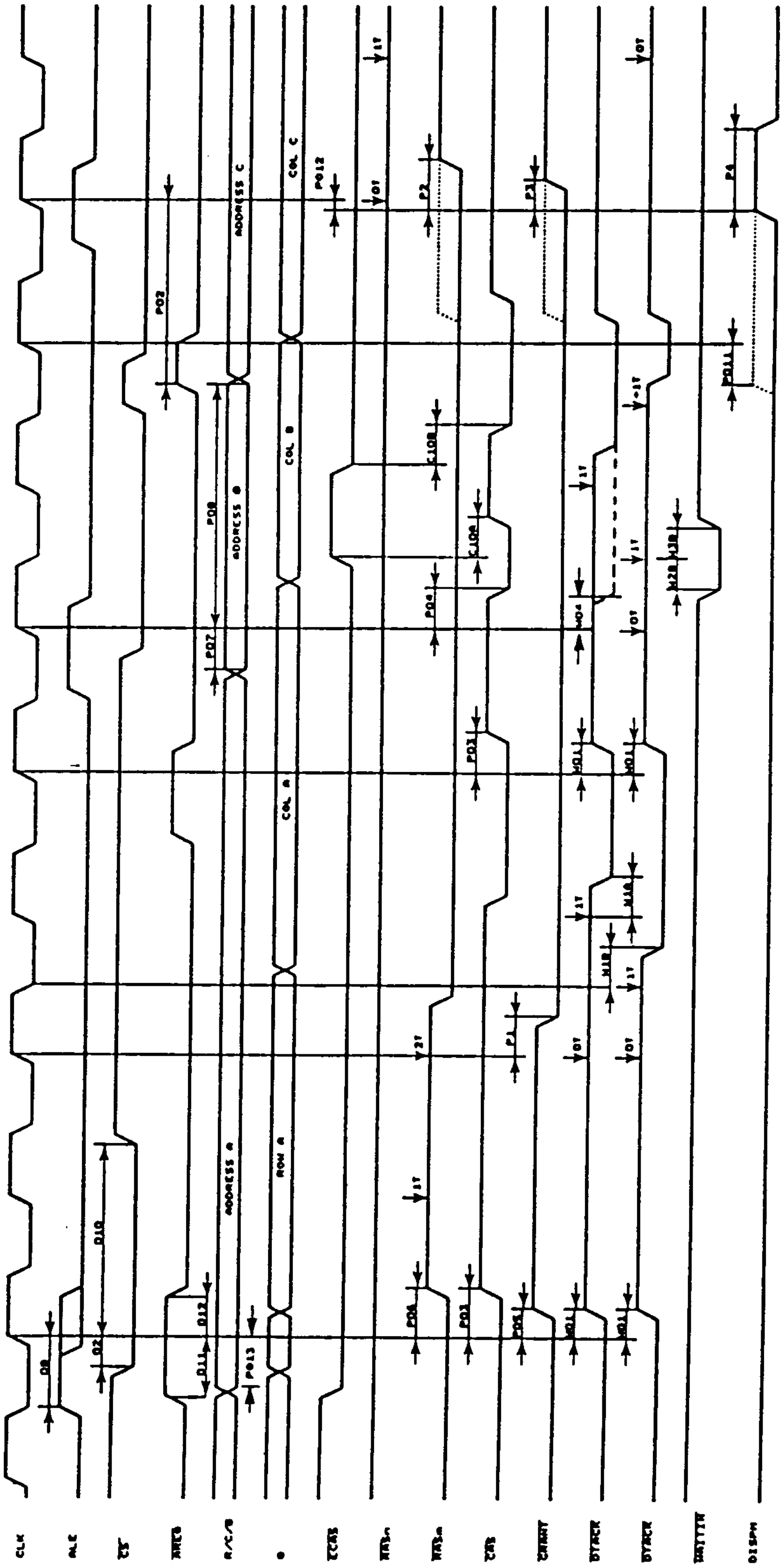


Figure 38. Page Access Mode
Mode 1

MODE SETTING		
R0	0	2T LRP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	0	1T BURST
R5	1	
R6	X	
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (MIN)
B0	X	
B1	1	ASYN MODE 1
ECAS0	0	
ECAS1	0	
ECAS2	1	PAGE MODE
ECAS3	0	

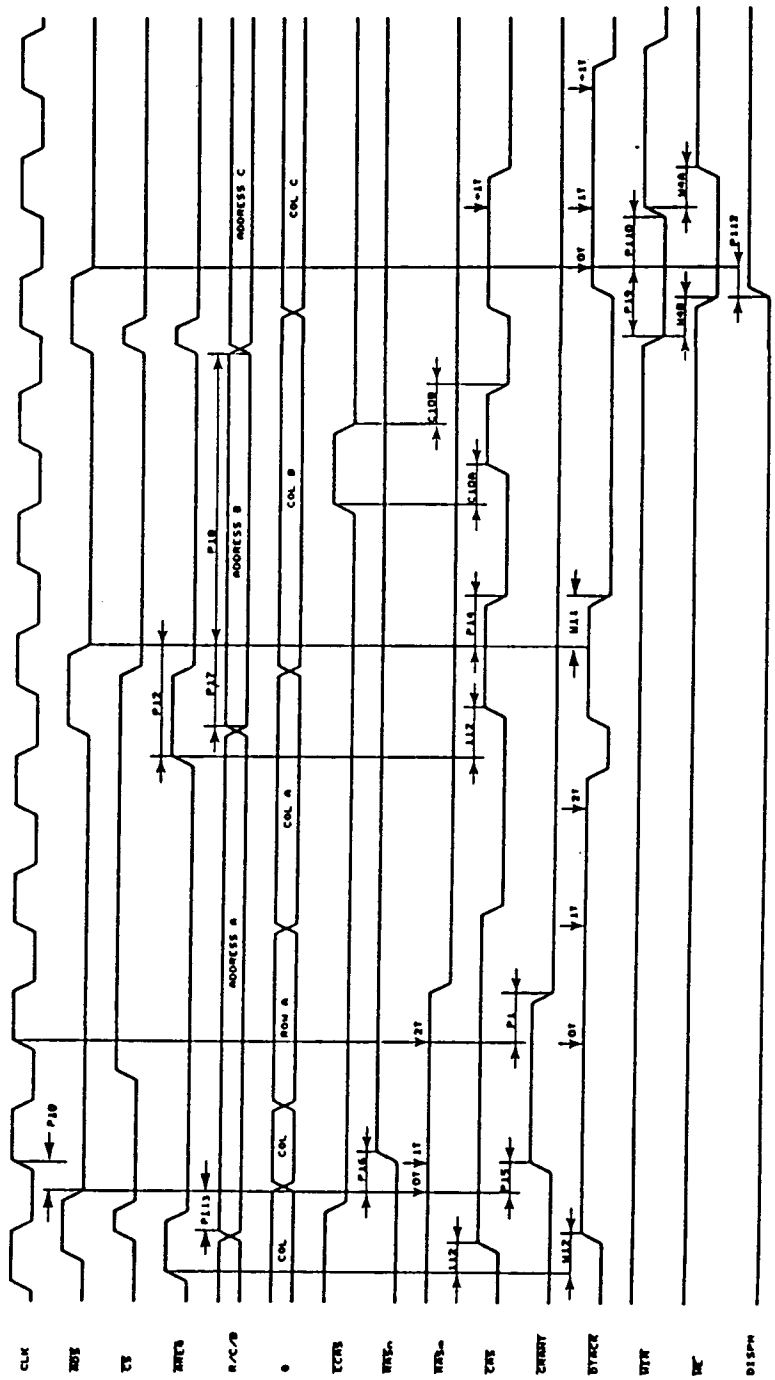


Figure 39. 68030 Burst Access Mode

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	2T NON BURST
R3	1	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
B0	X	
B1	1	ASYN MODE 1
ECAS0	0	
ECAS1	1	68030 MODE
ECAS2	0	
ECAS3	0	

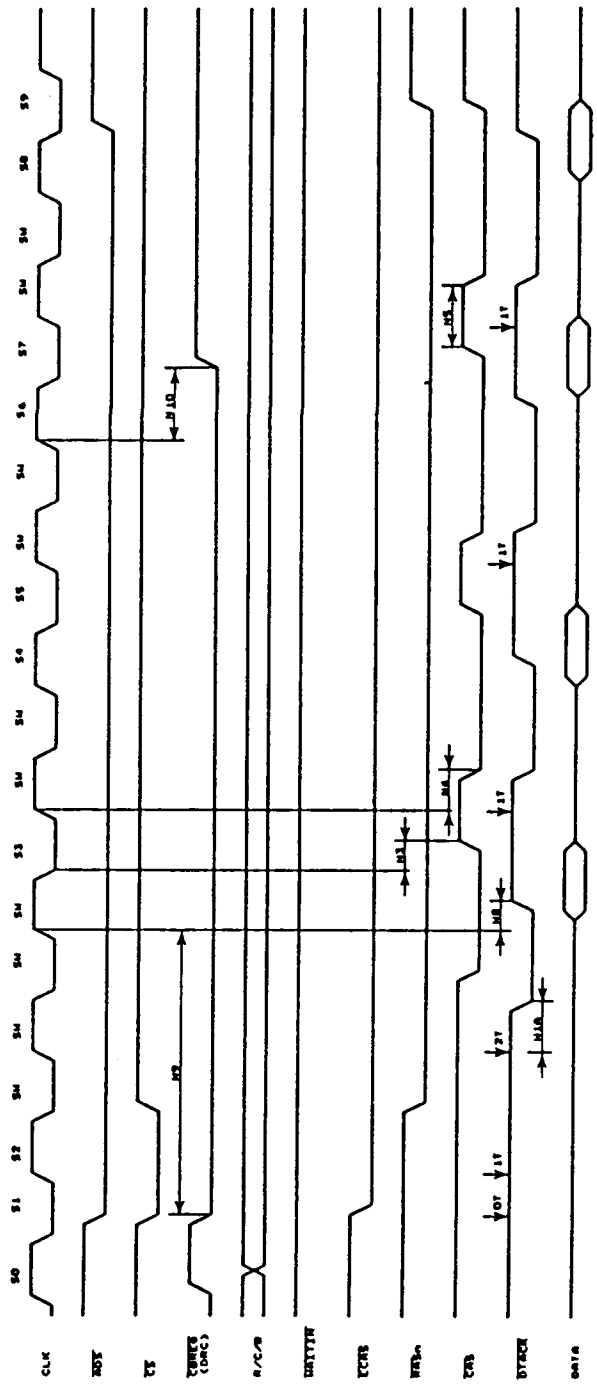


Figure 40. 68030 Burst Access Mode with Page Mode

MODE SETTING		
R0	0	2T tAP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	1	DEFER DTACK
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	X	
R0	X	
R1	1	ASYN MODE 1
FCAS0	0	
FCAS1	1	68030 MODE
FCAS2	1	PAGE MODE
FCAS3	0	

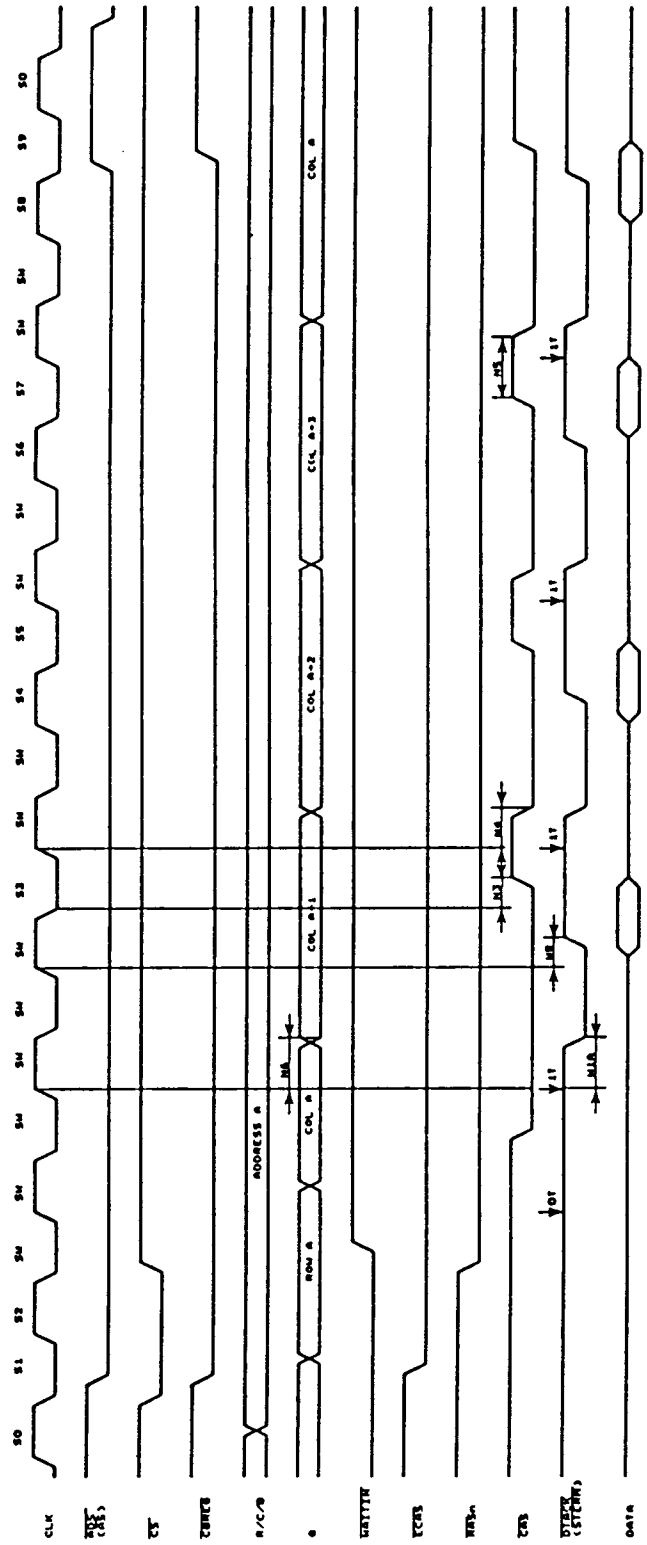


Figure 41. Burst Access Mode with Page Mode (68040, 80486)
Mode 1

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	1	DEFER DTACK
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (MIN)
R0	0	ADDRESS LATCH
R1	1	ASYN MODE 1
FCAS0	0	
FCAS1	0	
FCAS2	1	PAGE MODE
FCAS3	1	BURST MODE

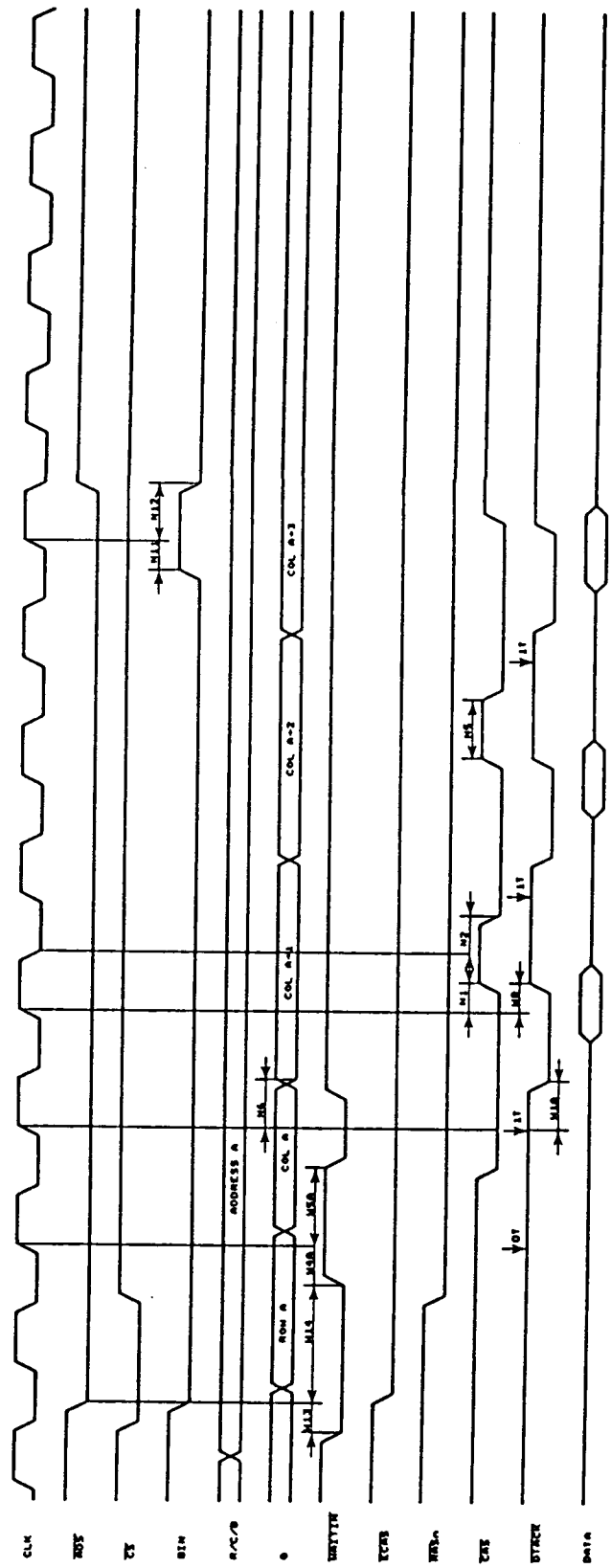


Figure 42. 68040 Burst Access Mode

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T non burst
R3	0	
R4	0	1T burst
R5	1	
R6	0	add 1T
R7	0	CLK rising edge
R8	1	non interl.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS pairs
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	delay CAS (min)
B0	0	address latch
B1	0	syn mode 0
ECAS0	0	
ECAS1	0	
ECAS2	0	
ECAS3	1	burst mode

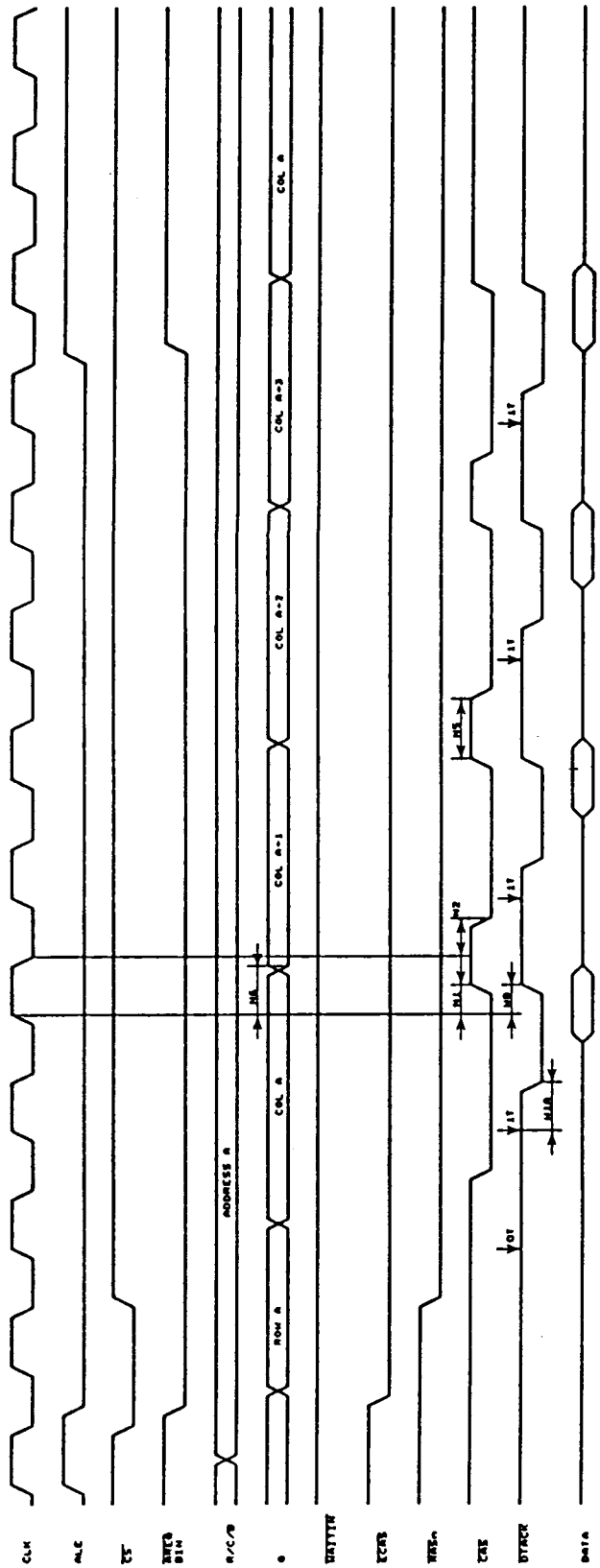


Figure 43. 68040 Burst Access Mode
Mode 0 DELAY $\overline{CAS}$ During Burst Write

MODE SETTING		
R0	0	2T tRP
R1	0	
R2	0	1T NON BURST
R3	0	
R4	0	1T BURST
R5	1	
R6	0	ADD 1T
R7	0	CLK RISING EDGE
R8	1	NON INTERL.
R9	X	
C0	X	
C1	X	
C2	X	
C3	X	
C4	0	RAS/CAS PAIRS
C5	1	
C6	0	
C7	X	
C8	X	
C9	1	DELAY CAS (WIN)
B0	0	ADDRESS LATCH
B1	0	SYN MODE 0
ECAS0	0	
ECAS1	0	
ECAS2	0	
ECAS3	1	BURST MODE

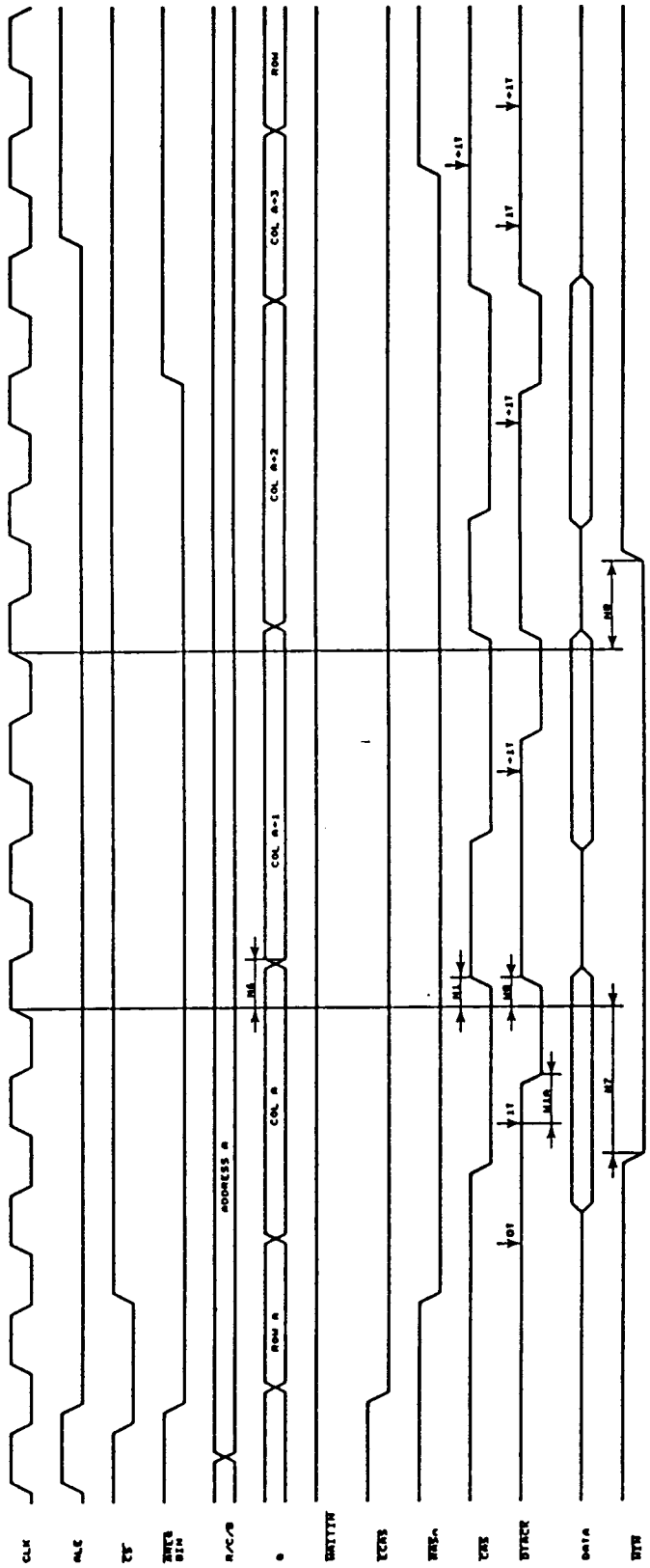


Figure 44. Mode Load by Fake Access

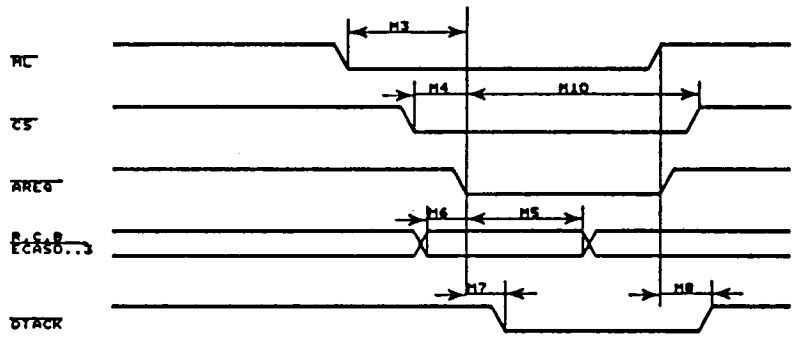


Figure 45. Mode Load Controlled by Mode Load Input Only

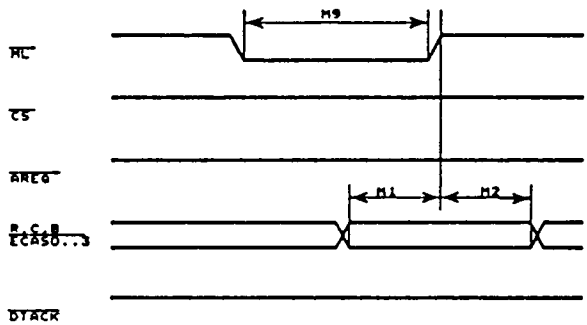


Figure 46. REFRESH, Single Access Mode Burst Mode

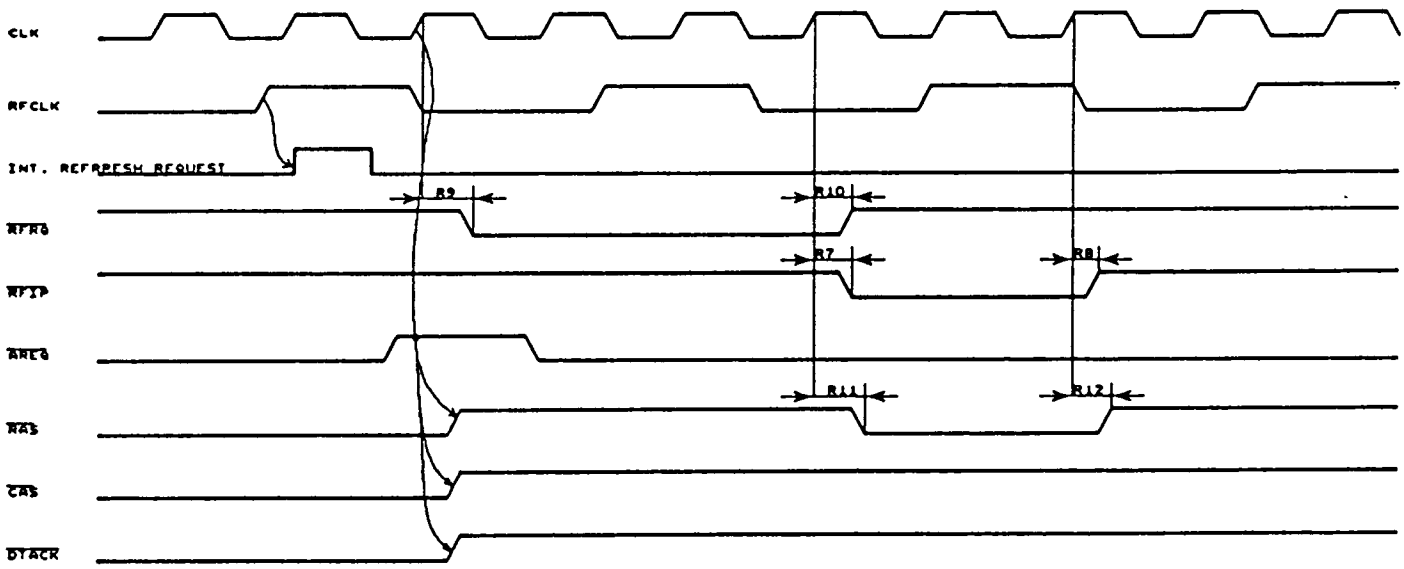


Figure 47. REFRESH in Page Mode

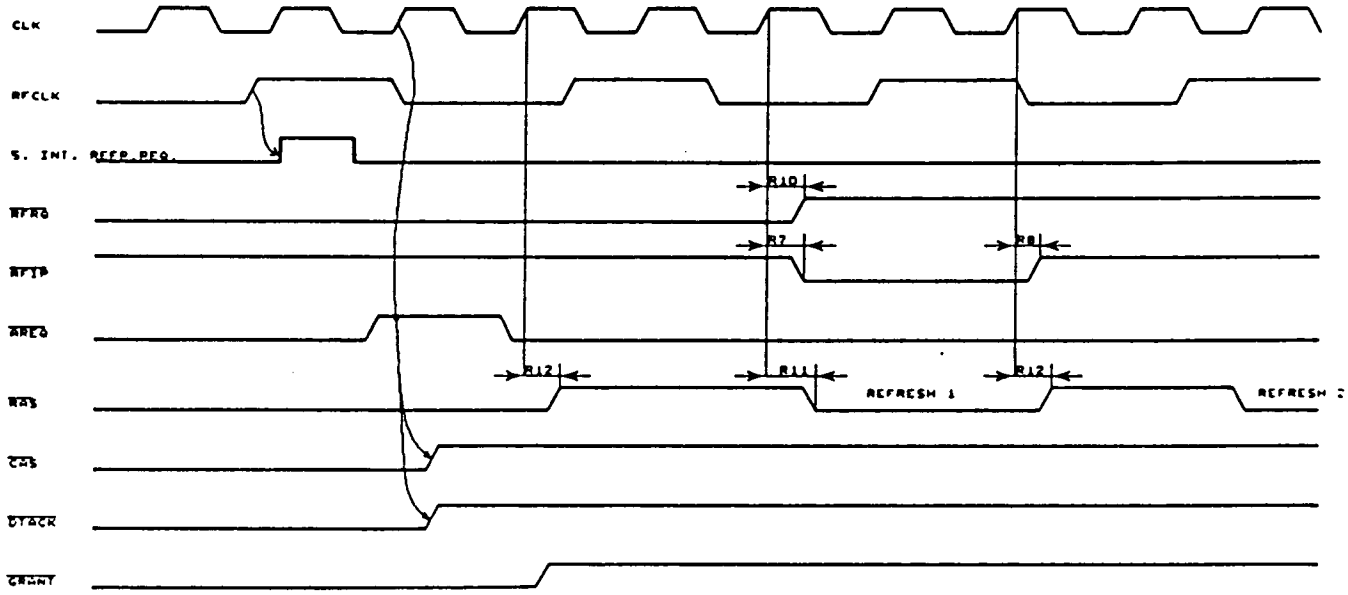


Figure 48. REFRESH with Extend Refresh

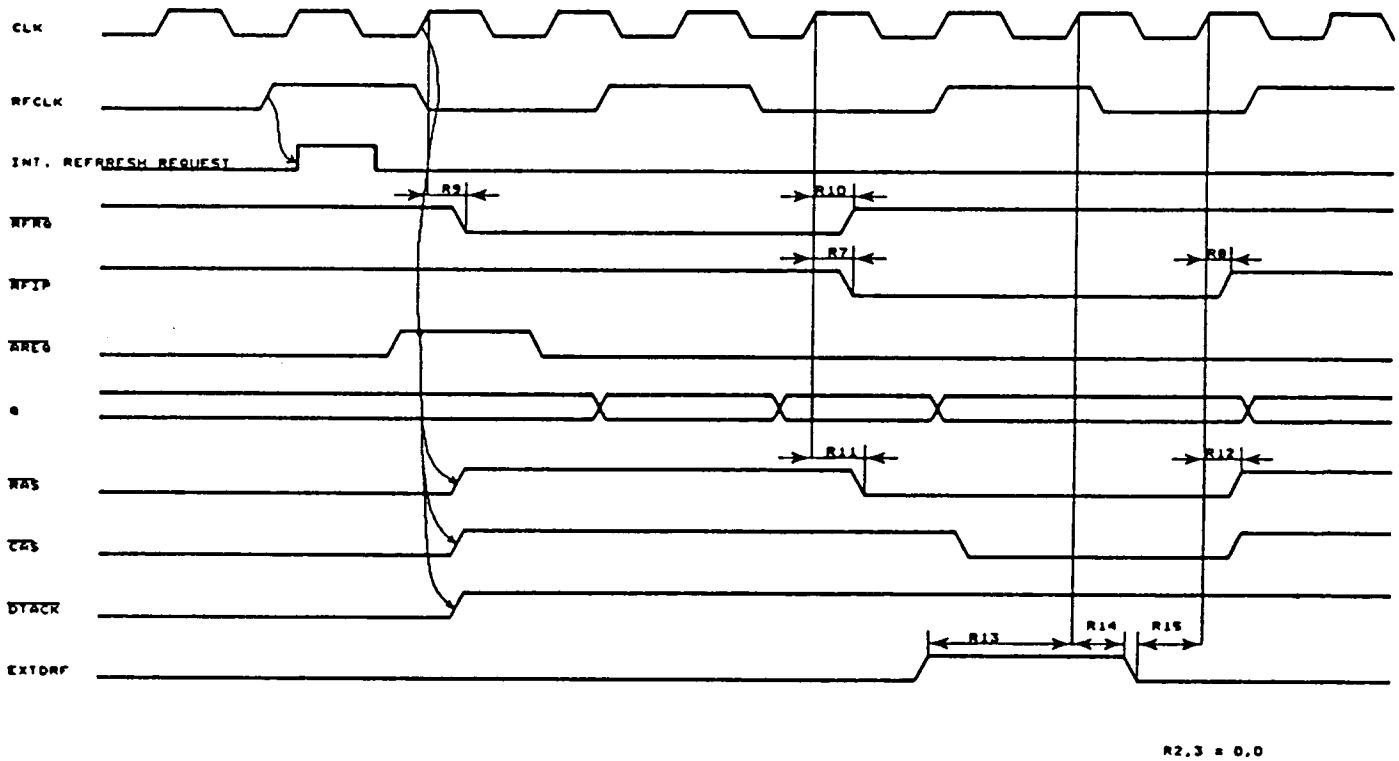


Figure 49. Page Mode REFRESH with Extend Refresh

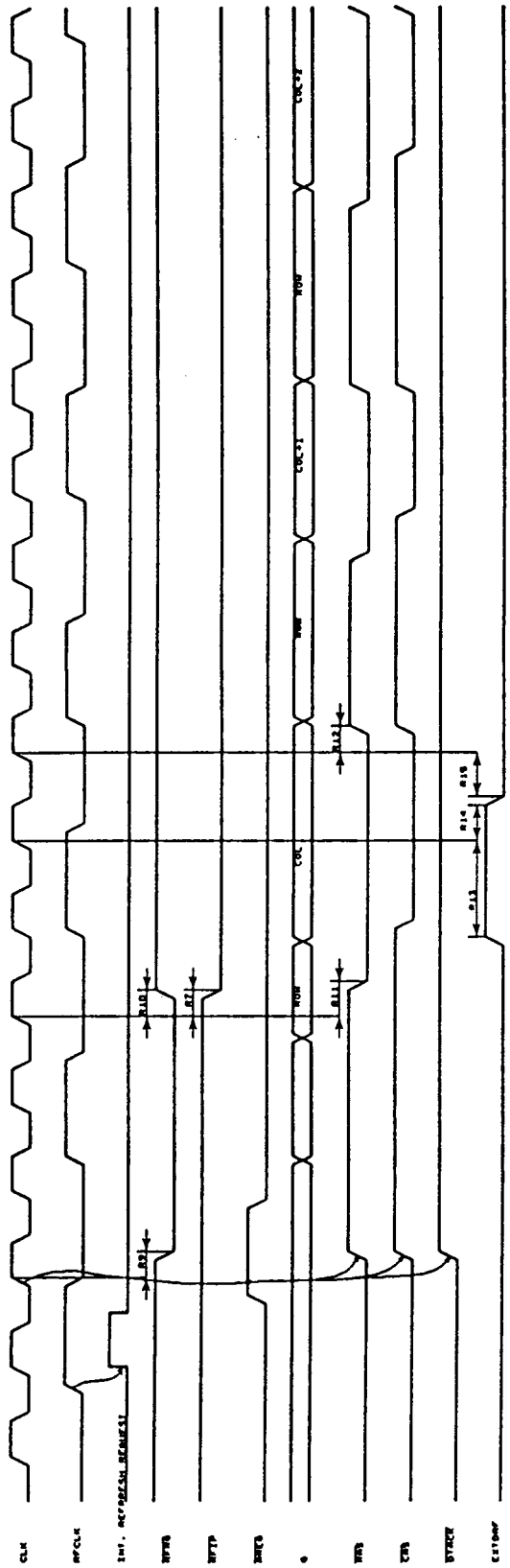


Figure 50. External Controlled Refresh

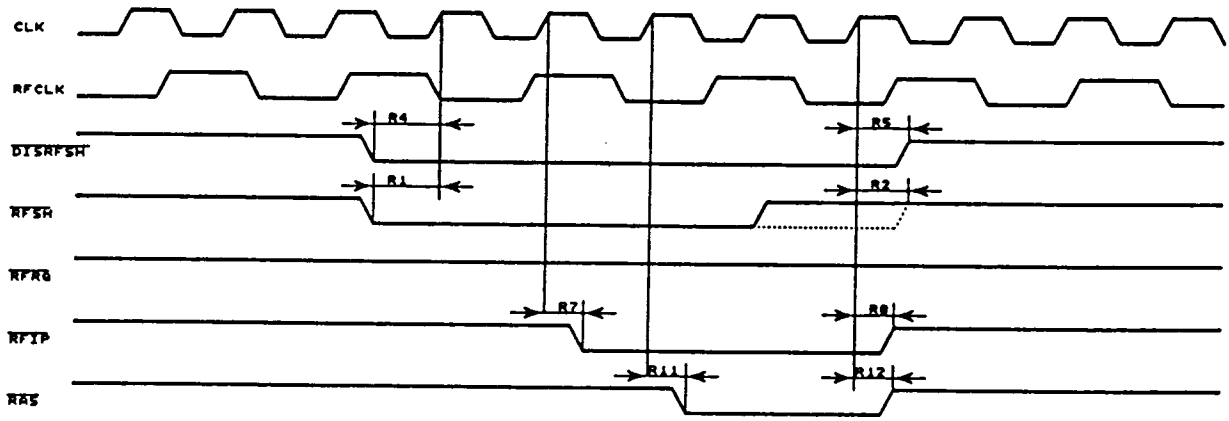


Figure 51. External Controlled Refresh ($\overline{ECAS0}$ = '0')

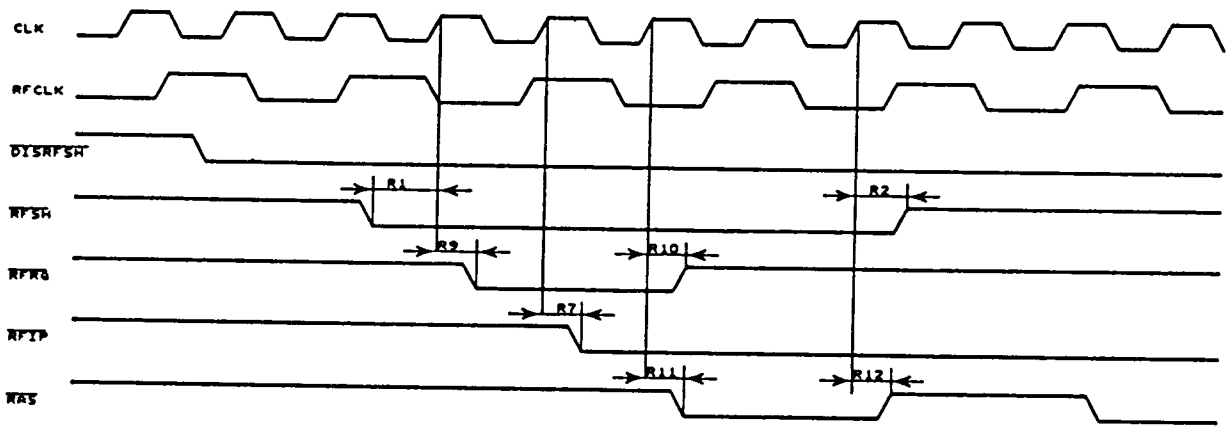


Figure 52. Page Mode — Disable Page Mode and Internal Refresh

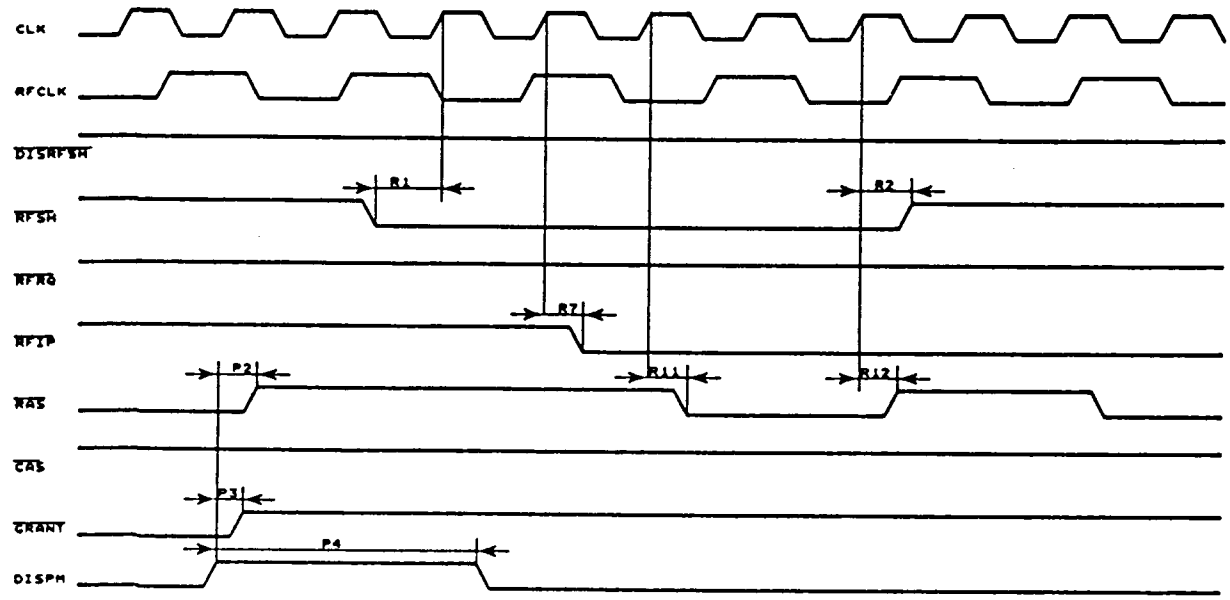


Figure 53. Access Cycle Termination

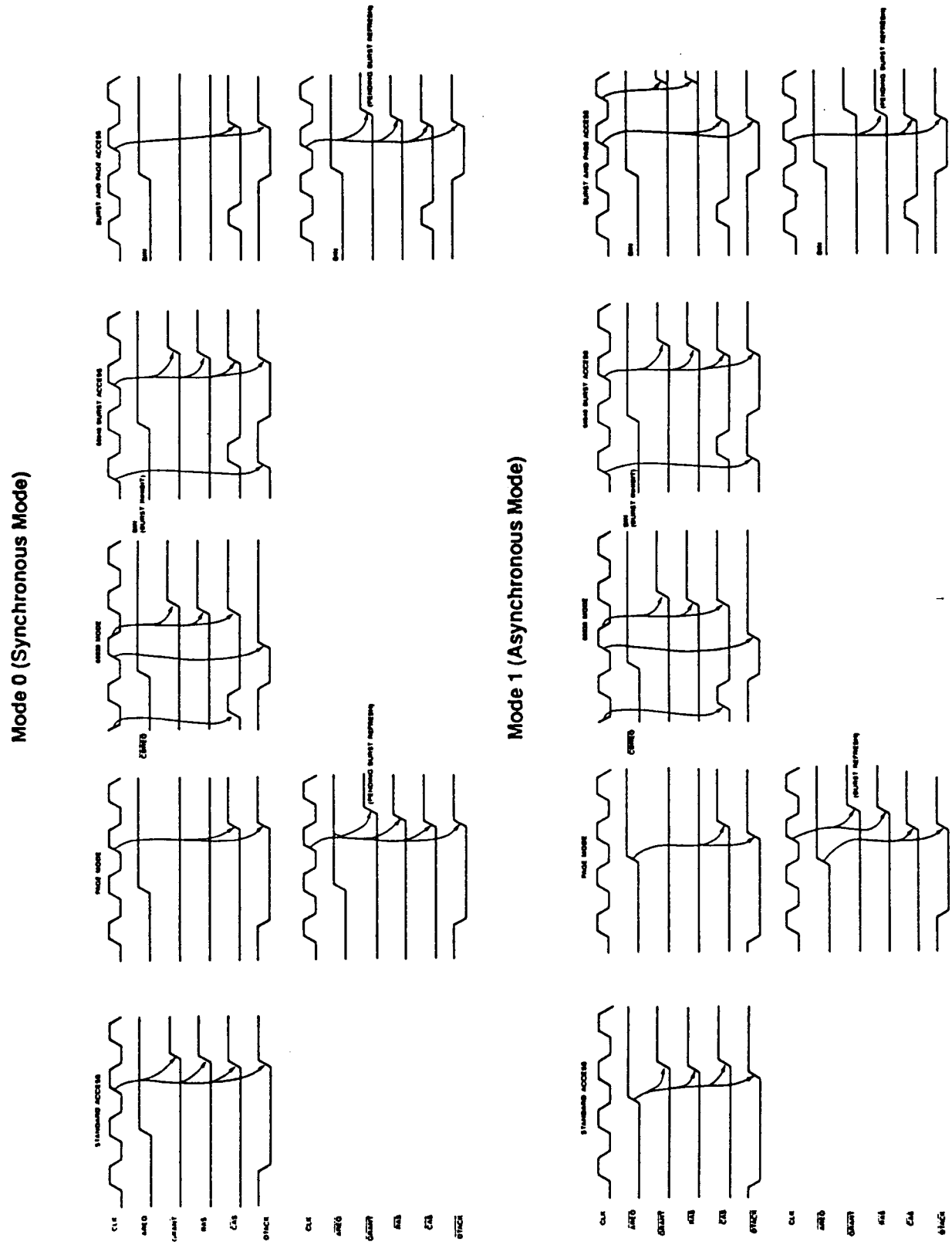
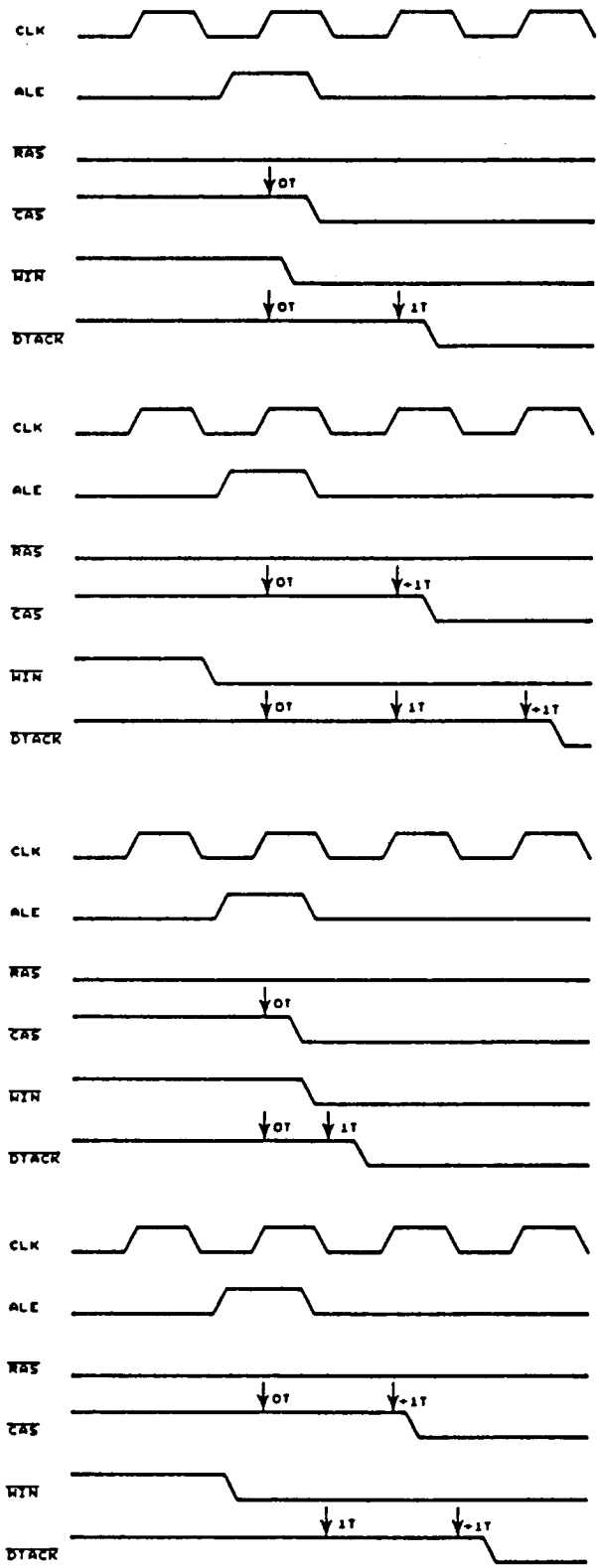


Figure 53. Access Cycle Termination (Continued)

Page Mode — Mode 0



Page Mode — Mode 1

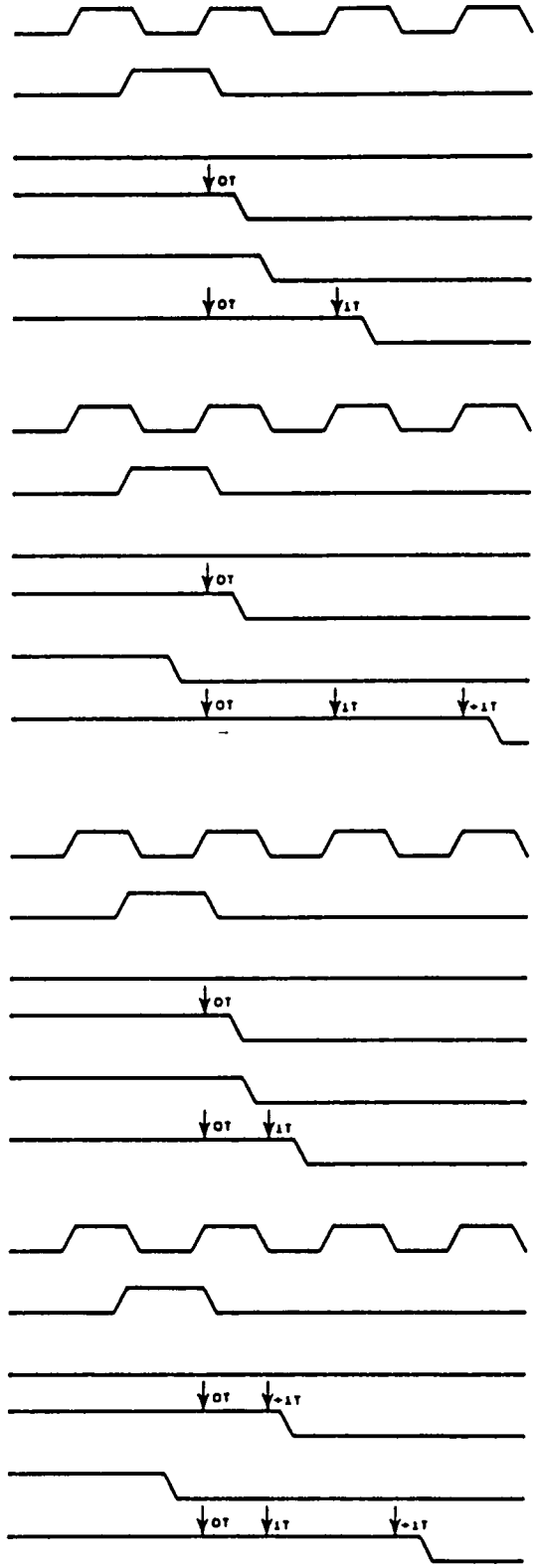


Figure 53. Access Cycle Termination (Continued)

68030 Mode

68040 Burst Mode

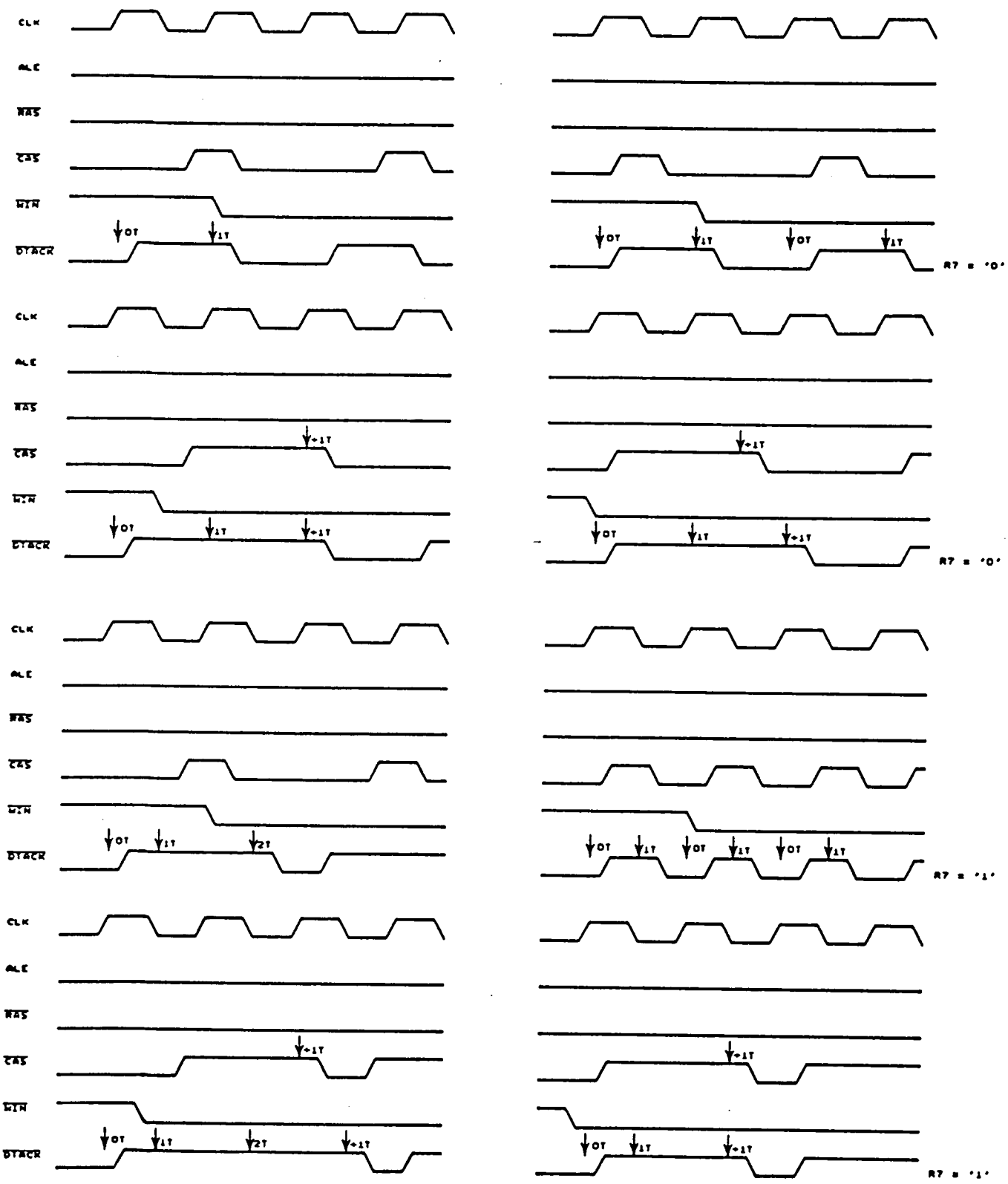


Figure 53. Access Cycle Termination (Continued)

68030 Mode

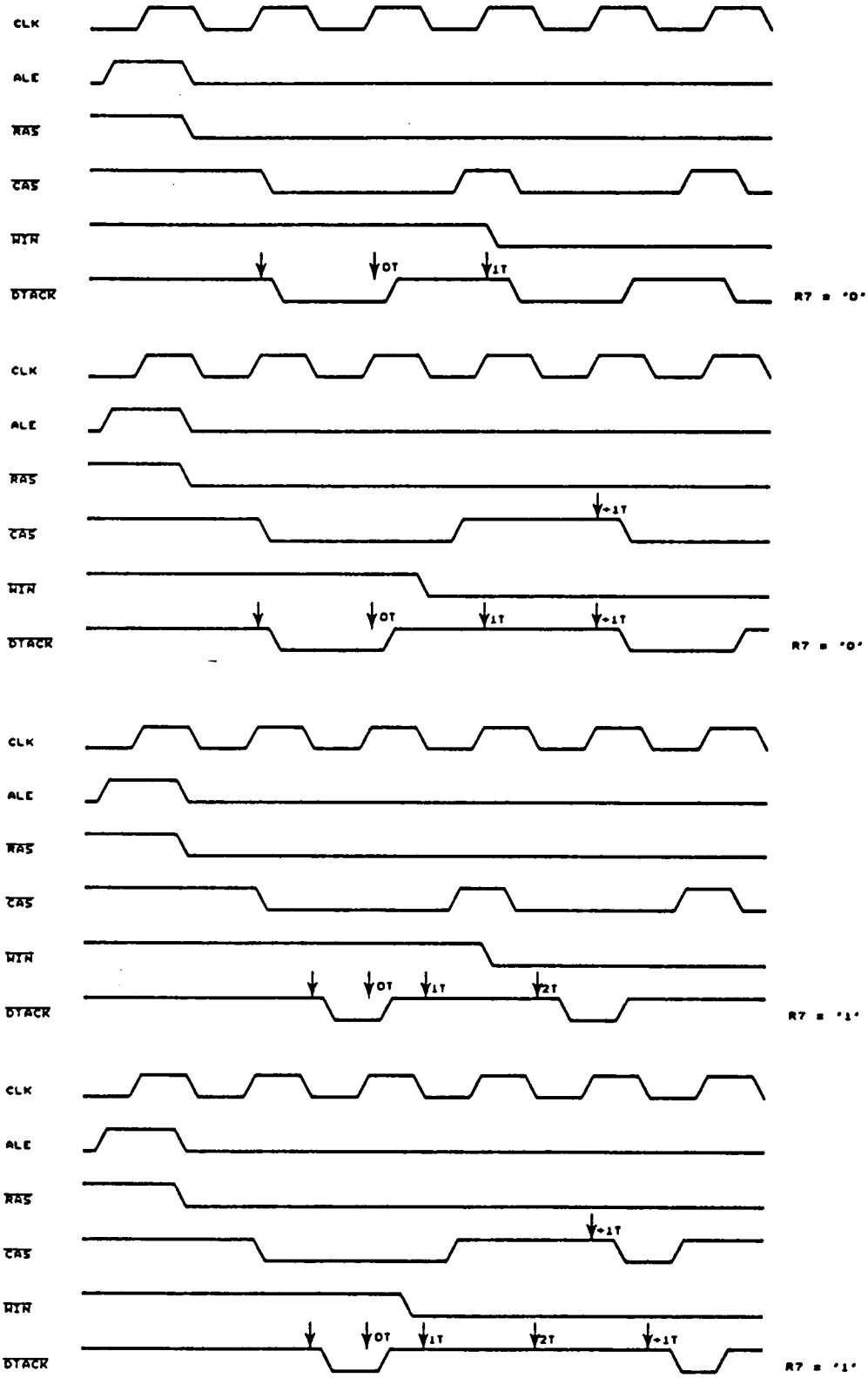
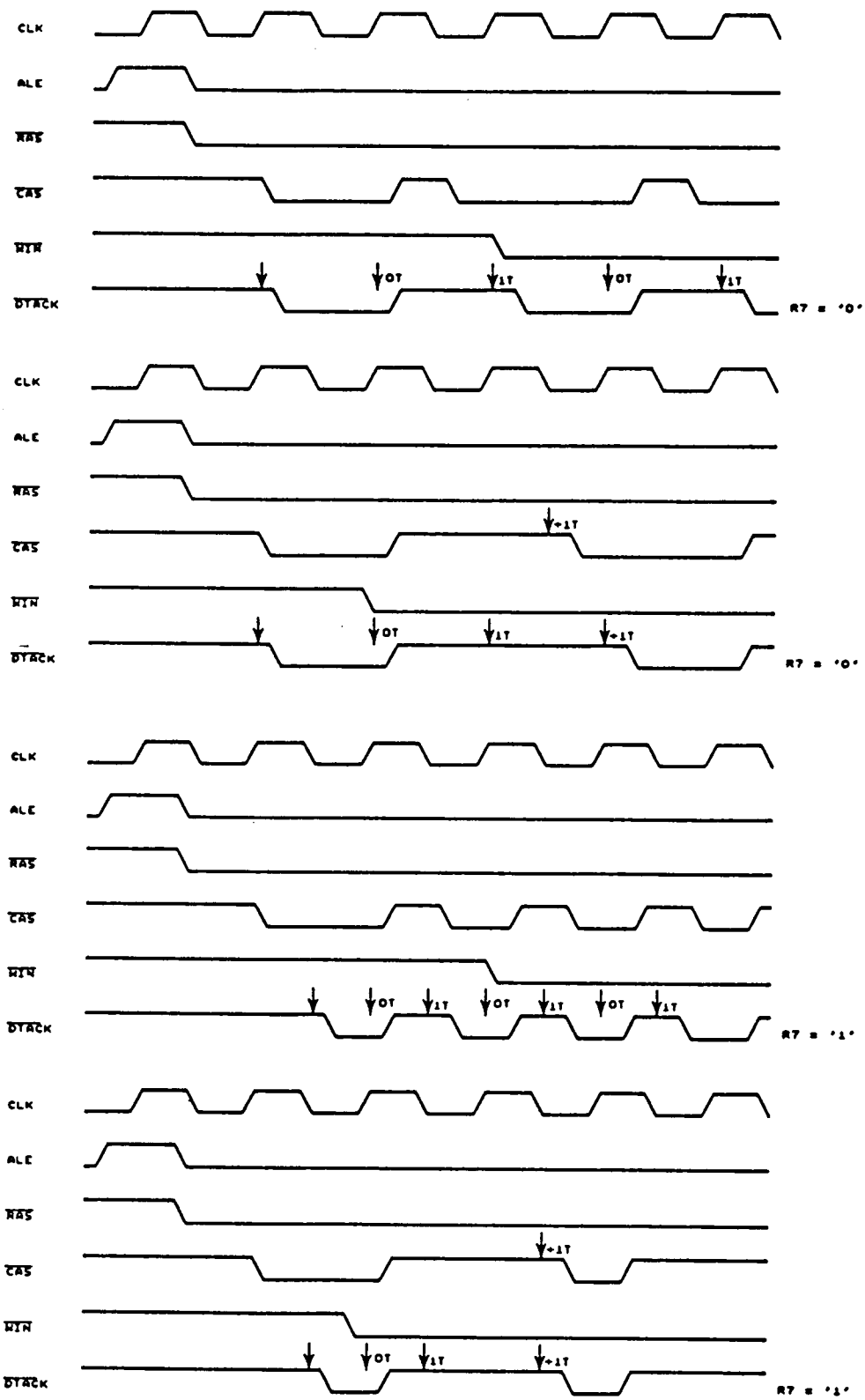


Figure 53. Access Cycle Termination (Continued)

68040 Burst Mode



Mode 0 Parameters

	Parameter	-40	
		Min	Max
01	ALE minimum low time	10	
02	$\overline{CS}$ to access start setup	3	
03	Access start to $\overline{RAS}$ asserted		24
04	Address setup to access start to guarantee 0ns row address setup time	3	
05	Address hold time from ALE low when using the on chip latch	10	
06	Access start to $\overline{CAS}$ asserted		
a	t_{RAH} = 12ns, t_{ASC} = 0ns	44	62
b	t_{RAH} = 12ns, t_{ASC} = 10ns	44	65
c	t_{RAH} = 18ns, t_{ASC} = 0ns	44	70
d	t_{RAH} = 18ns, t_{ASC} = 10ns	44	75
07	Access start to column address		
a	t_{RAH} = 12ns		50
b	t_{RAH} = 18ns		55
08	ALE high to CLK rising edge	3	
09	ALE pulse width	10	
010	$\overline{CS}$ hold after access start	10	
011	$\overline{AREQ}$ to CLK rising edge setup time	3	
012	$\overline{AREQ}$ from CLK rising edge hold time	2	
014	CLK rising edge to $\overline{RAS}$ deasserted		24
015	CLK rising edge to $\overline{CAS}$ deasserted	8	20
016	CLK rising edge to $\overline{GRANT}$ deasserted		20
017	ALE negated from CLK rising edge	2	

Mode 0 Page Mode Related Parameters

	Parameter	-40	
		Min	Max
P01	Access start (CLK rising edge) to $\overline{GRANT}$ asserted (non-delayed access)		21
P02	$\overline{AREQ}$ high setup to access start to guarantee $\overline{CAS}$ will stay high in case of page miss	3+1T	
P03	$\overline{CAS}$ deasserted from CLK rising edge	8	20
P04	Access Start to $\overline{CAS}$ low if page hit	6	24
P05	$\overline{GRANT}$ high from access start in case of page miss		22
P06	$\overline{RAS}$ high from access start in case of a page miss	5	26
P07	Row and bank address set up to assure a page miss is recognized	3	
P08	Row and bank address hold from access start		10
P09	$\overline{WIN}$ low set up to access start (C9 = '1')	4	
P010	$\overline{WIN}$ low hold time from access start (C9 = '1')	6	
P011	DISPM high setup to CLK rising edge	3	
P012	DISPM asserted to access start	3	
P013	Address setup to access start to guarantee 0ns column address setup time	3	

Mode 1 Parameters

	Parameter	-40	
		Min	Max
11			
a	Access start to CLK rising edge (R7 = '0')	7	
b	Access start to CLK falling edge (R7 = '1')	8	
12	$\overline{CS}$ to access start setup	3	
13	Access start to $\overline{RAS}$ asserted		17
14	Address setup to access start to guarantee 0ns row address setup time	5	
15	Address hold time from access start when using the on chip latch	10	
16	Access start to $\overline{CAS}$ asserted		
a	t_{RAH} = 12ns, t_{ASC} = 0ns	44	60
b	t_{RAH} = 12ns, t_{ASC} = 10ns	44	65
c	t_{RAH} = 18ns, t_{ASC} = 0ns	44	70
d	t_{RAH} = 18ns, t_{ASC} = 10ns	44	70
17	Access start to column address		
a	t_{RAH} = 12ns		50
b	t_{RAH} = 18ns		55
18	$\overline{AREQ}$ rising edge to CLK rising edge to be recognized as 1T of $\overline{RAS}$ precharge	14	
19	$\overline{ADS}$ pulse width	10	
110	$\overline{CS}$ hold after access start	10	
111	$\overline{AREQ}$ deasserted to $\overline{RAS}$ deasserted		23
112	$\overline{AREQ}$ deasserted to $\overline{CAS}$ deasserted	8	19
113	$\overline{GRANT}$ deasserted from $\overline{AREQ}$ high		20
114	$\overline{AREQ}$ asserted	8	
115	$\overline{AREQ}$ pulse width	10	
116	$\overline{AREQ}$ rising edge to access start (R8 = '1' non interleave)	10	

Mode 1 Page Mode Related Parameters

	Parameter	-40	
		Min	Max
P10	$\overline{ADS}$ falling edge to CLK rising edge to be recognized as 1T of $\overline{RAS}$ precharge in case of page miss	15	
P11	Access start ($\overline{ADS}$ falling edge) to $\overline{GRANT}$ low		18
P12	$\overline{AREQ}$ high set-up to access start to guarantee $\overline{CAS}$ will stay high in case of page miss	10	
P14	Access start to $\overline{CAS}$ low if page hit	6	22
P15	$\overline{GRANT}$ high from $\overline{ADS}$ falling edge if page miss is detected		20
P16	$\overline{RAS}$ high from access start in case of a page miss		25
P17	Row and bank address set up to assure a page miss is recognized	5	
P18	Row and bank address hold from access start		10
P19	$\overline{WIN}$ low set up to access start (C9 = '1')	4	
P110	$\overline{WIN}$ low hold time from access start (C9 = '1')	6	
P112	DISPM asserted to access start	3	
P113	Address setup to access start to guarantee 0ns column address setup time	5	

Common Parameters

	Parameter	-40 Min	-40 Max
C1	R, C input to Q output from ALE/$\overline{ADS}$ going high	8	25
C2	R, C input to Q output	8	20
C3	Row address hold time		
a	t_{RAH} = 12ns	12	
b	t_{RAH} = 18ns	18	
C4			
a	$\overline{WIN}$ high to $\overline{WE}$ high		15
b	$\overline{WIN}$ low to $\overline{WE}$ low		15
C5	Column address setup time		
a	t_{ASC} = 0ns	0	
b	t_{ASC} = 10ns	10	
C6	Column address hold time (interleave only)	25	60
C7	CLK rising edge to $\overline{RAS}$ asserted after delayed access		24
C8	CLK rising edge to $\overline{CAS}$ asserted after delayed access		
a	t_{RAH} = 12ns, t_{ASC} = 0ns	44	62
b	t_{RAH} = 12ns, t_{ASC} = 10ns	44	65
c	t_{RAH} = 18ns, t_{ASC} = 0ns	44	70
d	t_{RAH} = 18ns, t_{ASC} = 10ns	44	75
C9	CLK rising edge to $\overline{CAS}$ deasserted (mode C9 = '1')		20
C10			
a	$\overline{ECAS}$ high to $\overline{CAS}$ high	6	15
b	$\overline{ECAS}$ low to $\overline{CAS}$ low	6	15
C11	CLK high	11.5	
C12	CLK low	11.5	
C13	CLK period	25	
C14	RFCLK high	16	
C15	RFCLK low	16	
C16	RFCLK period	40	
C17	CLK rising edge to column address		
a	t_{RAH} = 12ns		50
b	t_{RAH} = 18ns		55

Common Page Mode Related Parameters

	Parameter	-40 Min	-40 Max
P1	$\overline{GRANT}$ low from access start (defered access)		21
P2	DISPM rising edge to $\overline{RAS}$ negated		21
P3	DISPM rising edge to $\overline{GRANT}$ negated		18
P4	DISPM high pulse width	10	

Common Wait State Parameters

	Parameter		-40 Min	-40 Max
W1				
a	CLK rising edge to $\overline{DTACK}$ low	(R7 = '0')	6	17
b	CLK falling edge to $\overline{DTACK}$ low	(R7 = '1')	6	18
W2				
a	$\overline{WAITIN}$ setup to CLK rising edge to add 1T	(R6 = '0', R7 = '0')	3	
b	$\overline{WAITIN}$ setup to CLK falling edge to add 1T	(R6 = '0', R7 = '1')	3	
W3				
a	$\overline{WAITIN}$ hold time from clock rising edge	(R6 = '0', R7 = '0')	5	
b	$\overline{WAITIN}$ hold time from clock falling edge	(R6 = '0', R7 = '1')	5	
W4	$\overline{WAITIN}$ high setup time to	(R6 = '1')		
a	CLK rising edge	(R7 = '0')	0	
b	CLK falling edge	(R7 = '1')	0	
W5	$\overline{WAITIN}$ high hold time from	(R6 = '1')		
a	CLK rising edge	(R7 = '0')	5	
b	CLK falling edge	(R7 = '1')	5	
W7	$\overline{WAITIN}$ low hold time from	(R6 = '1')		
a	CLK rising edge	(R7 = '0')	5	
b	CLK falling edge	(R7 = '1')	5	
W8	CLK rising edge to $\overline{DTACK}$ deasserted (burst mode)		8	17

Mode 0 Wait State Parameters

	Parameter		-40 Min	-40 Max
W01	CLK rising edge to $\overline{DTACK}$ high		6	18
W02	$\overline{WAITIN}$ low setup to access start	(R6 = '1')	1	
W03	$\overline{WAITIN}$ low hold time from access start	(R6 = '1')	8	
W04	CLK rising edge to $\overline{DTACK}$ asserted during page hit (0T programmed)		6	20

Mode 1 Wait State Parameters

	Parameter		-40 Min	-40 Max
W11	$\overline{ADS}$ falling edge to $\overline{DTACK}$ asserted			18
W12	$\overline{AREQ}$ rising edge to $\overline{DTACK}$ deasserted		4	15
W13	$\overline{WAITIN}$ low setup to access start	(R6 = '1')	0	
W14	$\overline{WAITIN}$ low hold time from access start	(R6 = '1')	8	

Mode Load Parameters

	Parameter	-40	
		Min	Max
M1	Mode address setup time	5	
M2	Mode address hold time	10	
M3	$\overline{ML}$ asserted to $\overline{AREQ}$ asserted	10	
M4	$\overline{CS}$ asserted to $\overline{AREQ}$ asserted	5	
M5	Mode address hold time from $\overline{AREQ}$ asserted	20	
M6	Mode address setup time to $\overline{AREQ}$ asserted	5	
M7	$\overline{AREQ}$ asserted to $\overline{DTACK}$ asserted		20
M8	$\overline{AREQ}$ or $\overline{ML}$ deasserted to $\overline{DTACK}$ deasserted		15
M9	$\overline{ML}$ pulse width	20	
M10	$\overline{CS}$ hold time from $\overline{AREQ}$ falling edge (for "fake access")	10	

Burst Mode Parameters

	Parameter		-40	
			Min	Max
N1	CLK rising edge to $\overline{CAS}$ deasserted	($\overline{ECAS3}$ = '1')	8	18
N2	CLK falling edge to $\overline{CAS}$ asserted	($\overline{ECAS3}$ = '1')	8	17
N3	CLK falling edge to $\overline{CAS}$ deasserted	($\overline{ECAS1}$ = '1')	8	18
N4	CLK rising edge to $\overline{CAS}$ asserted	($\overline{ECAS1}$ = '1')	8	17
N5	$\overline{CAS}$ high pulse width		10	
N6	CLK rising/falling edge to column + 1 output	(B0 = '0')	8	21
N7	$\overline{WIN}$ low set up to CLK rising edge	(C9 = '1')	3	
N8	$\overline{WIN}$ low hold time from CLK rising edge	(C9 = '1')	3	
N9	$\overline{CBREQ}$ setup to CLK rising edge that negates $\overline{DTACK}$		4	
N10	$\overline{CBREQ}$ hold time form CLK rising edge that negates $\overline{DTACK}$		2	
N11	BIN setup to CLK rising edge		8	
N12	BIN hold time from CLK rising edge		2	

Refresh Related Parameters

	Parameter	-40	
		Min	Max
R1	$\overline{RFSH}$ low setup time to CLK rising edge	10	
R2	$\overline{RFSH}$ low hold time from CLK rising edge	5	
R3	$\overline{RFSH}$ pulse width for resetting refresh counter	15	
R4	$\overline{DISRFSH}$ low setup to CLK rising edge	10	
R5	$\overline{DISRFSH}$ low hold time from CLK rising edge	5	
R6	$\overline{DISRFSH}$ low pulse width	15	
R7	CLK rising edge to $\overline{RFIP}$ asserted		15
R8	CLK rising edge to $\overline{RFIP}$ deasserted		23
R9	CLK rising edge to $\overline{RFRQ}$ asserted		18
R10	CLK rising edge to $\overline{RFRQ}$ deasserted		19
R11	CLK rising edge to refresh $\overline{RAS}$ asserted		23
R12	CLK rising edge to refresh $\overline{RAS}$ deasserted		23
R13	EXTDRF setup to CLK rising edge	5	
R14	EXTDRF hold time from CLK rising edge	2	
R15	EXTDRF low setup to CLK rising edge	5	

PACKAGE DIMENSIONS

The Samsung KS84EC30 DRAM Controller is available in a 68 pin PLCC package as shown in Figure 54.

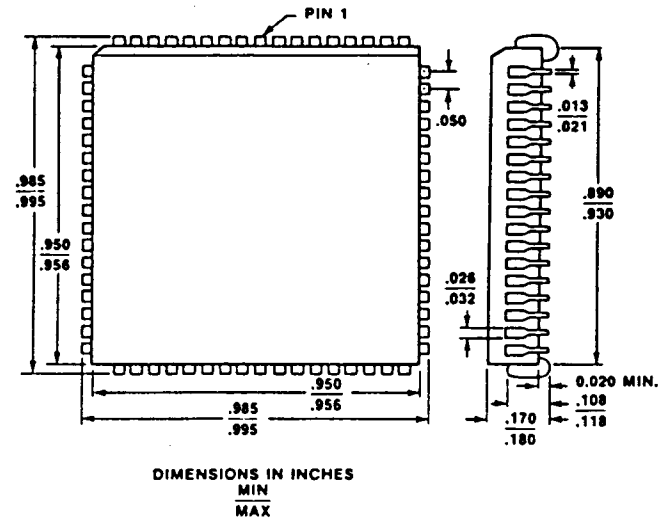
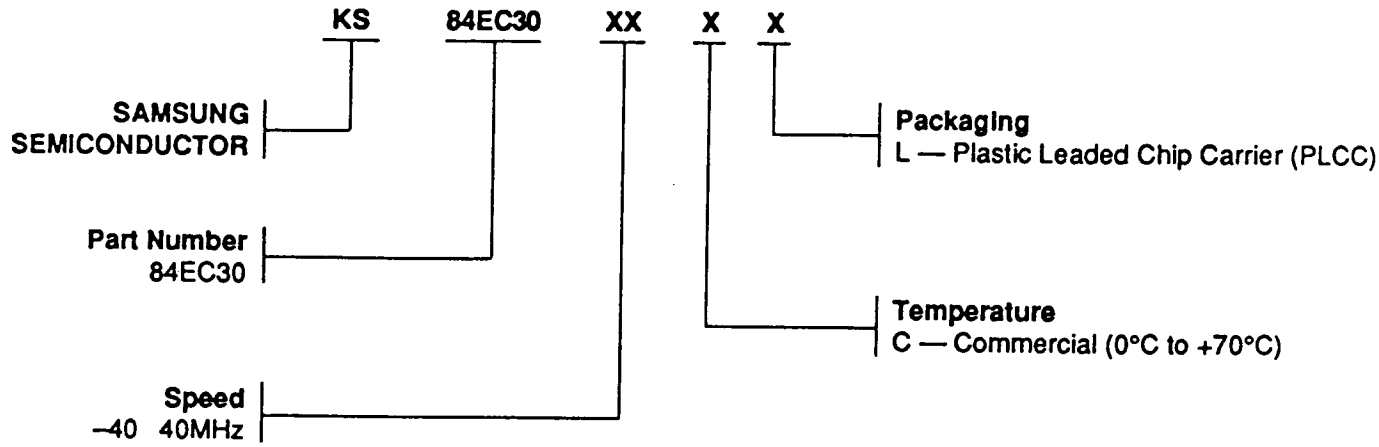


Figure 54. 68-Pin PLCC Package

ORDERING INFORMATION AND PRODUCT CODE



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