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# DEI1090
# LED Driver with Square-Law Dimming Control

## FEATURES

- Emulates incandescent lamp 'Square Law' luminance curve.
- LED dimming controlled by Pulse Width Modulation ranging from 50HZ to 200HZ.
- Maximum LED current adjustable from 10mA to 20mA.
- 200:1 Dimming Range at 50Hz. 40:1 Dimming Range at 200Hz
- Drives 8 LED outputs with matched current drive.
- Drivers can be cascaded to synchronously drive additional LEDs.
- Package Options
  - o Plastic 16 lead SOIC
  - o 20L QFN 5 X 5

## APPLICATIONS

- LED replacement for dimmable incandescent lamps.
- Avionics instrument and panel lighting.
- Balanced display and keyboard backlighting.

## GENERAL DESCRIPTION

DEI1090 device is a 16 pin bipolar integrated circuit designed to drive eight LEDs and provide Pulse Width Modulated (PWM) dimming control according to the luminance curve of incandescent lamps. All eight LEDx pins are driven with an average current proportional to the square of the input dimming voltage to control the LED brightness. Drivers can be cascaded to synchronously drive additional LED groups. The dimming control input may be a DC or AC voltage.

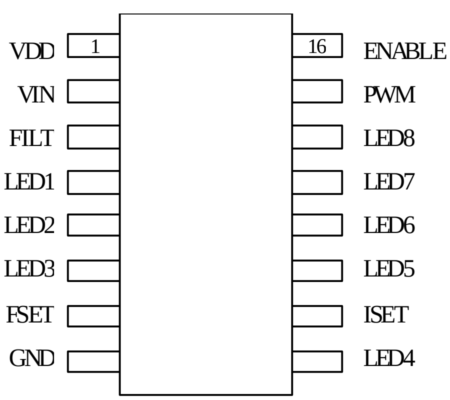
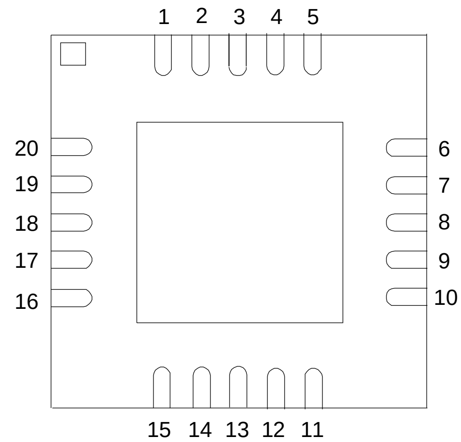



**Table 1 – SOIC Terminal Description**

| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | VDD | **POWER INPUT:** +4.5 to +16.5 VDC |
| 2 | VIN | **ANALOG INPUT:** 0 to 2.5V AC or DC analog input for brightness control. |
| 3 | FILT | **ANALOG IO:** Optional external filter resistor and capacitor used when 400HZ AC control signals are supported. This pin must be connected to ground through a resistor even in DC applications. |
| 4-6,9, 11-14 | LED1-8 | **LED DRIVE OUTPUT:** LED cathode connection. LED average current is proportional to the square of VIN. |
| 7 | FSET | **ANALOG INPUT:** External capacitor input to set PWM frequency. |
| 8 | GND | **POWER INPUT:** Ground. |
| 10 | ISET | **ANALOG INPUT:** External resistor input to set LED |
| 15 | PWM | **ANALOG OUTPUT:** PWM output drives multiple 1090 slave devices for synchronous operation. |
| 16 | ENABLE | **LOGIC INPUT:** HIGH enables operation. LOW sets all LED outputs OFF and sets standby state. |




BOTTOM VIEW

| PIN | NAME | DESCRIPTION |
|---|---|---|
| **3** | **VDD** | **POWER INPUT:** +4.5 to +16.5 VDC. |
| **4** | **VIN** | **ANALOG INPUT:** 0 to 2.5V AC or DC analog input for brightness control. |
| **5** | **FILT** | **ANALOG IO:** Optional external filter resistor and capacitor used when 400HZ AC control signals are supported. This pin must be connected to ground through a resistor even in DC applications. |
| **6, 8, 9, 14, 16, 17, 18, 19** | **LED1-8** | **LED DRIVE OUTPUT:** LED cathode connection. LED average current is proportional to the square of VIN. |
| **11** | **FSET** | **ANALOG INPUT:** External capacitor input to set PWM frequency. |
| **7, 12, 13, 20** PAD | **GND** | **POWER INPUT:** Ground. |
| **15** | **ISET** | **ANALOG INPUT:** External resistor input to set LED current. |
| **1** | **PWM** | **ANALOG OUTPUT:** PWM output drives multiple 1090 slave devices for synchronous operation. |
| **2** | **ENABLE** | **LOGIC INPUT:** HIGH enables operation. LOW sets all LED outputs OFF and sets standby state. |
| **10** | | **No Connect** |

**Table 1A – QFN Terminal Description**

## FUNCTIONAL DESCRIPTION

### *Top Level*

Figure 1 is the top level diagram of the DEI1090 Square Law LED Dimmer. The input voltage from a dimming bus is scaled at
the VIN control pin to a range between 0 and 2.5V. The load on the dimming bus is kept to a minimum since the DEI1090 is locally powered through the VDD pin.

A peak detector/filter is provided to allow use of either a DC or AC control input. The optional filter is set by an external resistor and capacitor at the FILT pin. **A resistor load must be used even in DC applications. (Recommended 100kΩ)**

The ENABLE pin enables the part when high and must be tied to VDD when not used. When the ENABLE pin is low, the part is put into a standby state and all LEDs are set to off.

Eight LED driver outputs are provided. Each is driven with a Pulse Width Modulated (PWM) current waveform that has an average current proportional to the square of the voltage at the VIN pin. The PWM frequency is set with an external capacitor at the FSET pin. The peak LED current at 100% duty cycle is a multiple of the Iset current which is set with an external resistor at the ISET pin.

The PWM pin is provided to allow cascading multiple DEI1090s to expand the number of synchronously controlled LED driver output.

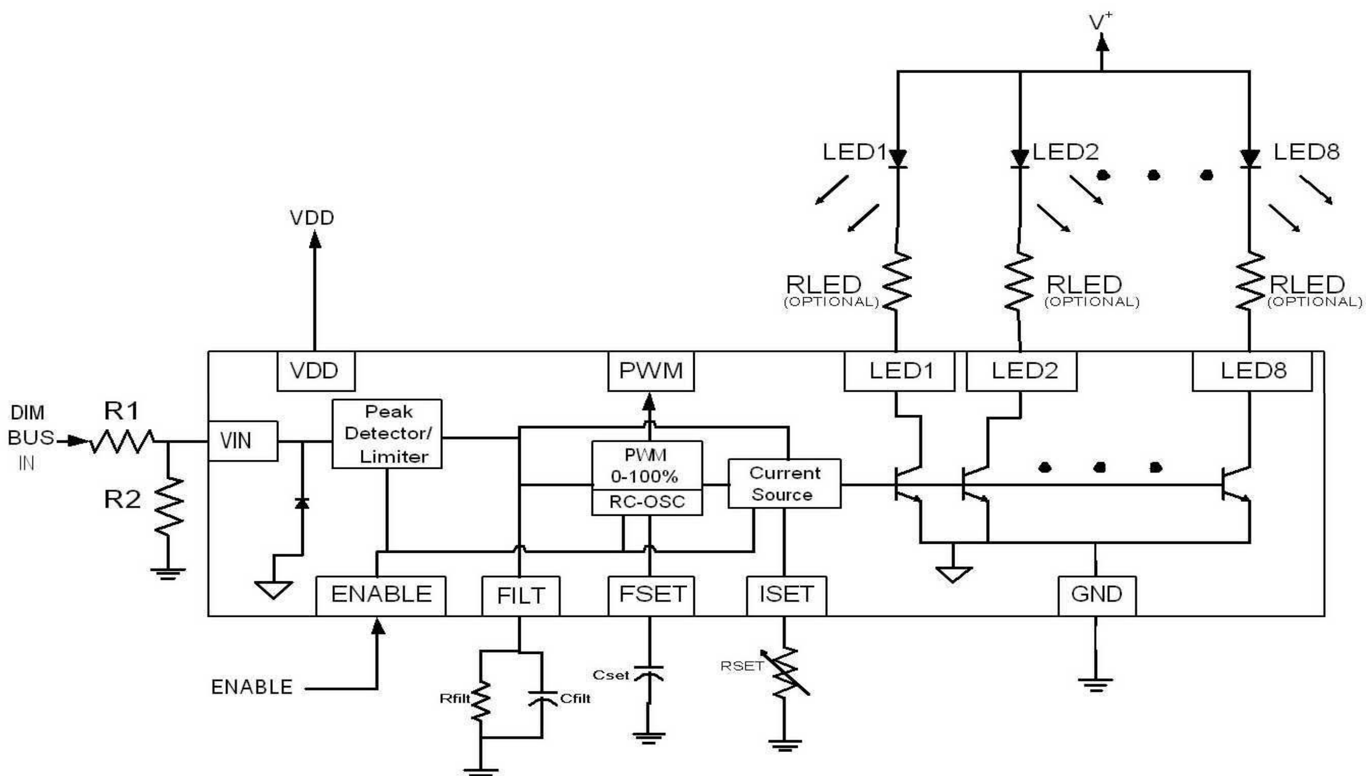



**Figure 1 - DEI1090 Simplified Block Diagram**

### *Input Filter and Peak Detector*

An external resistor divider is used to scale the voltage applied to the VIN pin providing interface to a variety of standard avionics dimming bus formats i.e. 0-5VDC, 0-5VAC, 0-28VDC as showing in Table . The VIN interface contains a peak detector and a filter circuit to allow 400HZ AC control input signals. The external filter connections are shown in Figure 1. When an AC input is used, Rfilt and Cfilt should be set up to filter 400 Hz into DC. The signal to the FILT pin is limited to an internal 2.5V reference. **A resistor load (Rfilt in the figure) must be used for the FILT pin even in DC applications.**

## *Dimming Control*

The DEI1090 VIN control signal ranges from 0V to 2.5V full scale. This controls the PWM duty cycle and the LED current to produce an average current proportional to the square of the control voltage. The square-law characteristic equations are shown below and the resulting LED average current vs. VIN curve is shown in Figure 2.

The square-law curve includes a 0.5V typical onset voltage (Vos) where LED illumination begins. When VIN is below Vos, the LEDs are off (Iled < Ioff) which emulates the behavior of an incandescent lamp. The current gain (Igain) from the ISET pin to the LEDx output pins is typically around 24 for a 5V system.

$$Iled(peak) = \begin{cases} 0 & if\ Vin < Vos \\ \left[\dfrac{(Vin - Vos)}{Rset}\right] * Igain & if\ Vin > Vos\ and < 2.5V \\ \left[\dfrac{(2.5V - Vos)}{Rset}\right] * Igain & if\ Vin > 2.5V \end{cases}$$

$$Iled(dutycycle) = \begin{cases} 0\,\% & if\ Vin < Vos \\ \dfrac{(Vin - Vos)}{(2.5V - Vos)} & ifVin > Vos\ and < 2.5V \\ 100\% & if\ Vin > 2.5V \end{cases}$$

$$Iavg = \begin{cases} 0 & if\ Vin < Vos \\ \left[\dfrac{(Vin - Vos)^2}{(2.5V - Vos) * Rset}\right] * Igain & if\ Vin > Vos\ and < 2.5V \\ \left[\dfrac{(2.5V - Vos)}{Rset}\right] * Igain & ifVin > 2.5V \end{cases}$$

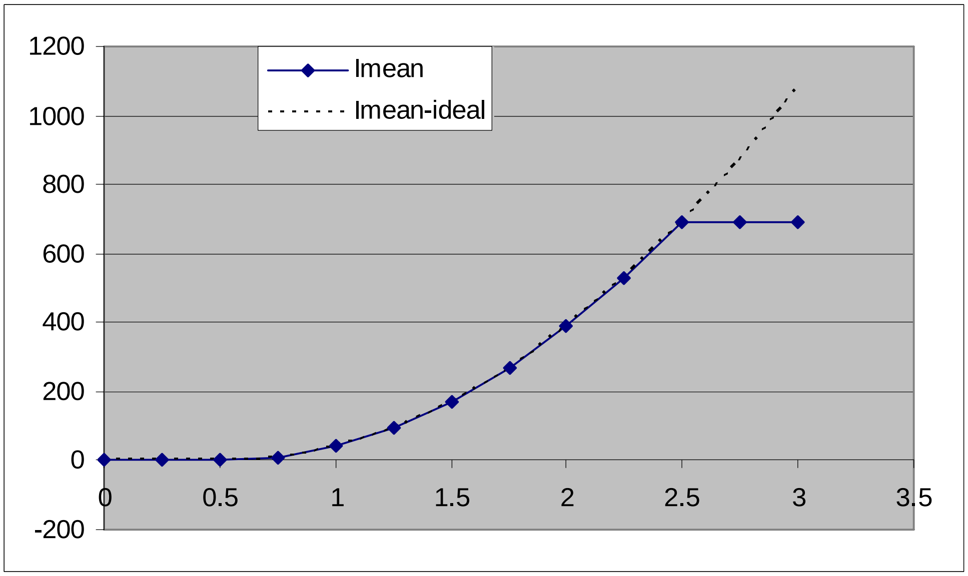



**Figure 2 - Square-Law Relationship of VIN vs. Iled Average**

## APPLICATION INFORMATION

### *Setting PWM Frequency*

The PWM frequency can be set with an external capacitor (Cfset) as shown in Figure 1. The PWM frequency is determined by:

$$PWM\ frequency = \frac{Ifset}{2 * Cfset};$$ where $C_{fset}$ is in uF and $I_{fset}$ is in uA

For example, to set the frequency to 120Hz nominal with a 12 uA charging current, $C_{fset}$ should be 0.05 μF. The serrodyne waveform will be seen at the FSET pin and is buffered to the PWM output. In most cases the actual frequency will be slightly lower since the reset of the serrodyne (ramp generator) is not instantaneous.

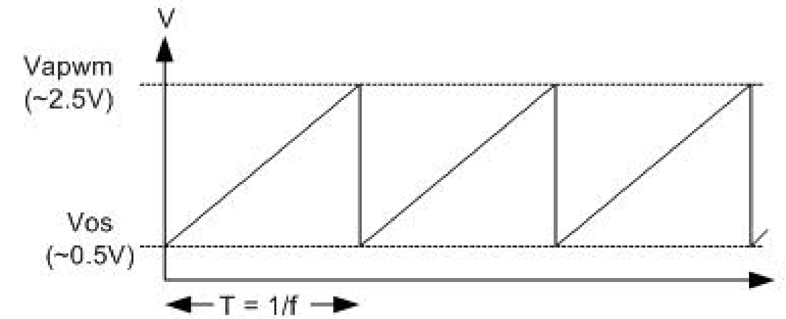



**Figure 3 - PWM Serrodyne Waveform**

### *Cascading Multiple Drivers*

Multiple drivers can be cascaded by connecting the PWM pin to the FSET pin of one slave device. If more than two are required, daisy chain the next PWM to the next FSET pin. The PWM output waveform is a buffered Serrodyne signal as generated at the FSET pin.

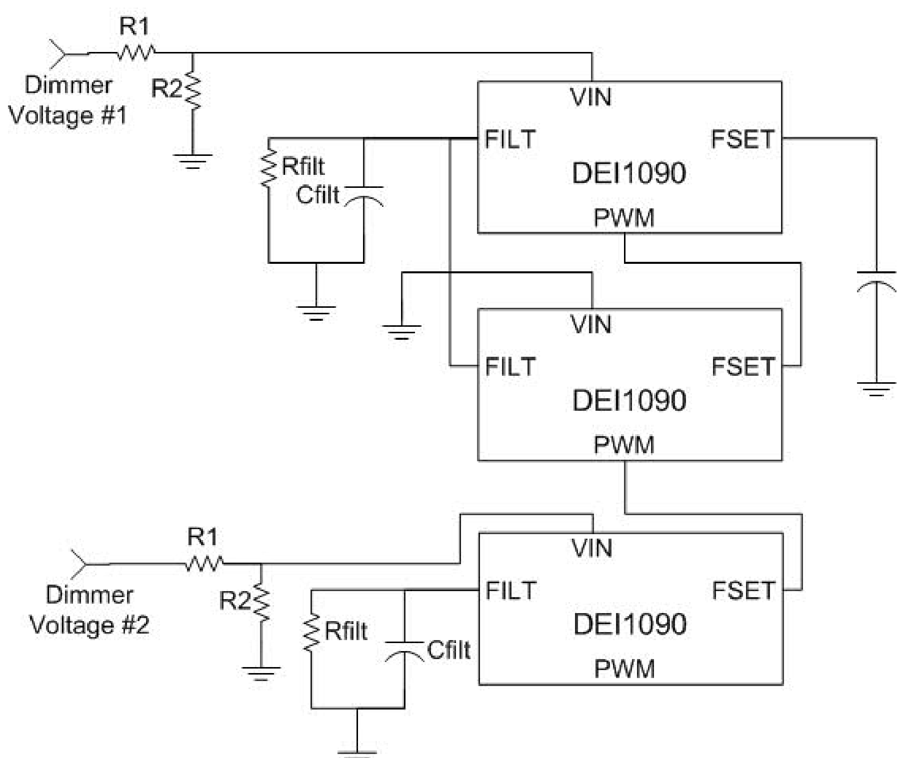



**Figure 4 - Cascading Multiple Drivers**

## *Setting Up Your Input and Filter*

Many dimmer applications use a 400 Hz AC source for the dimming voltage. The brightness of the incandescent lamp is proportional to the RMS value of the AC signal. As an added feature, the DEI1090 has an input peak detector and allows for an external filter to be added so that AC dimming signals can be used to create a proportional DC voltage. The input is also limited at this stage to an on-chip 2.5V reference value.

All applications require an input divider to bring the signal to a level that is suitable for the DEI1090 device. After the input is half wave rectified and peak detected, then it is sent to the FILT pin where a filter should be placed to remove ripple from the signal. The input resistors R1 and R2 shown in Figure 5 should be set up as shown in Table 2.

| Input Type | R1 | R2 | Comments |
|---|---|---|---|
| 5V AC Dimming Voltage | 1.83 * R | R | R should be at least 10K ohms to protect the chip from clamp current when an AC signal is used. |
| 5V DC Dimming Voltage | R | R | |
| 28V DC Dimming Voltage | 10.2 * R | R | |

**Table 2 - Resistor Ratios for Scaling Dimmer Voltages**

## *Example of Rset Determination*

Rset is selected to set the peak current value at 100% duty cycle. A fixed resistor or trimmer may be used to set the LED current for the required luminance at full scale Vin. The peak LED current range is from 10 mA and 20 mA. Resistor values should be set as shown in Table 3.

Note: To measure or adjust the peak current, drive Vin > 2.5V and < VDD.
* - Iled max in the table assumes a gain of 24.

| Rset | Iset max | Iled max * |
|---|---|---|
| 4.80 kΩ | 417 uA | 10 mA |
| 4.00 kΩ | 500 uA | 12 mA |
| 3.43 kΩ | 583 uA | 14 mA |
| 3.00 kΩ | 667 uA | 16 mA |
| 2.67 kΩ | 749 uA | 18 mA |
| 2.40 kΩ | 833 uA | 20 mA |

**Table 3 - Rset versus LED Maximum Current**

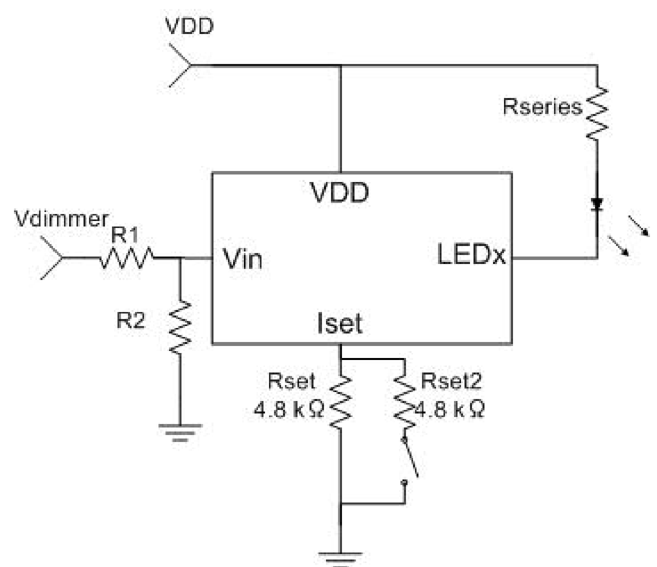



**Figure 5 - Dual Range LED Dimmer Example**

## *Creating a Dual Range Dimmer*

To create a dual range dimmer with two dimming curves, the circuit can be set up to switch a second Rset resistor in parallel with the primary Rset resistor.

An example is shown in Figure 5. This uses Rset = 4.8 kΩ resistor in parallel with Rset2 = 4.8 kΩ resistor and a switch. When the switch is open, Rset = 4.8 kΩ and the maximum LED current is ~ 10 mA. When the switch is closed, the equivalent resistance of 2.4 kΩ creates a maximum peak current of ~ 20 mA.

Note: To measure the peak current, drive Vin > 2.5V and < VDD.

## *LED Output Compliance Voltage and Power Consumption*

The DEI1090 regulates current through eight LED outputs. Each LEDx output can regulate LED current over a wide compliance voltage range. The voltage at the LED pin should be designed to be as low as possible to minimize power dissipation in the IC. Figure 6 shows typical LED output I-V characteristics for various Iset values.

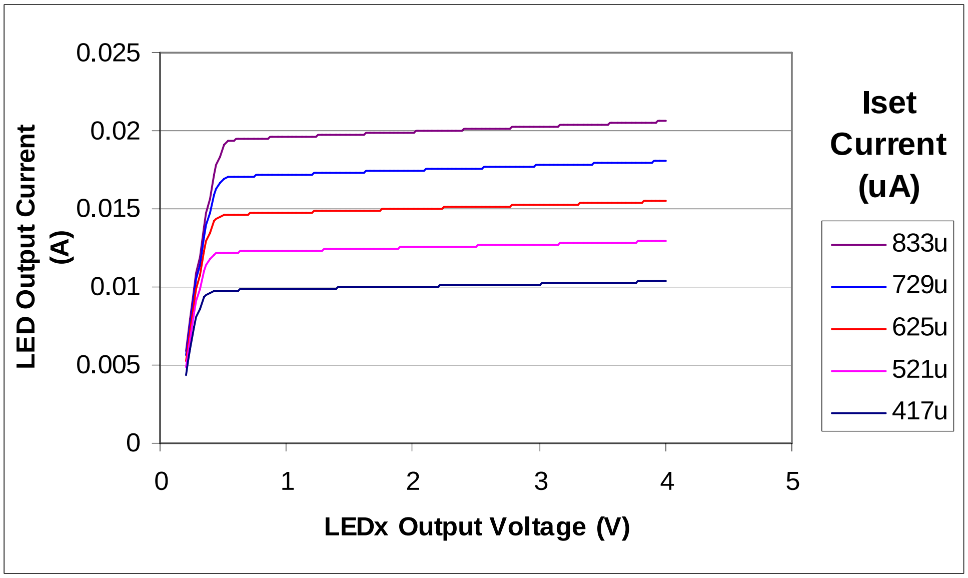



**Figure 6 – Output I-V Characteristics**

As is shown in Figure 6, an output voltage above 0.7V will regulate the output current.

Example calculation of IC power dissipation. Use Figure 1:

Given that the voltage across the LED is 2V and the current through each LED is 20 mA and there is 1 LED per output, Vdd supply is +12V, V+ is +5v and Iq (VDD quiescent current, see Table 6) is 3.5ma and the optional RLED resistors aren't being used, the average IC power dissipation due to the LED drive is:

Pd = Pq + Pld = Iq * Vdd + 8 * Iout * Vout = 3.5mA * 12v + 8 * 20 mA * (5v-2v) = 42mw + 480mw = 522mw

Pd must be kept below the maximum power listed in Table 4 to keep the junction temperature < Tjmax. Pd should be minimized for optimum IC reliability.

Assuming a Theta-ja (junction to ambient rise with power) of 74C/W, the junction temperature is .522 x 74 = 38.6C above ambient temperature.

One way to control the IC power dissipation is to place a resistor in series with the LED as shown in Figure 1. This will drop the excess V+ voltage in the resistor rather than in the IC.

## *Voltage Dependency of Igain*

The gain from Iset to Iled is nominally about 24. This gain has a supply voltage dependency so that the gain at VDD = 15V is higher than the gain when VDD = 5V. The minimum and maximum gain values for some common operating voltages are listed in Table 6. An example waveform of the linear voltage dependency is shown in Figure 7. **Note:** All LED outputs of the IC should be loaded. The part will still work with outputs unloaded but the current calculation may be skewed. For example, if four LED's are to be run at 20ma each, the Iset should be set to 10ma and the LED's paralleled in groups of two in order to use up all eight outputs.

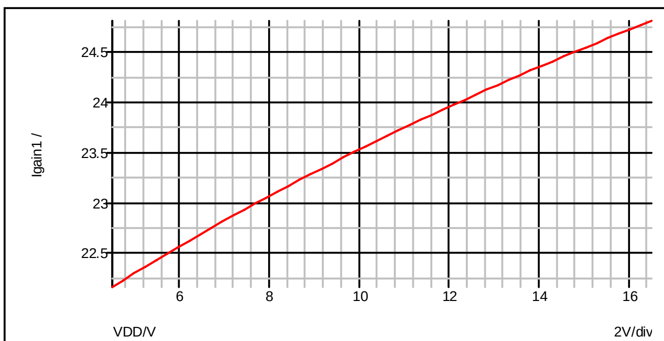



**Figure 7 - Voltage Dependency Curve**

## *Adjusting Onset Voltage and Gain Curve*

The LED onset voltage (Vos) is used to match the turn-on voltage of an incandescent lamp. If an application requires a Vos lower than the 0.5V Vos of the IC, an offset voltage may be added to the Vin input making the apparent turn-on voltage lower. As shown in Figure 8, the VDD is added in through Ros which is a much higher value than R1 and R2.

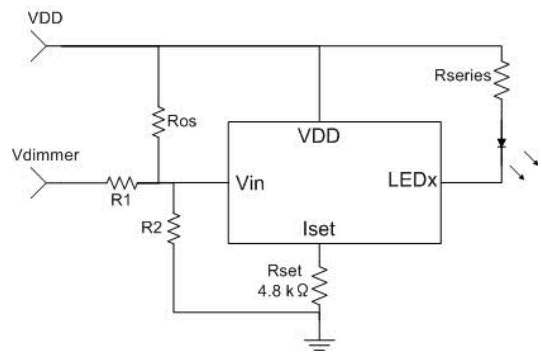



**Figure 8 – Vos reduction example**

As an example :

Vos is typically 0.5V

Choose R1 = R2 = 10 kΩ (5V DC Dimming Voltage)

If an onset voltage of 0.25 V is desired then, using the equation:

$$Vin = V\dim mer * \frac{R2 \| Ros}{R1 + (R2 \| Ros)} + VDD * \frac{R1 \| R2}{Ros + (R1 \| R2)}$$

Use Ros = 100 kΩ, then $Vin \cong V\dim mer * \frac{1}{2} + VDD * 0.05$.

This results in about an extra 0.25 V for a 5V supply and an apparent 0.25V onset voltage from the dimming bus. This onset voltage will vary with VDD.

Some applications might require a higher onset voltage. For example, the circuit in Figure 9 works with an input range of 9v through 28v to produce an equivalent .5v to 2.5v range at Vin of the IC. The zener diode in this example is 4.7v. The break point is set by D1 while the slope is set by the resistors.

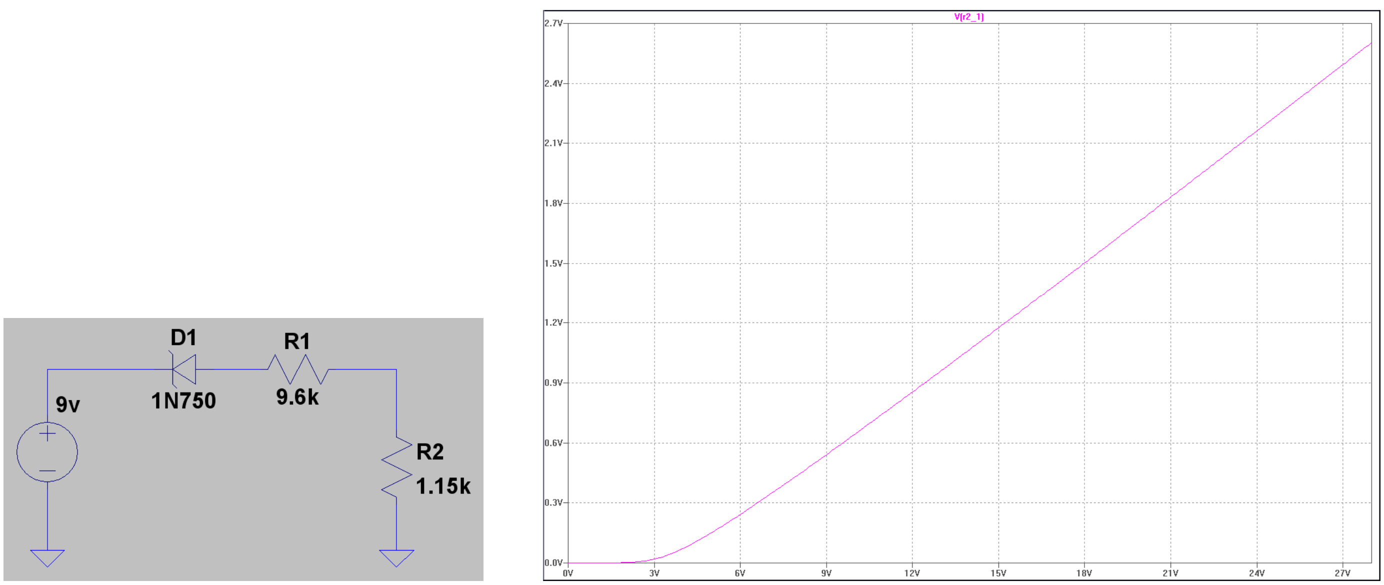



**Figure 9 Vos elevation example**

The schematic in Figure 10 provides two break points using diodes D1 and D2 that allow manipulating the curve to something other than the square law curve.  Zener diode D1 is 4.7v and D2 is 20v.  Input voltage range is 9v to 28v for a Vin on the IC of .5v to 2.5v.

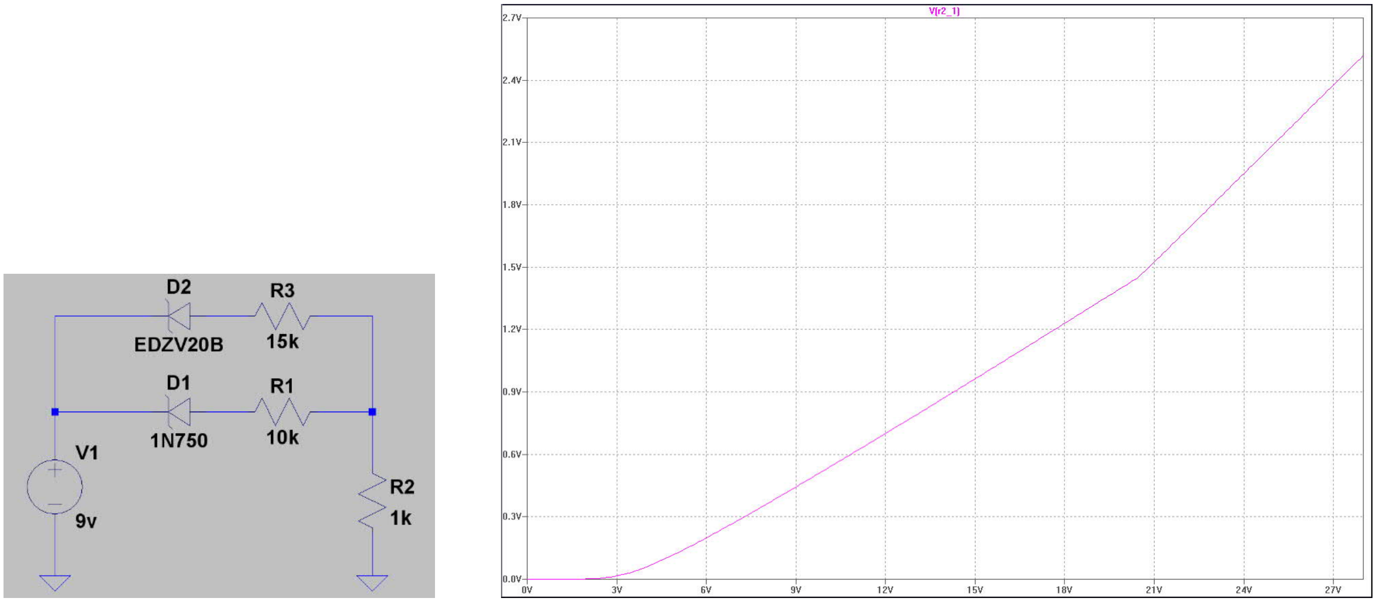



**Figure 10    Piecewise transfer curve modification example**

### *Slew Rate Control*

The current through the LED can be limited when required.  A 10us rise and fall time would require a minimum 50 mH inductor in series with the set resistor on the ground side.  Place a diode in parallel with the inductor from ground to the top pin in order to clamp negative going pulses to one diode drop below ground.

## ELECTRICAL DESCRIPTION

**Table 4 - Absolute Maximum Ratings**

| **PARAMETER** *(Voltages referenced to Ground)* | **MIN** | **MAX** | **UNITS** |
|---|---|---|---|
| VDD  Supply Voltage | | +20 | V |
| Storage Temperature | -65 | +150 | °C |
| Input Voltage<br>FSET, ISET, ENABLE, PWM pins<br>VIN pin (during AC dimmer operation, keep absolute current below 1 mA)<br>LED1-8 pins | – 0.3<br>– 0.6<br>– 0.3 | VDD+0.3<br>VDD+0.3<br>20 | V<br>V |
| Input Current: Any pin | -20 | 20 | mA |
| Power Dissipation @ 85 °C:  (> 10 Sec)<br>16 Lead SOIC | | 700 | mW |
| ESD per JEDEC A114-A Human Body Model | | 2000 | V |
| Peak Body Temperature,<br>Non-G Package<br>- G Package | - | 240<br>260 | °C |
| **Notes:** Stresses above absolute maximum ratings may cause permanent damage to the device. | | | |

## Table 5 - Recommended Operating Conditions

| **PARAMETER** *(Voltages referenced to Ground)* | **MIN** | **MAX** | **UNITS** |
|---|---|---|---|
| VDD Supply Voltage | +4.5 | +16.5 | V |
| Operating Temperature<br>Plastic Package | -55 | +85 | °C |
| Junction Temperature:<br>Tjmax, Plastic Packages (Limited by molding compound Tg) | | +125 | °C |

## Table 6 - Electrical Characteristics

**Conditions**: Temperature: -55°C to +85°C for plastic, VDD = 4.5 to 16.5V Unless otherwise noted.

| PARAMETER | CONDITIONS | SYMBOL | -55°C (4) | | | 25°C (4) *(or over temp range)* | | | 85°C (4) | | | UNITS (1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | |
| **SUPPLY CURRENT** | | | | | | | | | | | | |
| VDD Standby Current | ENABLE = 0.0 V, VDD=16.5V | Istdby | | 8 | 50 | | 6 | 15 | | 30 | 100 | uA |
| VDD Quiescent Current | ENABLE=VDD= 16.5V; VIN = 0.0 V; All LEDs off | Iq | | 2.5 | 5 | | 3.25 | 5 | | 3.5 | 5 | mA |
| **PULSE WIDTH MODULATOR** | | | | | | | | | | | | |
| VIN at 100% PWM Duty Cycle | | VAPWM | | | | 2.4 | 2.45 | 2.5 | | | | V |
| VIN at PWM Onset Voltage | | Vos1 | | | | 0.4 | 0.5 | 0.6 | | | | V |
| FSET charge current | FSET = 0V | $I_{FSET}$ | 11 | 13.3 | 15 | 13 | 15 | 16 | 13 | 14.2 | 16 | µA |
| PWM Output Voltage Accuracy from FSET Voltage (5) | Cascaded DEI1090 | PWMacc | | | | -3 | 0.3 | 3 | | | | % |
| **VIN BUFFER/PEAK DETECTOR/ FILTER** | | | | | | | | | | | | |
| VIN Input Voltage Range | | VIN | | | | 0 | | 2.5 | | | | V |
| VIN Input Current | VIN = 0V to 2.5V | Iin | | | | -10 | -5 | | | | | uA |
| Input Buffer Accuracy (DC) | VIN/Vfilt VIN = 1.0v | BufAcc | | | | -3 | 0.5 | 3 | | | | % |
| FILT Output Voltage | VIN = 0 to 2.5V | $V_{FILT}$ | | | | 0 | | 2.5 | | | | V |
| **LOGIC INPUT** | | | | | | | | | | | | |
| ENABLE Input Low | | Vil | | | 0.4 | | | 0.4 | | | 0.4 | V |
| ENABLE Input High | | Vih | 2.4 | | | 2.4 | | | 2.4 | | | V |
| ENABLE Input Current Low | ENABLE = Vilmax | Iil | | | | -5 | -1.8 | | | | | uA |
| ENABLE Input Current Hi | ENABLE = Vihmin | Iih | | | | -5 | -1.75 | | | | | uA |
| **LED DRIVER** | | | | | | | | | | | | |
| ISET Bias Voltage @ 100% Duty Cycle | VIN = 2.5V | $V_{SET}$ | | | | | 2.0 | | | | | V |
| LED Output Minimum Compliance Voltage (2) | $I_{LED}$ = 20mA | $V_{COMP}$ | | | | 0.7 | | | | | | V |
| LED Output Off State Leakage Current | VIN = 0V, LEDx = 5V | $I_{OFF}$ | | | | | 0.010 | 0.05 | | | | µA |

| Conditions: Temperature: -55°C to +85°C for plastic, VDD = 4.5 to 16.5V Unless otherwise noted. | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PARAMETER | CONDITIONS | SYMBOL | -55°C (4) | | | 25°C (4) *(or over temp range)* | | | 85°C (4) | | | UNITS (1) |
| | | | MIN | NOM | MAX | MIN | NOM | MAX | MIN | NOM | MAX | |
| Pin-to-PIN LED Output current matching, relative to median | VDD = 5V, 12V, 15V (3) | $I_{MATCH}$ | | | ±6 | | | ±5 | | | ±4 | % |
| Current Gain: Iset = 400uA | VDD = 5V (3) | $I_{LED5L}$ | 9 | | 14 | 9 | | 13 | 7 | | 11 | mA |
| | VDD = 12V (3) | $I_{LED12L}$ | 12 | | 17 | 11 | | 16 | 8 | | 11 | mA |
| | VDD = 15V (3) | $I_{LED15L}$ | 12 | | 17 | 12 | | 16 | 8 | | 12 | mA |
| Current Gain: Iset = 800uA | VDD = 5V (3) | $I_{LED5H}$ | 15 | | 21 | 16 | | 20 | 14 | | 18 | mA |
| | VDD = 12V (3) | $I_{LED12H}$ | 19 | | 26 | 17 | | 23 | 16 | | 20 | mA |
| | VDD = 15V (3) | $I_{LED15H}$ | 20 | | 27 | 17 | | 23 | 16 | | 20 | mA |

**Notes:**

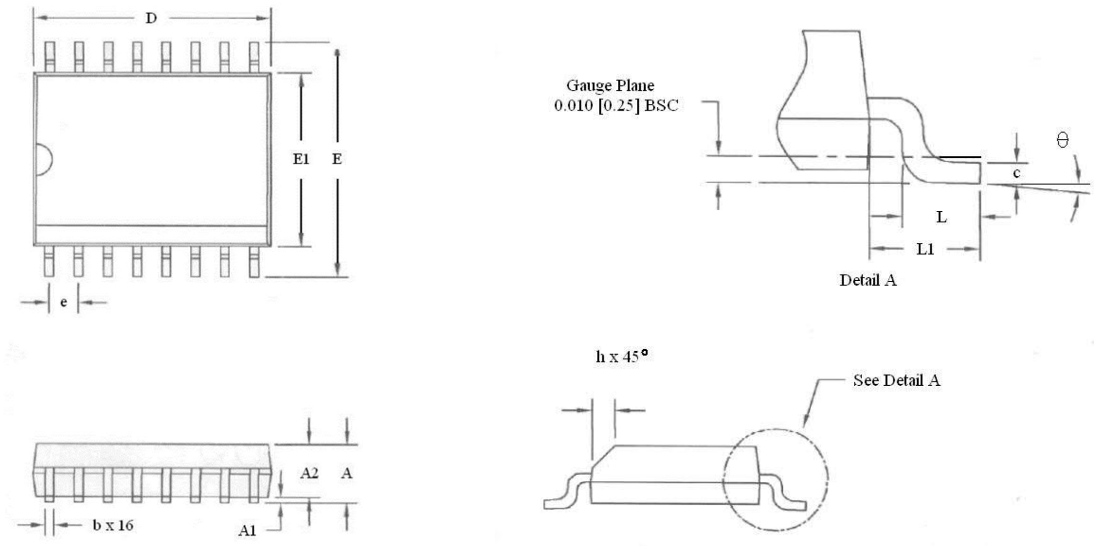
1. Currents flowing into the device are positive. Currents flowing out of the device are negative. Voltages are referenced to ground.
2. Guaranteed by design.
3. LEDx = 1V, VIN = 2.5V, FSET = 0.5V
4. If no -55C or 85C limits are stated, 25C limits apply at all temperatures.
5. Applies to SES part only. MES part TBD.

## PACKAGE DESCRIPTION

**Table 7 – Package Characteristics**

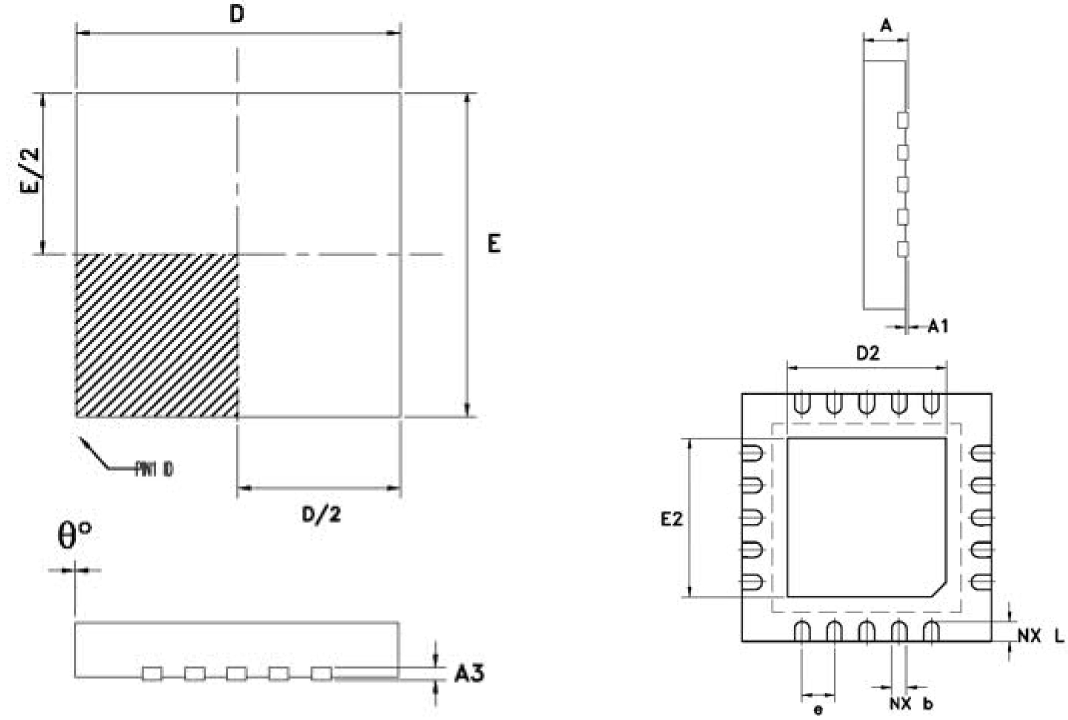
| PACKAGE TYPE | 20 QFN 5X5 G | 16 Lead WB SOIC - G |
|---|---|---|
| REFERENCE | 20 QFN 5X5 G | 16 Lead WB SOIC - G |
| **THERMAL RESISTANCE:** | | |
| $\theta_{JA}$ (4 layer PCB with Power Planes) | ~ 37 °C/W (see note) | 74 °C/W |
| $\theta_{JC}$ | ~ 7 °C/W | 24 °C/W |
| JEDEC MOISTURE SENSITIVITY LEVEL (MSL) | MSL 1 / 260°C | MSL 1 / 260°C |
| LEAD FINISH MATERIAL / JEDEC Pb-free CODE | NiPdAu | NiPdAu e4 |
| Pb-Free DESIGNATION | RoHS Compliant | RoHS Compliant |
| JEDEC REFERENCE | | MO-153-AC |
| **Note:** Exposed pad soldered to PCB land with thermal vias to internal ground plane. | | |

## *16 Lead WB SOIC, -G Package*




| DIMENSION IN INCHES | | | |
|---|---|---|---|
| SYM | MIN | NOM | MAX |
| A | 0.098 | 0.101 | 0.104 |
| A1 | 0.005 | 0.009 | 0.012 |
| A2 | 0.089 | 0.092 | 0.095 |
| b | 0.012 | 0.016 | 0.020 |
| c | 0.008 | 0.010 | 0.013 |
| D | 0.402 | 0.406 | 0.410 |
| E1 | 0.291 | 0.295 | 0.299 |
| E | 0.400 | 0.404 | 0.414 |
| e | 0.050 Typical | | |
| L | 0.016 | -- | 0.050 |
| L1 | 0.051 | 0.055 | 0.059 |
| θ | 0° | -- | 8° |
| h | 0.010 | 0.015 | 0.020 |

*20 Lead QFN 5X5, -G Package*




| Dimension | mm | | mils | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | 0.85 | 0.95 | 33.46 | 37.40 |
| A1 | 0 | 0.05 | 0 | 1.97 |
| A3 | 0.175 | 0.225 | 6.89 | 8.86 |
| D | 4.9 | 5.1 | 192.91 | 200.79 |
| E | 4.9 | 5.1 | 192.91 | 200.79 |
| D2 | 3.15 | 3.25 | 124.02 | 127.95 |
| E2 | 3.15 | 3.25 | 124.02 | 127.95 |
| e | 0.65BSC | | 25.59BSC | |
| NX b | 0.25 | 0.35 | 9.84 | 13.78 |
| NX L | 0.35 | 0.45 | 13.78 | 17.72 |
| θ° | 0° | 4° | 0° | 4° |

## ORDERING INFORMATION

| Part Number | Marking | Package | Temperature |
|---|---|---|---|
| DEI1090-MES-G | DEI1090 MES | 20 QFN 5X5 G | -55 ºC to +85 ºC |
| DEI1090-SES-G | DEI1090 E4 | 16 WB SOIC | -55 ºC to +85 ºC |

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