



YSS247

ASR

Analog Surround

■ OUTLINE

The YSS247 is a stereo signal processing LSI with Yamaha's original wide surround and control/loudness circuit.

With this LSI, it is possible to emphasize diffusion feeling of the sound when reproducing the stereo sound with a compact type audio equipments such as a mini-component set and an amplifier built-in speaker.

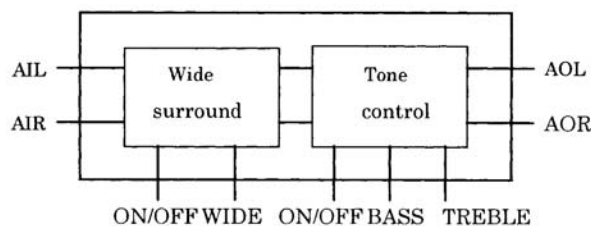
Also, since this LSI processes analog signals as they are, no micro-processor, A/D, D/A or memory is required.

■ FEATURES

- **Wide surround** Surround by amplitude phase conversion circuit
- **Tone control** BASS (100Hz \pm 10dB)、TREBLE (10KHz \pm 10dB) — recommended
- **Loudness** Either tone control or loudness selectable
- **Others** Wide surround ON/OFF switch
Wide surround wide control
Tone control ON/OFF switch
Tone control BASS, TREBLE control
All functions controlled by pin voltage
- **Operating voltage** Wide operating voltage range from 3.0V to 5.5V
- **Package** 20 SSOP(YSS247-E)
- **Process** Silicon gate CMOS process

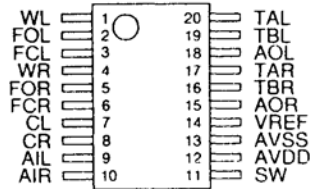
■ BLOCK DIAGRAM

Wide surround + tone control



■ PIN CONFIGURATION

20SSOP
(YSS247-E)



■ PIN FUNCTION

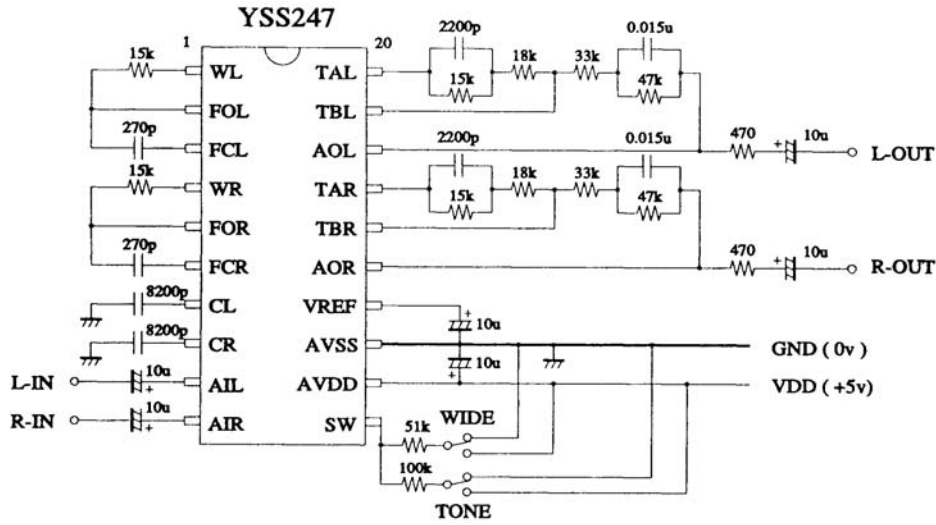
Pin No. 20 SSOP	Pin name	Function
1	WL	3D Lch Wide Input
2	FOL	3D Lch Filter Output
3	FCL	3D Lch Capacitor
4	WR	3D Rch Wide Input
5	FOR	3D Rch Filter Output
6	FCR	3D Rch Capacitor
7	CL	3D Lch Capacitor
8	CR	3D Rch Capacitor
9	AIL	Lch Input
10	AIR	Rch Input
11	SW	3D & Tone Control ON/OFF
12	AVDD	Power Supply
13	AVSS	GND
14	VREF	Voltage Reference
15	AOR	Rch Output
16	TBR	Rch Tone Control(B)
17	TAR	Rch Tone Control(A)
18	AOL	Lch Output
19	TBL	Lch Tone Control(B)
20	TAL	Lch Tone Control(A)

■ DESCRIPTION OF PIN FUNCTION

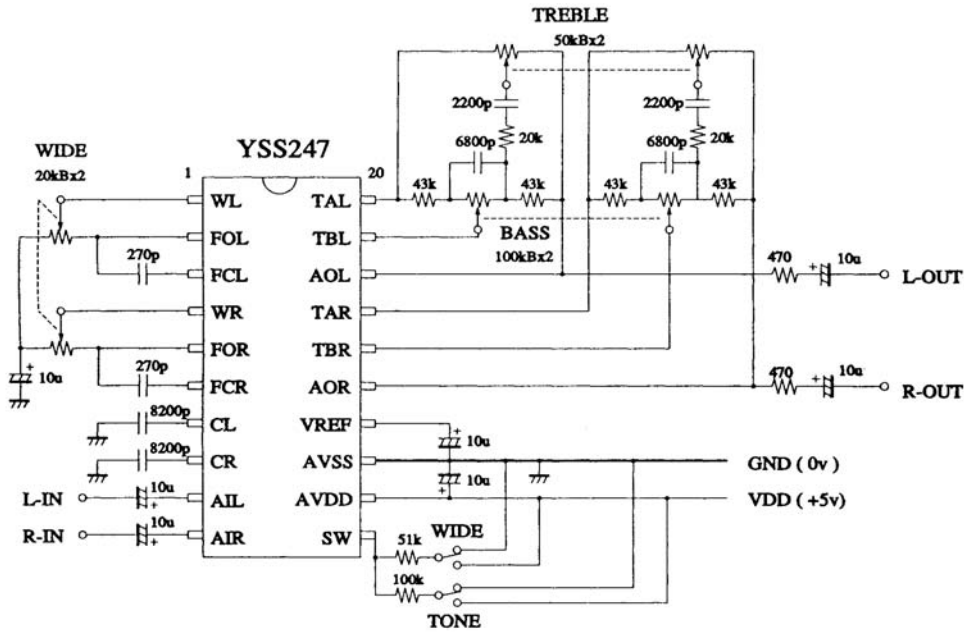
1. WL (1 pin) Lch Wide input terminal
WR (4 pin) Rch Wide input terminal
The surround effect is provided when the FOL output is inputted to WL and the FOR output to WR, both after the level adjustment.
2. FOL (2 pin) Lch Filter output terminal
FOR (5 pin) Rch Filter output terminal
Connect a capacitance between FOL and FCL and between FOR and FCR.
3. FCL (3 pin) Lch filter capacitance connection terminal
FCR (6 pin) Rch filter capacitance connection terminal
Refer to the above paragraph.
4. CL (7 pin) Lch filter capacitance connection terminal
CR (8 pin) Rch filter capacitance connection terminal
Connect a capacitance between CL and GND and between CR and GND.
5. AIL (9 pin) Lch analog input terminal
AIR (10 pin) Rch analog input terminal
To AIL, connect a capacitor and input the Lch signal.
To AIR, connect a capacitor and input the Rch signal.
6. SW (11 pin) Surround, tone control function on/off terminal
With 2 resistors (51k Ω , 100k Ω) connect one ends to this pin and connect the other ends to AVDD (ON) or AVSS (OFF) surround (51k Ω) and tone control (100k Ω) function ON/OFF can be controlled.
7. AVDD (12 pin) Power supply terminal
Apply +3.0 to +5.5V voltage to the AVSS potential.
Connect a capacitance between AVDD and AVSS.
8. AVSS (13 pin) GND terminal
Analog signal reference voltage pin
9. VREF (14 pin) Operating voltage
(AVDD-AVSS)/2 potential is generated to provide the center voltage of the internal circuit.
Connect a capacitance between this pin and AVSS.
10. AOR (15 pin) Rch analog output terminal
AOL (18 pin) Lch analog output terminal
With a capacitance connected to AOR and AOL, analog signals are output.
11. TBR (16 pin), TAR (17 pin) Rch tone control input terminals
TBL (19 pin), TAL (20 pin) Lch tone control input terminals
The Rch tone control circuit is formed by using the CR circuit among AOR, TBR and TAR.
The Lch tone control circuit is formed by using the CR circuit among AOL, TBL and TAL.
(Refer to the application circuit example.)

■ APPLICATION CIRCUIT EXAMPLE

Simple circuit example using ON/OFF switch



Circuit example with volume variable surround and tone control effects.



The YSS247 can be used by changing the constant of the external parts according to application and conditions.

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Item	Symbol	min.	max.	Unit
Power supply voltage	AVDD	AVSS-0.5	AVSS+7.0	V
Input voltage	V _{in}	AVSS-0.5	AVDD+0.5	V
Output voltage	V _{out}	AVSS-0.3	AVDD+0.3	V
Storage temperature	T _{stg}	-50	125	°C

2. Recommended operating conditions

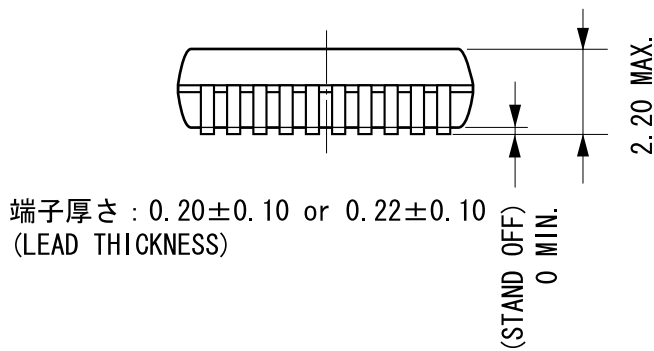
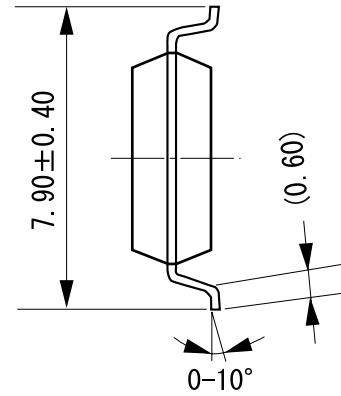
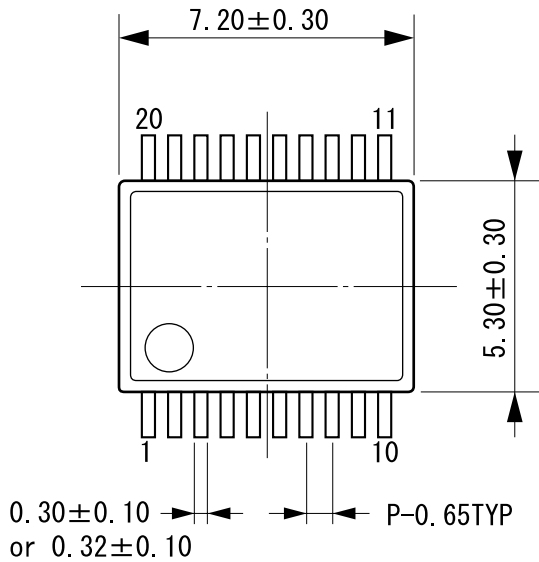
Item	Symbol	min.	typ.	max.	Unit
Power supply voltage	AVDD	3.0	5.0	5.5	V
Operating temperature	Top	0	25	70	°C

3. Analog characteristics (Conditions : Ta=25°C, VDD=5.0V)

Item	Symbol	min.	typ.	max.	Unit
Power supply current	VDD=5.0V	—	10	—	mA
Analog input voltage		—	1.0	—	V _{rms}
Analog output voltage		—	1.0	—	V _{rms}
Signal noise ratio	IHF-A	—	95	—	dB
Distortion rate	1 V _{rms} input Wide, Tone off	—	0.0025	—	%
Gain deviation		—	—	0.5	dB
Frequency characteristic	10 Hz~50 kHz	-3.0	—	0.5	dB
Input impedance		—	30	—	k Ω
Input capacitance		—	—	15	pF
Center voltage		—	2.5	—	V

EXTERNAL DIMENSIONS
● YSS247-E (SSOP specification)

C-PK20EP-1



モールドコーナー形状は、この図面と若干異なるタイプもあります。
 カッコ内の寸法値は参考値です。
 モールド外形寸法はバリを含みません。
 単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
 The figure in the parentheses () should be used as a reference.
 Plastic body dimensions do not include resin burr.
 UNIT: mm

注) 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
 詳しくはヤマハ代理店までお問い合わせください。
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