Philips Components

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TDA8703/TDA8703T

8-bit high-speed analog-to-digital converter

FEATURES

- 8-bit resolution
- Sampling rate up to 40 MHz
- High signal-to-noise ratio over a large analog input frequency range (7.1 effective bits at 4.43 MHz full-scale input)
- Binary or two's complement 3-state TTL outputs
- Overflow/underflow 3-state TTL output
- TTL compatible digital inputs
- Low-level AC clock input signal allowed
- Internal reference voltage generator
- Power dissipation only 290 mW (typical)
- Low analog input capacitance, no buffer amplifier required
- No sample and hold circuit required

APPLICATIONS

- High-speed analog-to-digital conversion for:
  - video data digitizing
  - radar pulse analysis
  - transient signal analysis
  - high energy physics research
  - $\Sigma\Delta$ modulators

DESCRIPTION

The TDA8703 is a monolithic bipolar 8-bit high-speed analog-to-digital converter (ADC) for video and other applications. It converts the analog input signal into 8-bit binary-coded digital words at a maximum sampling rate of 40 MHz. All digital inputs and outputs are TTL compatible, although a low-level AC clock input signal is allowed.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8703	24	DIL	plastic	SOT101
TDA8703T	24	SO24	plastic	SOT137A

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		-	28	36	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stages supply current		-	11	14	V
ILE	DC integral linearity error		-	-	± 1	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 1	-	-	± 2	LSB
B	−3 dB bandwidth	note 2; f_{CLK} = 40 MHz	-	19.5	-	MHz
$f_{CLK}/f_{\overline{CLK}}$	maximum conversion rate	note 3	40	-	-	MHz
P_{tot}	total power dissipation		-	290	415	mW

Notes to the Quick Reference Data

1. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
2. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at input).
3. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4): When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

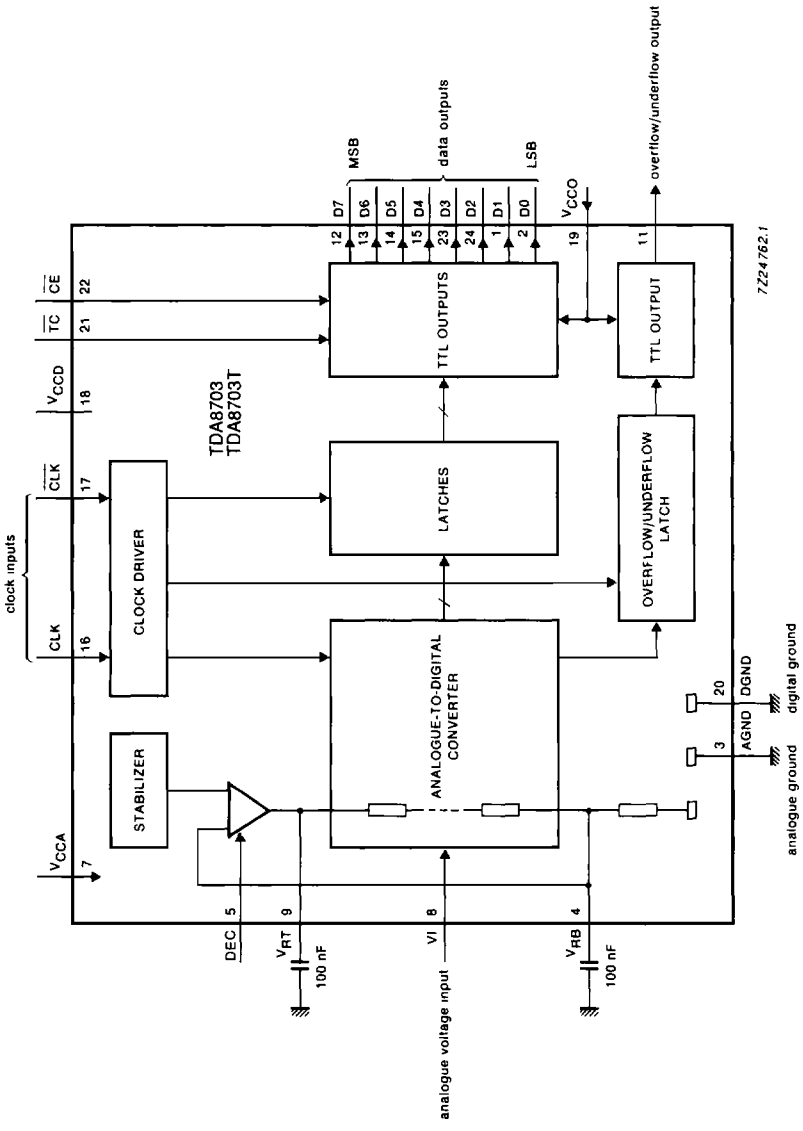

Fig.1 Block diagram.

PIN CONFIGURATION

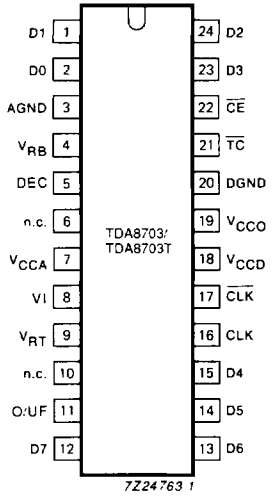

Fig.2 Pin configuration.

PINNING

SYMBOL	PIN	DESCRIPTION
D1	1	data output, bit 1
D0	2	data output, bit 0 (LSB)
AGND	3	analog ground
V_{RB}	4	reference voltage bottom (decoupling)
DEC	5	decoupling input (internal stabilization loop decoupling)
n.c.	6	not connected
V_{CCA}	7	positive supply voltage for analog circuits (+5 V)
VI	8	analog voltage input
V_{RT}	9	reference voltage top (decoupling)
n.c.	10	not connected
O/UF	11	overflow/underflow data output
D7	12	data output, bit 7 (MSB)
D6	13	data output, bit 6
D5	14	data output, bit 5
D4	15	data output, bit 4
CLK	16	clock input
$\overline{CLK}$	17	complementary clock input
V_{CCD}	18	positive supply voltage for digital circuits (+5 V)
V_{CCO}	19	positive supply voltage for output stages (+5 V)
DGND	20	digital ground
$\overline{TC}$	21	input for two's complement output (TTL level input, active LOW)
$\overline{CE}$	22	chip enable input (TTL level input, active LOW)
D3	23	data output, bit 3
D2	24	data output, bit 2

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage range		−0.3	7.0	V
V_{CCD}	digital supply voltage range		−0.3	7.0	V
V_{CCO}	output stages supply voltage		−0.3	7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCO} - V_{CCD}$	supply voltage differences		−1.0	1.0	V
$V_{CCA} - V_{CCO}$	supply voltage differences		−1.0	1.0	V
V_{VI}	input voltage range	referenced to AGND	−0.3	7.0	V
$V_{CLK(p-p)}$/ $V_{\overline{CLK}(p-p)}$	AC input voltage for switching (peak-to-peak value)	see note; referenced to DGND	-	2.0	V
I_O	output current		-	+ 10	mA
T_{stg}	storage temperature range		−55	+ 150	°C
T_{amb}	operating ambient temperature range		0	+ 70	°C
T_j	junction temperature		-	+ 125	°C

Notes to the Ratings

The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:

- TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
- TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
- AC drive modes (modes 3 and 4): When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.

If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.

THERMAL RESISTANCE

SYMBOL	PACKAGE	TYP.	UNIT
$R_{th\ j-a}$	SOT101	+ 55	K/W
$R_{th\ j-a}$	SOT137A	+ 75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS (see Tables 1 and 2)

$V_{CCA} = V_7 - V_3 = 4.5$ V to 5.5 V; $V_{CCD} = V_{18} - V_{20} = 4.5$ V to 5.5 V; $V_{CCO} = V_{19} - V_{20} = 4.5$ V to 5.5 V; AGND and DGND shorted together; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCO} - V_{CCD} = -0.5$ V to +0.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; $T_{amb} = 0$ °C to +70 °C; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = V_{CCO} = 5.0$ V and $T_{amb} = 25$ °C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	output stages supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current		-	28	36	mA
I_{CCD}	digital supply current		-	19	25	mA
I_{CCO}	output stage supply current	all outputs LOW	-	11	14	mA
Inputs CLOCK INPUT $\overline{CLK}$ AND CLK (note 1; referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V	-400	-	-	µA
I_{IH}	input current HIGH	$V_{CLK}/V_{\overline{CLK}} = 0.4$ V $V_{CLK}/V_{\overline{CLK}} = V_{CCD}$	- -	- -	100 300	µA µA
Z_o	input impedance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4	-	kΩ
C	input capacitance	$f_{CLK}/f_{\overline{CLK}} = 10$ MHz	-	4.5	-	pF
$V_{CLKip-p} - V_{\overline{CLK}ip-p}$	AC input voltage for switching (peak-to-peak value)	note 1; DC level = 1.5 V	0.5	-	2.0	V
INPUTS $\overline{TC}$ AND $\overline{CE}$ (referenced to DGND)						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.0	-	V_{CCD}	V
I_{IL}	input current LOW	$V_{IL} = 0.4$ V	-400	-	-	µA
I_{IH}	input current HIGH	$V_{IH} = 2.7$ V	-	-	20	µA
VI (analog input voltage referenced to AGND)						
V_{VI}	input voltage	output code = 0 output code = 255	1.54 3.3	1.61 3.4	1.69 3.5	V V
V_{VIp-p}	input voltage amplitude (peak-to-peak value)		1.72	1.79	1.85	V
I_{IL}	input current LOW	$V_{VI} = 1.4$ V	-	0	-	µA
I_{IH}	input current HIGH	$V_{VI} = 3.6$ V	60	120	180	µA
Z_o	input impedance	$f_i = 1$ MHz	-	10	-	kΩ
C_i	input capacitance	$f_i = 1$ MHz	-	14	-	pF
Reference resistance						
R_{ref}	reference resistance	V_{RT} to V_{RB}	-	220	-	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
DIGITAL OUTPUTS (D7 – D0) (referenced to DGND)						
V_{OL}	output voltage LOW	I_O = 1 mA	0	-	0.4	V
V_{OH}	output voltage HIGH	I_O = −0.4 mA	2.7	-	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	−20	-	20	μA
Switching characteristics (note 2; see Fig.3)						
$f_{CLK}/\overline{f_{CLK}}$	maximum clock frequency		40	-	-	MHz
Analog signal processing (f_{CLK} = 40 MHz)						
B	−3 dB bandwidth	note 3	-	19.5	-	MHz
G_d	differential gain	note 4	-	0.6	-	%
o_d	differential phase	note 4	-	0.8	-	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz	-	-	0	dB
f_{all}	harmonics (full-scale). all components	f_i = 4.43 MHz	-	−55	-	dB
SVR1	supply voltage ripple rejection	note 5	-	−28	−25	dB
SVR2	supply voltage ripple rejection	note 5	-	1	2.5	%/V
Transfer function (f_{CLK} = 40 MHz)						
ILE	DC integral linearity error		-	-	± 1	LSB
DLE	DC differential linearity error		-	-	±1/2	LSB
AILE	AC integral linearity error	note 6	-	-	± 2	LSB
	effective bits	f_i = 4.43 MHz	-	7.1	-	bits
Timing (note 7; see Figs 3 to 6; f_{CLK} = 40 MHz)						
t_{dS}	sampling delay		-	-	2	ns
t_{HD}	output hold time		6	-	-	ns
t_{dLH}	output delay time	LOW-to-HIGH transition	-	8	10	ns
t_{dHL}	output delay time	HIGH-to-LOW transition	-	14	16	ns
t_{dZH}	3-state output delay times	enable-to-HIGH	-	19	25	ns
t_{dZL}	3-state output delay times	enable-to-LOW	-	16	20	ns
t_{dHZ}	3-state output delay times	disable-to-HIGH	-	14	20	ns
t_{dLZ}	3-state output delay times	disable-to-LOW	-	9	12	ns

Notes to the characteristics

1. The circuit has two clock inputs CLK and $\overline{CLK}$. There are four modes of operation:
   - TTL (mode 1); $\overline{CLK}$ decoupled to DGND by a capacitor. CLK input is TTL threshold voltage of 1.5 V and sampling on the LOW-to-HIGH transition of the input clock signal.
   - TTL (mode 2); CLK decoupled to DGND by a capacitor. $\overline{CLK}$ input is TTL threshold voltage of 1.5 V and sampling on the HIGH-to-LOW transition of the input clock signal.
   - AC drive modes (modes 3 and 4); When driving the CLK input directly and with any AC signal of 0.5 V (peak-to-peak value) imposed on a DC level of 1.5 V, sampling takes place on the LOW-to-HIGH transition of the clock signal. When driving the $\overline{CLK}$ input with such a signal, sampling takes place on the HIGH-to-LOW transition.
   - If one of the clock inputs is not driven, then it is recommended to decouple this input to DGND with a 100 nF capacitor.
2. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock must not be less than 2 ns.
3. The −3 dB bandwidth is determined by the 3 dB reduction in the reconstructed output (full-scale signal at the input).
4. Low frequency ramp signal ($V_{VI(p-p)}$ = 1.8 V and f_i = 15 kHz) combined with a sinewave input voltage ($V_{VIp-p)}$ = 0.5 V, f_i = 4.43 MHz) at the input.
5. Supply voltage ripple rejection:
   - SVR1; variation of the input voltage producing output code 127 for supply voltage variation of 1 V:
     SVR1 = 20 log $(\Delta V_{VI(127)} \div \Delta V_{CCA})$
   - SVR2; relative variation of the full-scale range of analog input for a supply voltage variation of 1 V:
     SVR2 = $\left(\Delta(V_{VI(0)} - V_{VI(255)}) \div (V_{VI(0)} - V_{VI(255)})\right) \div \Delta$VCCA.
6. Full-scale sinewave (f_i = 4.4 MHz; $f_{CLK}/f_{\overline{CLK}}$ = 27 MHz).
7. Output data acquisition
   - Output data is available after the maximum delay of t_{dHL} and t_{dLH}.
   - Output data is fully stable during the low level of the clock. Thus, it is recommanded that acquisition of this data is made after the falling edge of the clock, instead of after the max (t_{dHL}, t_{dLH}).

Table 1 Output coding and input voltage (typical values; referenced to AGND)

			BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
STEP	$V_{VI(P-P)}$	O/UF	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
underflow	<1.65	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1.65	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	.	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
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.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	.	0	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	3.45	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
overflow	>3.45	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Table2 Mode selection

$\overline{TC}$	$\overline{CE}$	D7 – D0	O/UF
X	1	high impedance	high impedance
0	0	active; two's complement	active
1	0	active; binary	active

Where:

X = don't care.

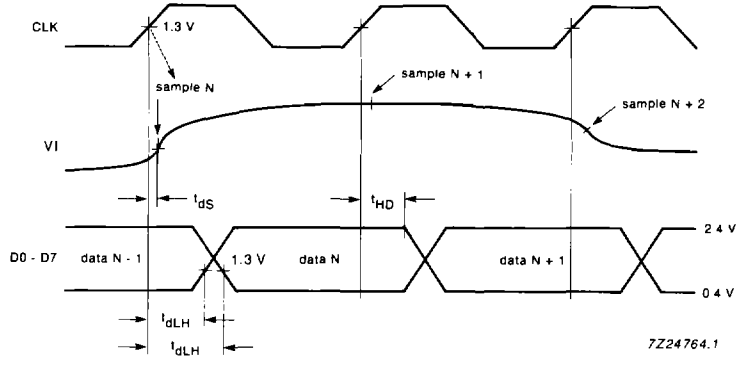

Fig.3 Timing diagram.

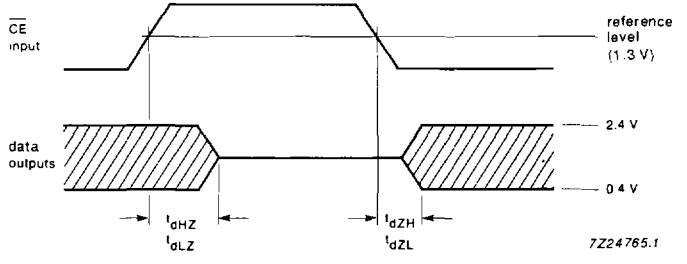

Fig.4 3-state delay timing diagram.

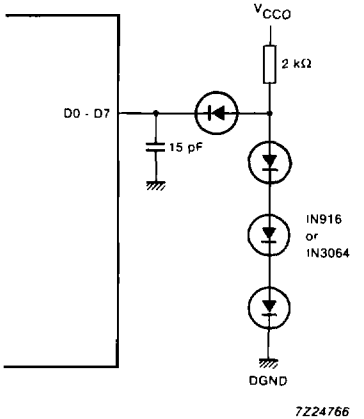

Fig.5 Load circuit for timing measurement; data outputs ($\overline{CE}$ = LOW).

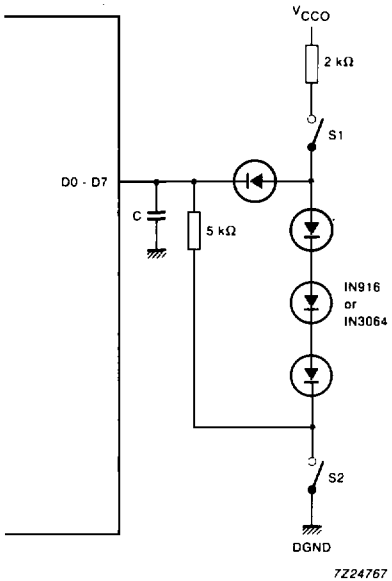

Fig.6 Load circuit for timing measurement; 3-state outputs ($\overline{CE}$: f_i = 1 MHz: V_{VI} = 3 V).

Note to Fig.6

TIMING MEASUREMENT	SWITCH S1	SWITCH S2	CAPACITOR C
t_{dZH}	open	closed	15 pF
t_{dZL}	closed	open	15 pF
t_{dHZ}	closed	closed	5 pF
t_{dLZ}	closed	closed	5 pF

INTERNAL PIN CONFIGURATIONS

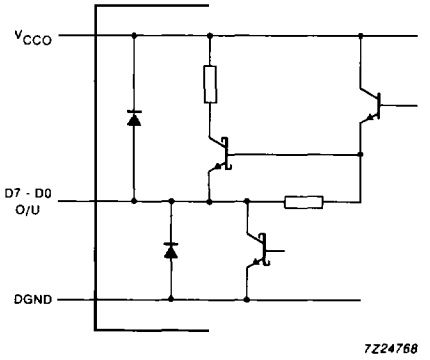

Fig.7 TTL data and overflow/underflow outputs.

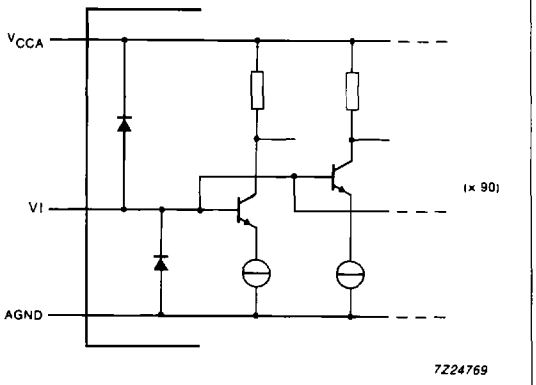

Fig.8 Analog inputs.

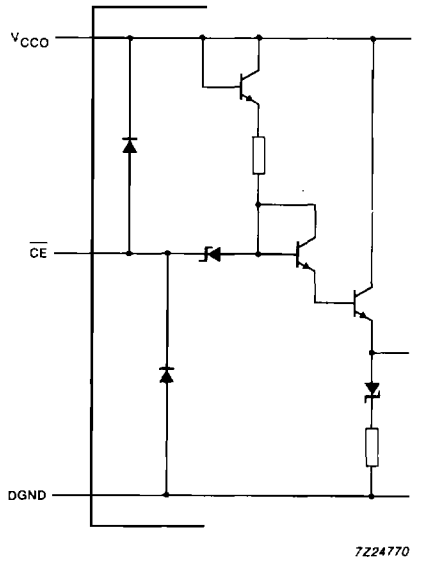

Fig.9 $\overline{CE}$ (3-state) input.

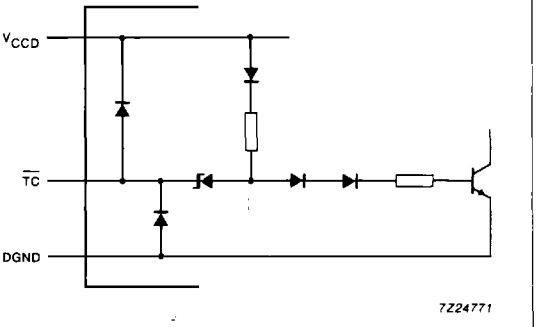

Fig.10 $\overline{TC}$ (two's complement) input.

INTERNAL PIN CONFIGURATIONS (continued)

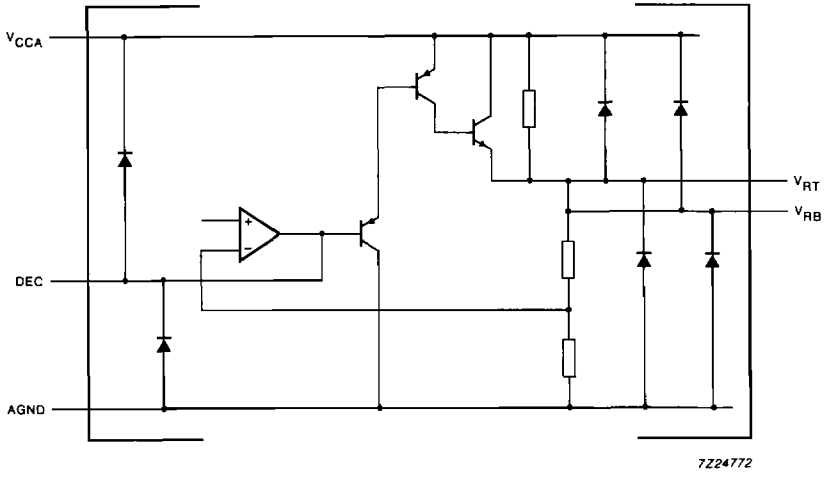

Fig.11 V_{RB}, V_{RT} and DEC.

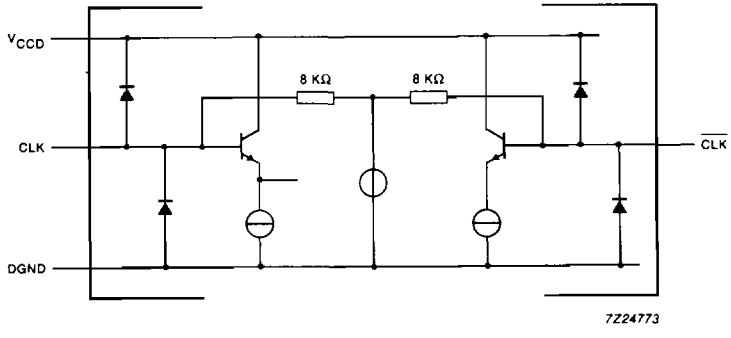

Fig.12 CLK and $\overline{CLK}$ inputs.

APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).

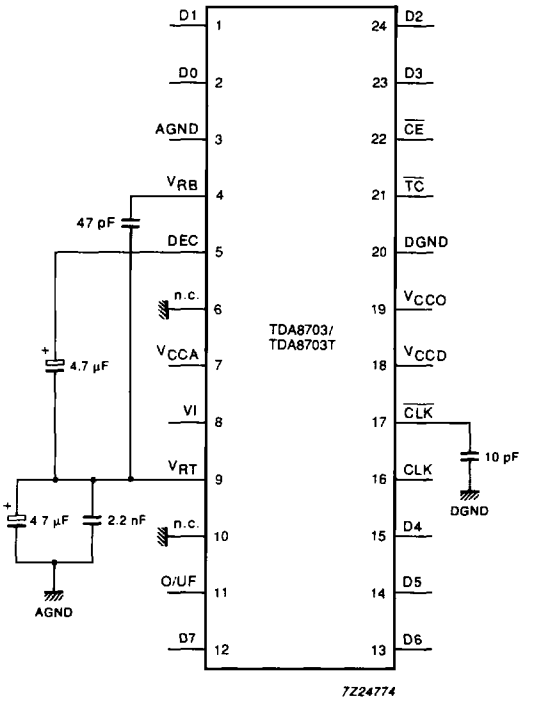

Fig.13 Application diagram.

Notes to Fig.13

1. CLK should be decoupled to the DGND with a 100 nF capacitor, if a TTL signal is used on CLK (see 'Notes to the characteristics', note 1).
2. CLK and $\overline{CLK}$ can be used in a differential mode (see 'Notes to the characteristics', note 1).
3. V_{RB} and V_{RT} are decoupling pins for the internal reference ladder; do not draw current from these pins in order to achieve good linearity.
4. Analog and digital supplies should be separated and decoupled.
5. Pins 6 and 10 should be connected to AGND in order to prevent noise influence.