PYRAMID SEMICONDUCTOR CORPORATION

P4C164LL

VERY LOW POWER 8KX8 STATIC CMOS RAM

FEATURES

- **V_{CC} Current (Commercial/Industrial)**
  - **— Operating: 55 mA**
  - **— CMOS Standby: 3 µA**
- **Access Times**
  - **—80/100 (Commercial or Industrial)**
  - **—90/120 (Military)**
- **Single 5 Volts ±10% Power Supply**
- **Easy Memory Expansion Using $\overline{CE}_1$, CE_2 and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
  - **—28-Pin 300 and 600 mil DIP**
  - **—28-Pin 330 mil SOP**

DESCRIPTION

The P4C164LL is a 64K density low power CMOS static RAM organized as 8Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

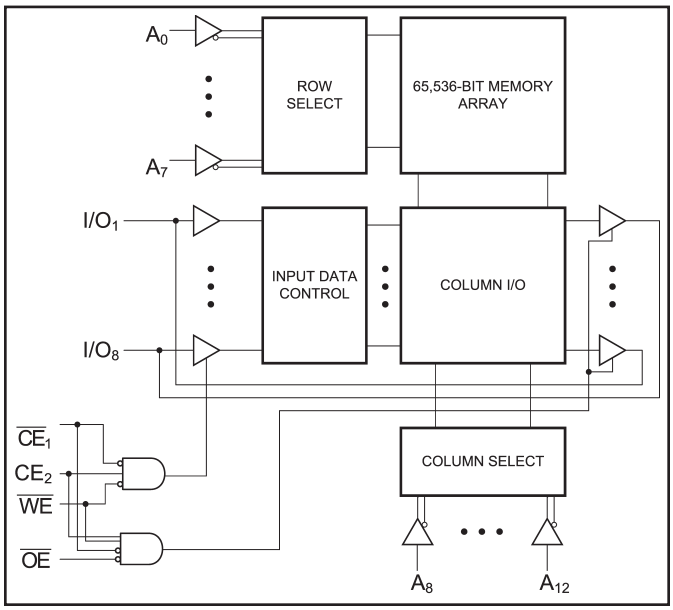
Access times of 80 and 100 ns are available for commercial and industrial temperatures; access times of 90 and 100 ns are available for military temperature. CMOS is utilized to reduce power consumption to a low level.

The P4C164LL device provides asynchronous operation with matching access and cycle times.

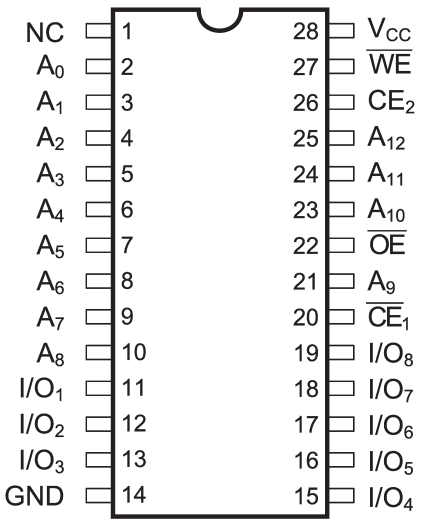
Memory locations are specified on address pins A_0 to A_{12}. Reading is accomplished by device selection ($\overline{CE}_1$ LOW, CE_2 HIGH) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}_1$ or $\overline{OE}$ is HIGH or $\overline{WE}$ or CE_2 is LOW.

Package options for the P4C164LL include 28-pin 300 and 600 mil DIP and 28-pin 330 mil SOP packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P5, P6, C5-1), SOP (S5)
TOP VIEW

RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Grade	Ambient Temp	Supply Voltage
Commercial	0°C to 70°C	$4.5V \le V_{CC} \le 5.5V$
Industrial	-40°C to +85°C	$4.5V \le V_{CC} \le 5.5V$
Military	-55°C to +125°C	$4.5V \le V_{CC} \le 5.5V$

MAXIMUM RATINGS(1)

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage with Respect to GND	-0.5	7.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	VCC + 0.5	V
T_A	Operating Ambient Temperature	-55	125	°C
S_{TG}	Storage Temperature	-65	150	°C
I_{OUT}	Output Current into Low Outputs		25	mA
I_{LAT}	Latch-up Current	> 200		mA

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)(2)

Sym	Parameter	Test Conditions		Min	Max	Unit
V_{OH}	Output High Voltage (I/O_0 - I/O_7)	I_{OH}= -1mA, V_{CC} = 4.5V		2.4		V
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 2.1mA			0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.5(3)	0.8	V
I_{LI}	Input Leakage Current	$GND \le V_{IN} \le V_{CC}$	Com / Ind	-2	+2	µA
			Military	-5	+5	
I_{LO}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE_1} \ge V_{IH}$	Com / Ind	-2	+2	µA
			Military	-10	+10	
I_{SB}	V_{CC} Current TTL Standby Current (TTL Input Levels)	V_{CC} = 5.5V, I_{OUT} = 0 mA, $\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$	Com / Ind		100	µA
			Military		400	
I_{SB1}	V_{CC} Current CMOS Standby Current (CMOS Input Levels)	V_{CC} = 5.5V, I_{OUT} = 0 mA, $\overline{CE_1} \ge V_{CC}$ - 0.2V or $CE_2 \le 0.2V$	Com / Ind		3	µA
			Military		25	

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

CAPACITANCES[4]

Symbol	Parameter	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	*				
			-80	-90	-100	-120	Unit
I_{CC}	Dynamic Operating Current	Com / Ind / Military	55	55	55	55	mA

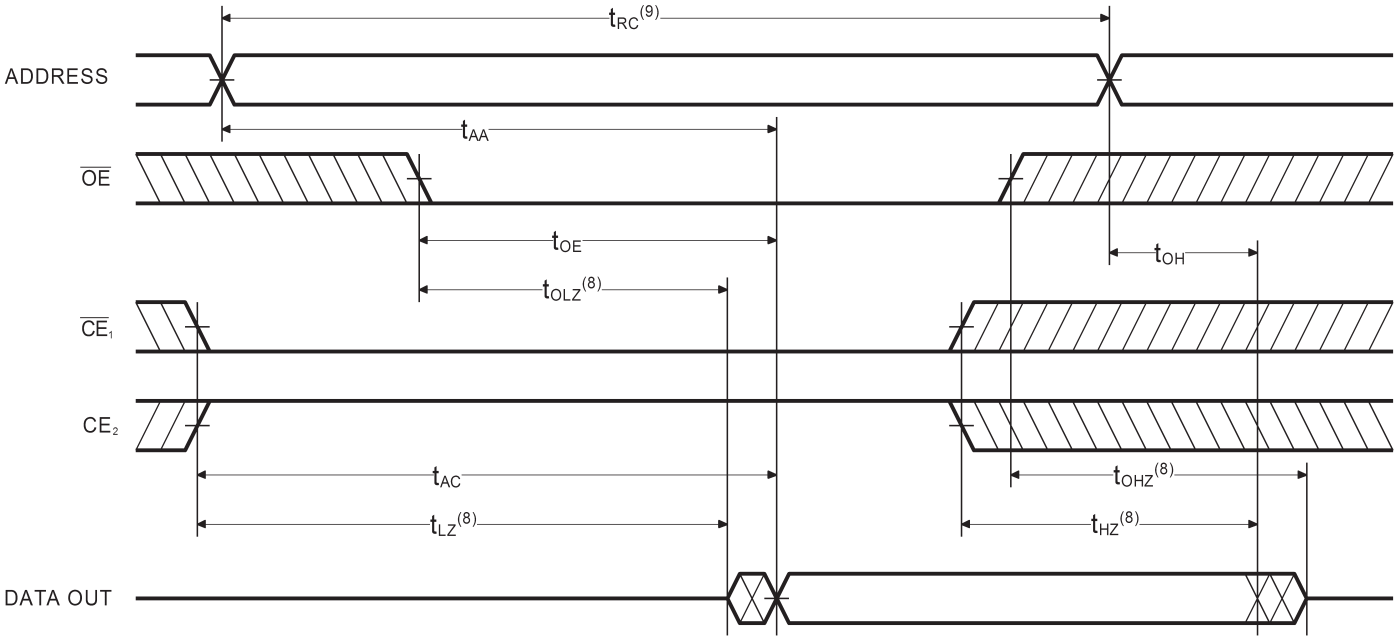
* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e. $\overline{CE}_1$ and $\overline{WE} \le V_{IL}$ (max), $\overline{OE}$ is high. Switching inputs are 0V and 3V.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

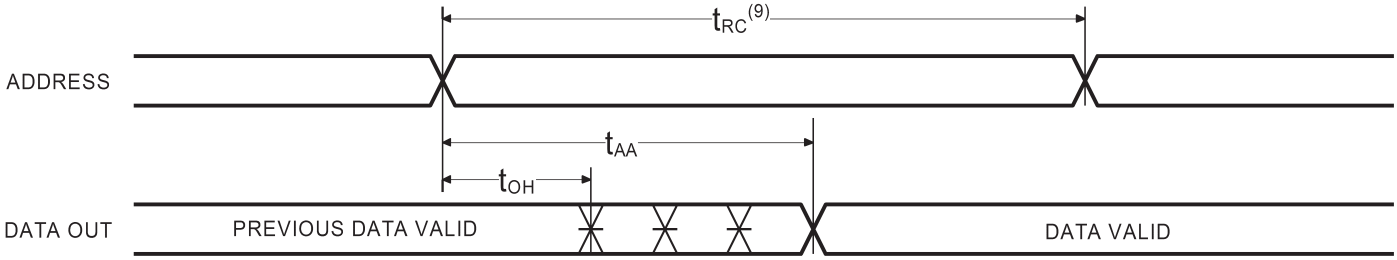
(Over Recommended Operating Temperature & Supply Voltage)

Sym	Parameter	-80		-90		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	80		90		100		120		ns
t_{AA}	Address Access Time		80		90		100		120	ns
t_{AC}	Chip Enable Access Time		80		90		100		120	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z		30		30		30		30	ns
t_{OE}	Output Enable Low to Data Valid		40		40		40		40	ns
t_{OLZ}	Output Enable Low to Low Z	5		5		5		5		ns
t_{OHZ}	Output Enable High to High Z		20		20		20		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		80		90		100		120	ns

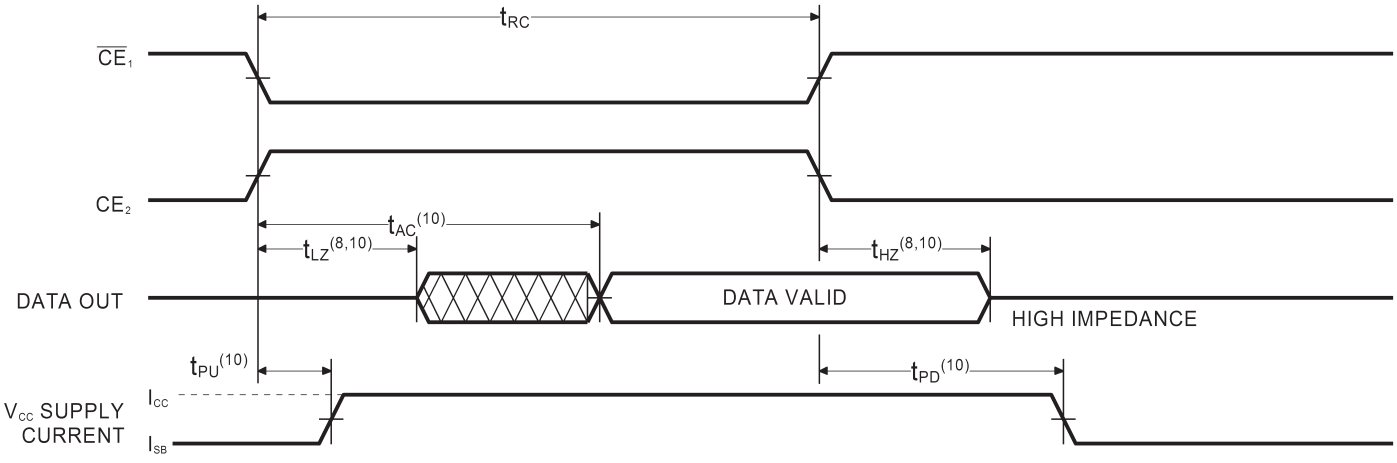
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[1]



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE_1}$, CE_2 CONTROLLED)



Notes:

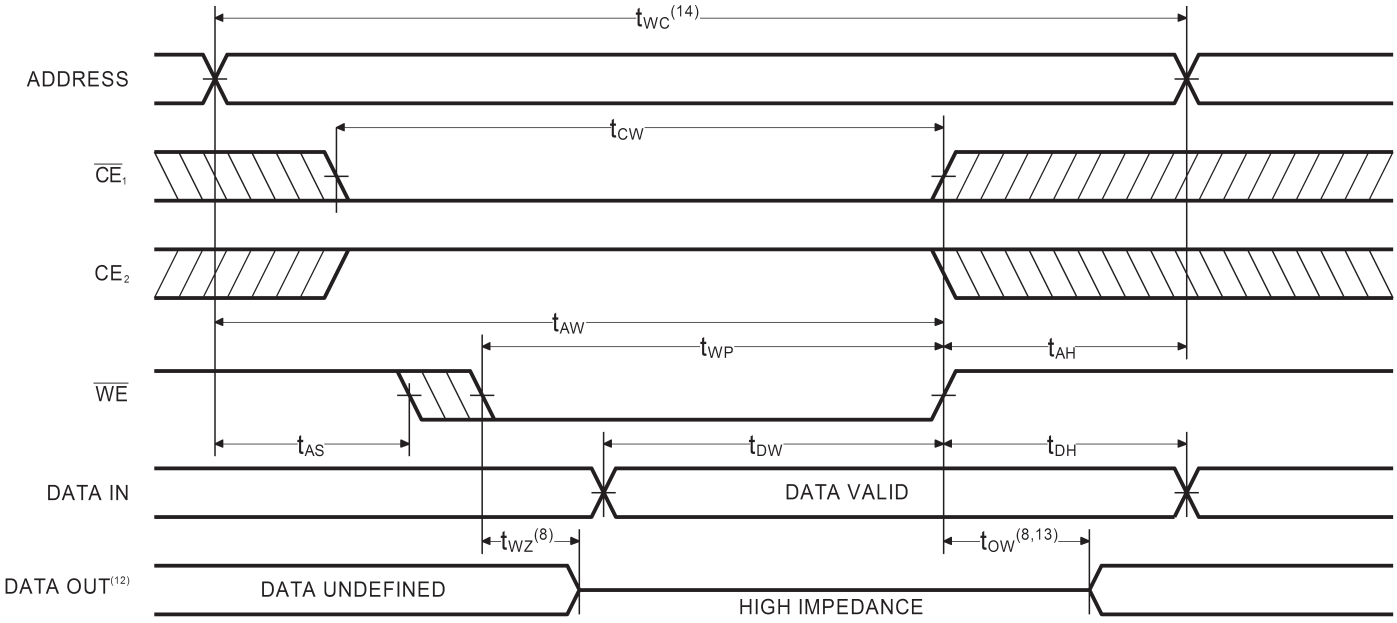
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE_1}$ or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-80		-90		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	80		90		100		120		ns
t_{CW}	Chip Enable Time to End of Write	70		80		80		100		ns
t_{AW}	Address Valid to End of Write	70		80		80		100		ns
t_{AS}	Address Setup Time	0		0		0		0		ns
t_{WP}	Write Pulse Width	60		60		60		60		ns
t_{AH}	Address Hold Time	0		0		0		0		ns
t_{DW}	Data Valid to End of Write	40		40		40		40		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		30		30		30		30	ns
t_{OW}	Output Active from End of Write	10		10		10		10		ns

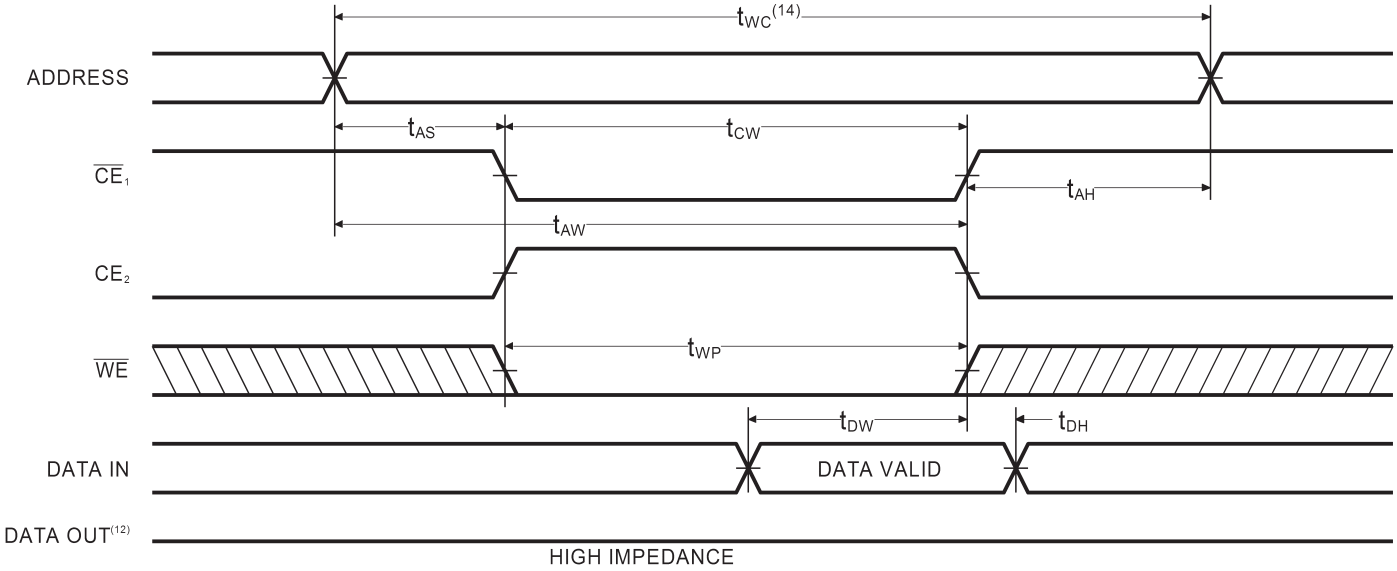
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[6]



Notes:

11. $\overline{CE_1}$ and $\overline{WE}$ must be LOW, and CE_2 HIGH for WRITE cycle.
12. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE_1}$ goes HIGH, or CE_2 goes LOW, simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (CE CONTROLLED)[6]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

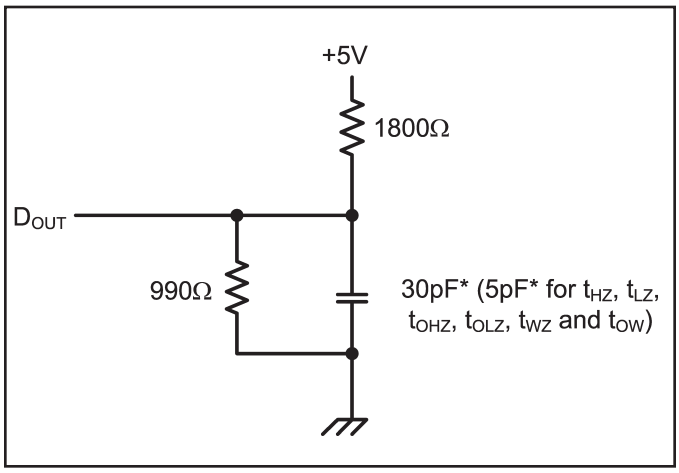


Figure 1. Output Load

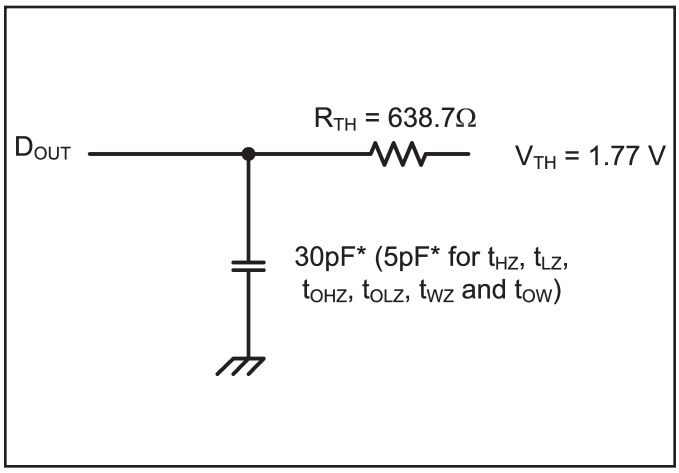


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C164LL, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589Ω resistor must be used in series with D_{OUT} to match 639Ω (Thevenin Resistance).

DATA RETENTION CHARACTERISTICS

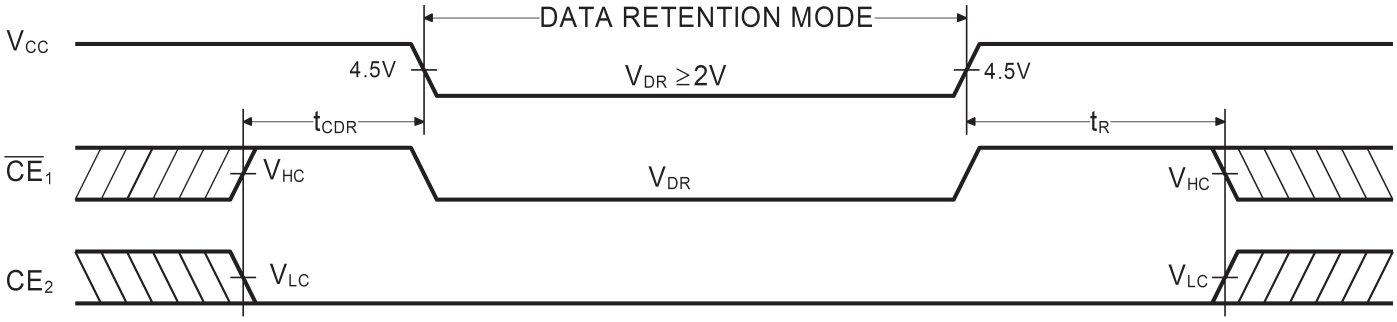
Symbol	Parameter	Test Condition	Min	Typ. * V_{CC} = 2.0V	Typ. * V_{CC} = 3.0V	Max V_{CC} = 2.0V	Max V_{CC} = 3.0V	Unit
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE_1} \geq V_{CC}$ - 0.2V or		1	2	3	4	µA
t_{CDR}	Chip Deselect to Data Retention Time	$CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or	0					ns
t_R†	Operation Recovery Time	$V_{IN} \leq 0.2V$	t_{RC}§					ns

* $_{TA}$ = +25°C

§t_{RC} = Read Cycle Time

† This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM



ORDERING INFORMATION

P4C164LL — xx x x LF

Device Type | Speed | Package | Processing | Lead Free

Lead Free Designation (LF=RoHS compliant (Plastic only); Blank=Standard)

Processing:
- C 0°C to +70°C
- I -40°C to +85°C
- M -55°C to +125°C
- MB Mil Temp with MIL-STD-883, Class B compliance

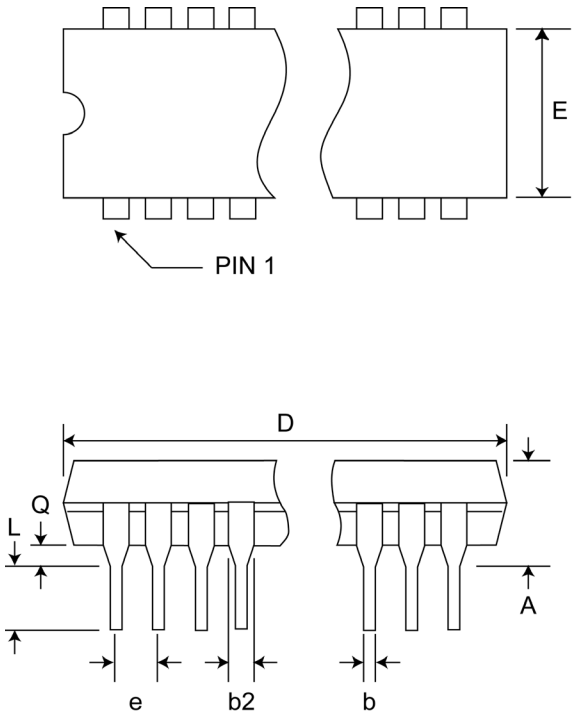
Package:
- S Plastic SOP, 330 mil
- P3 Plastic DIP, 300 mil
- P6 Plastic DIP, 600 mil
- CW Ceramic DIP, 600 mil

Speed: 80, 90, 100, 120 ns

Device Type: 8K x 8 VERY LOW POWER SRAM

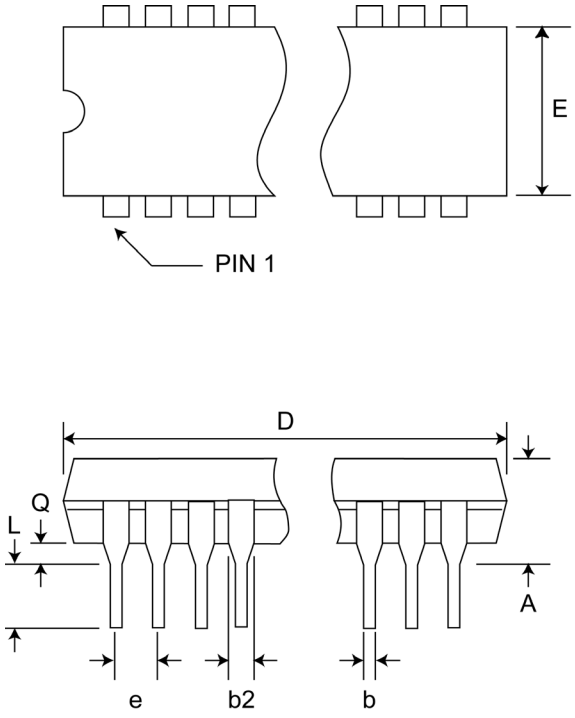
Pkg #	P5	
# Pins	28 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1		-
b	0.014	0.023
b2	0.045	0.070
C	0.008	0.014
D	1.345	1.400
E1	0.270	0.300
E	0.300	0.380
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE (300 mil)



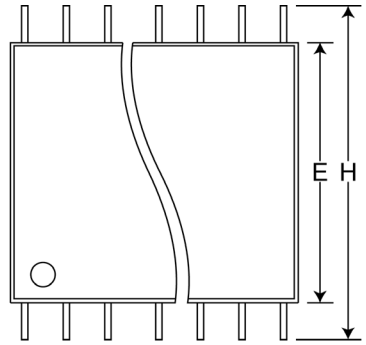
Pkg #	P6	
# Pins	28 (600 mil)	
Symbol	**Min**	**Max**
A	0.090	0.200
A1	0.000	0.070
b	0.014	0.020
b2	0.015	0.065
C	0.008	0.012
D	1.380	1.480
E1	0.485	0.550
E	0.600	0.625
e	0.100 BSC	
eB	0.600 TYP	
L	0.100	0.200
α	0°	15°

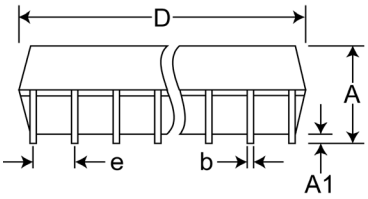
PLASTIC DUAL IN-LINE PACKAGE (600 mil)

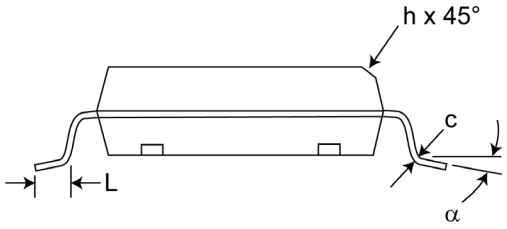


SOIC/SOP SMALL OUTLINE IC PACKAGE

Pkg #	S5	
# Pins	28 (330 mil)	
Symbol	**Min**	**Max**
A	0.079	0.120
A1	0.000	0.008
B	0.012	0.020
C	0.004	0.012
D	0.701	0.728
e	0.050 BSC	
E	0.331	0.346
H	0.457	0.488
L	0.016	0.050
α	0°	8°

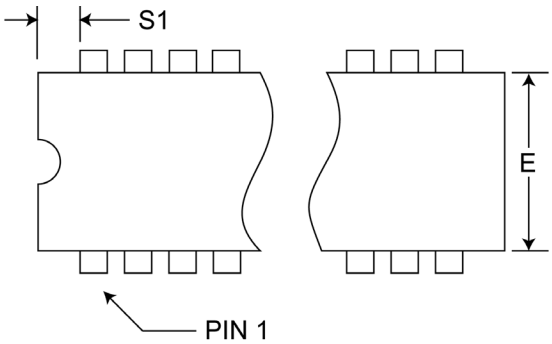


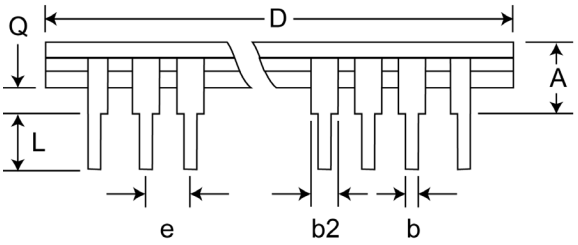


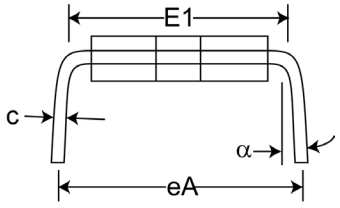


CERAMIC DUAL IN-LINE PACKAGE (600 mil)

Pkg #	C5-1	
# Pins	28 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-







REVISIONS

DOCUMENT NUMBER	SRAM116
DOCUMENT TITLE	P4C164LL - VERY LOW POWER 8Kx8 STATIC CMOS RAM

REV	ISSUE DATE	ORIGINATOR	DESCRIPTION OF CHANGE
OR	Oct-2005	JDB	New Data Sheet
A	Aug-2006	JDB	Added Lead Free Designation
B	Jun-2007	JDB	Corrected SOP package details
C	Mar-2010	JDB	Added Military temperature range
04	Jun-2014	JDB	Updated SOIC/SOP Package dimensions