512K X 16, 1 MEG X 8 CMOS Mask Programmable ROM

FEATURES

- Access time: 200ns max.
- Low Power dissipation:
  - 275mW max. (Active)
  - 5.5mW max. (Standby, TTL input level)
  - 275μW max. (Standby, CMOS input level)
- Fully static operation, no clock required
- Automatic power down ($\overline{CE}$)
- Complete TTL compatibility
- EPROMs accepted as program data input
- Organization (selectable by $\overline{BYTE}$ pin):
  - 524,288 words x 16 bits
  - 1,048,576 words x 8 bits
- 42 pin DIP package
- 64 pin Quad Flat package

DESCRIPTION

The MOSEL MS318003 is a CMOS SI-gate mask-programmable static read only memory organized as 524,288 words by 16 bits, or 1,048,576 words by 8 bits.

The MS318003 has TTL compatible I/O three state output level with full-static operation (i.e. no need of clock signal) and single +5V power supply. Also, the MS318003 is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

Memory output organization of MS318003 is selectable between 16 bits and 8 bits. (ex. The system using 8 bit CPU and 16 bit CPU can use common data from ROM.)

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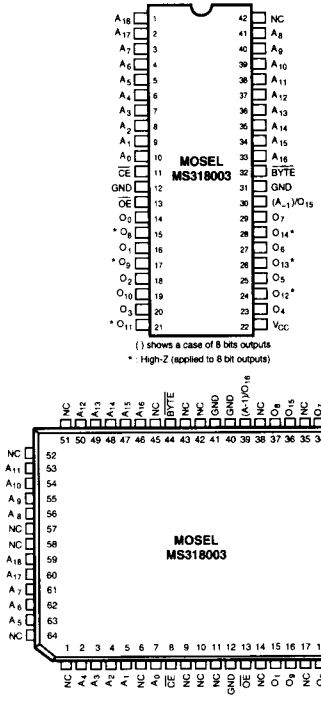
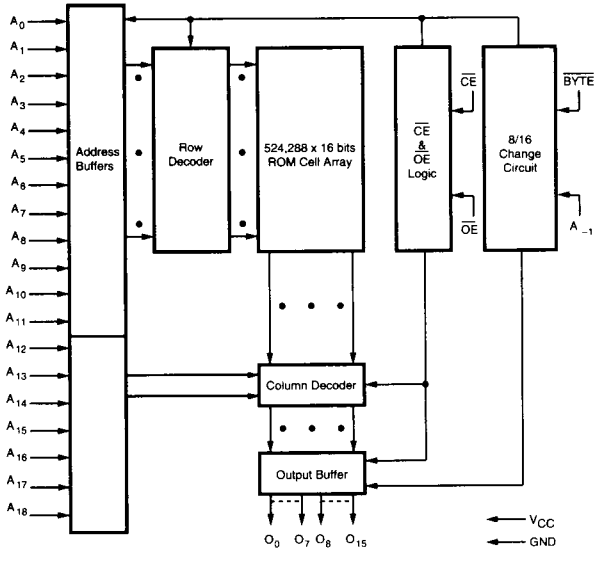
PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTIONS

SYMBOL	FUNCTION
A_0 - A_{18}	Address Input
O_0 - O_{15}	Data Output
GND	Ground
V_{CC}	Power Supply
NC	No Connection
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{BYTE}$	Selects 16 or 8 bit Data Out
A_{-1}	Address Input (8 bit Data select out only)

ABSOLUTE MAXIMUM RATINGS(1)

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−45°C to +125°C
Supply Voltage to Ground Potential	−0.3V to +7.0V
Applied Output Voltage	−0.5V to V_{CC}+0.5V
Applied Input Voltage	−0.5V to V_{CC}+0.5V

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	Vcc
Commercial	0°C to + 70°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS (over the commercial operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS318003 MIN.		MAX.	UNITS
V_{IL}	Input Low Voltage		−0.3	-	0.8	V
V_{IH}	Input High Voltage		2.2		V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{IN}=0V to V_{CC}	−10	-	10	µA
I_{OL}	Output Leakage Current	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IH}	−10	-	10	µA
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−400µA	2.4	-	-	V
I_{CC}	Operating Power Supply Current (1)	$\overline{CE}$=V_{IL}, Min Cycle	-	-	50	mA
I_{CCSB}	Standby Power Supply Current	$\overline{CE}$=V_{IH}	-	-	1	mA
I_{CCSB1}	Super Standby Power Supply Current	$\overline{CE}$=V_{IH}=V_{CC}, V_{IN}=GND or V_{CC}	-	-	50	µA

1. Measured with device selected and outputs unloaded.

CAPACITANCE (Ta=25°C, f=1.0MHz)(1)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CI	Input Capacitance	$V_{IN/OUT}$= 0V	10	pF
CO	Output Capacitance	$V_{IN/OUT}$ = 0V	15	pF

1. This parameter is guaranteed but not 100% tested.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUT	POWER DISSIPATION MODE
H	X	Not Selected	High-Z	Standby
L	H	Not Selected	High-Z	Active
L	L	Selected	D_{OUT}	Active

OUTPUT SELECTION MODE

A_{-1}	$\overline{BYTE}$	O_0 to O_7	O_8 to O_{14}	O_{15}
X	H	D_0 to D_7	D_8 to D_{14}	D_{15}
L	L	D_0 to D_8	High-Z	A_{-1}
H	L	D_8 to D_{15}	High-Z	A_{-1}

AC TEST CONDITIONS

Input Pulse Levels	0.6 to 2.4V
Input Rise and Fall Times	t_R = 5 ns
Timing Measurement Level	V_{IL} = 0.8V V_{IH} = 2.2V
Reference	V_{OL} = 0.8V V_{OH} = 2.2V
Output Load	1 TTL Gate and 100pF

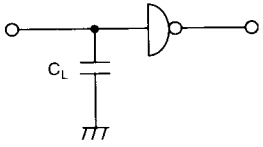


Figure 1. Output Load Circuit

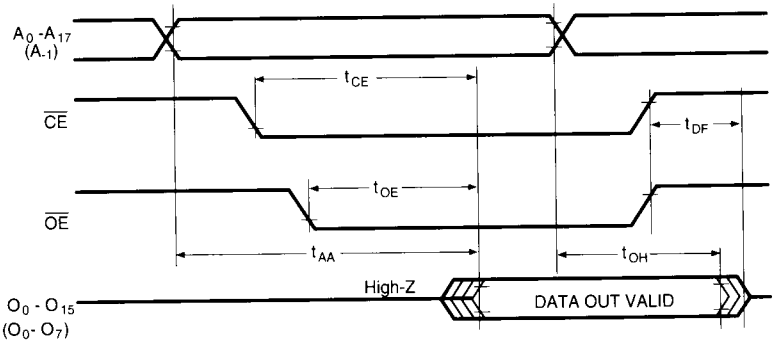
AC ELECTRICAL CHARACTERISTICS (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITION	MS318003-20 MIN.	MAX.	UNIT
t_{AA}	Chip Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	-	200	ns
t_{CE}	Chip Enable Access Time	$\overline{OE}$ = V_{IL}	-	200	ns
t_{OE}	Output Enable Access Time	Note 1	-	80	ns
t_{DF}	Output Disable	Note 2	-	60	ns
t_{OH}	Output Hold After Address Change	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	-	ns

Note 1: Maximum $\overline{OE}$ delay which does not affect t_{AA} is t_{AA}–t_{OE}

Note 2: t_{DF} is specified by either of $\overline{CE}$ or $\overline{OE}$ changing to HIGH earlier.

TIMING DIAGRAMS



( ) shows a case of 8 bit outputs

ORDERING INFORMATION

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
200	MS318003-20PC	P42-1	0°C to + 70°C
200	MS318003-20QC	Q64-1	0°C to +70°C