EPSON

SPC8110F

Local Bus LCD/CRT VGA Controller

■ DESCRIPTION

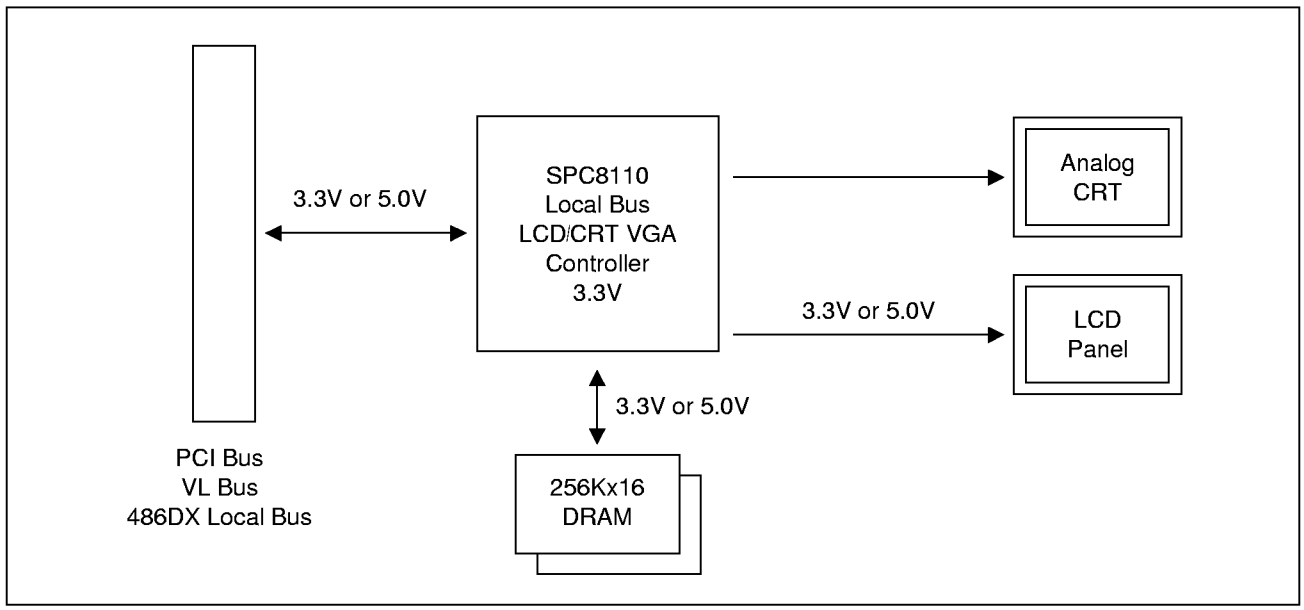
The SPC8110F0A is a single chip multi-function Low Voltage LCDÅïCRT VGA Controller with an built-in RAMDAC and a Liquid Crystal Display interface. With a built-in Hardware Cursor, a Bit Block Transfer Engine, and a CPU Local Bus Interface, the SPC8110F0A accelerates the display of Graphical User Interface software on Analog CRT Monitors and Single or Dual Panel Monochrome or Color LCD Displays.

Optimized for cost and power savings, the SPC8110F0A mixes 3.3V 0.72µm standard cell and gate array technology to achieve high density RAM, DAC, PLL, and digital logic integration. Power consumption in 8-bit monochrome LCD modes is estimated to be 470mW peak during extensive 32-bit 33MHz Local Bus BitBlt operations, 170mW in normal operation and 0.5mW in standby with self-refresh DRAM.

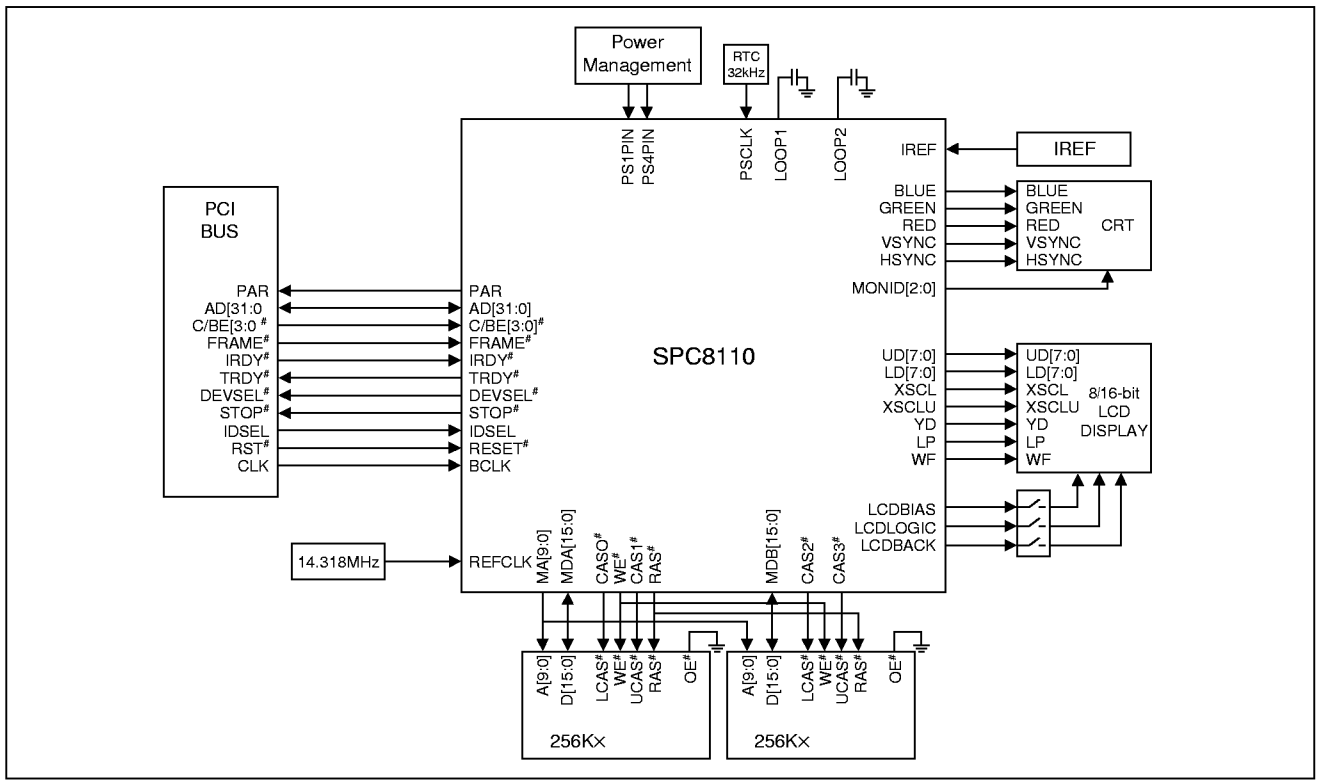
■ FEATURES

- Hardware VGA Compatible
- 32-bit PCI or VL-Bus™ Interface
- 1024KB display memory in two 256Kx16 self-refresh DRAM (asymmetrical or symmetrical)
- Hardware Bit Block Transfer Engine
- Hardware 64x64 pixel 2-bit Cursor
- Hardware Color Expansion
- 8 stage 32-bit Display Pipeline
- Linear Mode Addressing
- Internal PLL and Clock Generation
- Internal 256x18-bit RAMDAC
- Direct Analog CRT drive
- Support for resolutions up to 1024 x 768
- Support for STN, TFT panel and CRT
- 16, 32 & 64 LCD Gray Shades by FRM and Dithering
- Up to 4096 or 256K LCD Colors by FRM and Dithering
- Vertical Centering and Expansion
- Programmable Gray-scale Weighting and Contrast
- LCD Panel Power Sequencing
- Simultaneous LCD and Analog CRT display
- Software Video BIOS, Drivers, and Utilities support
- Extensive Hardware and Software activated Power Save Modes and Status Signals
- Package: QFP8-208pin (plastic) <SPC8110F0A>
  QFP22-208pin (plastic) <SPC8110F1A>
- 3.3 V Core Operating Voltage

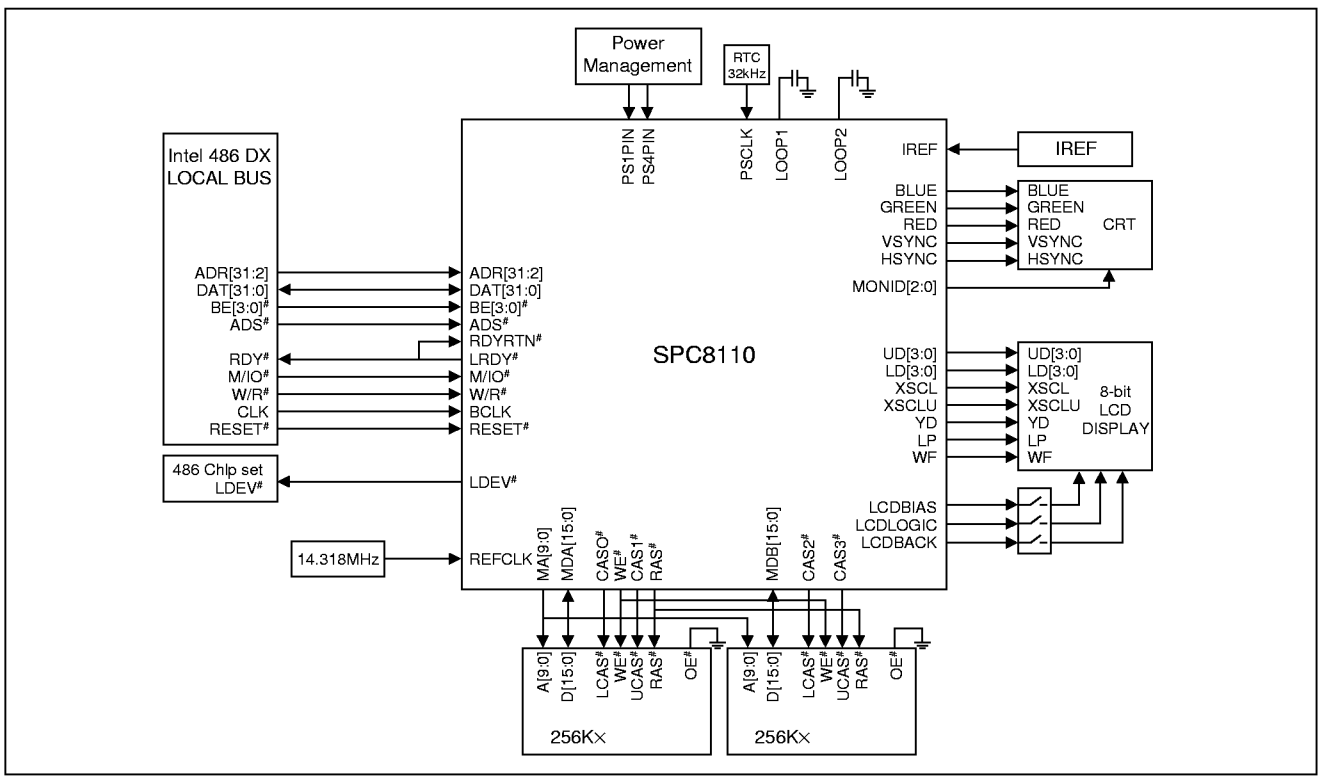
■ BLOCK DIAGRAM



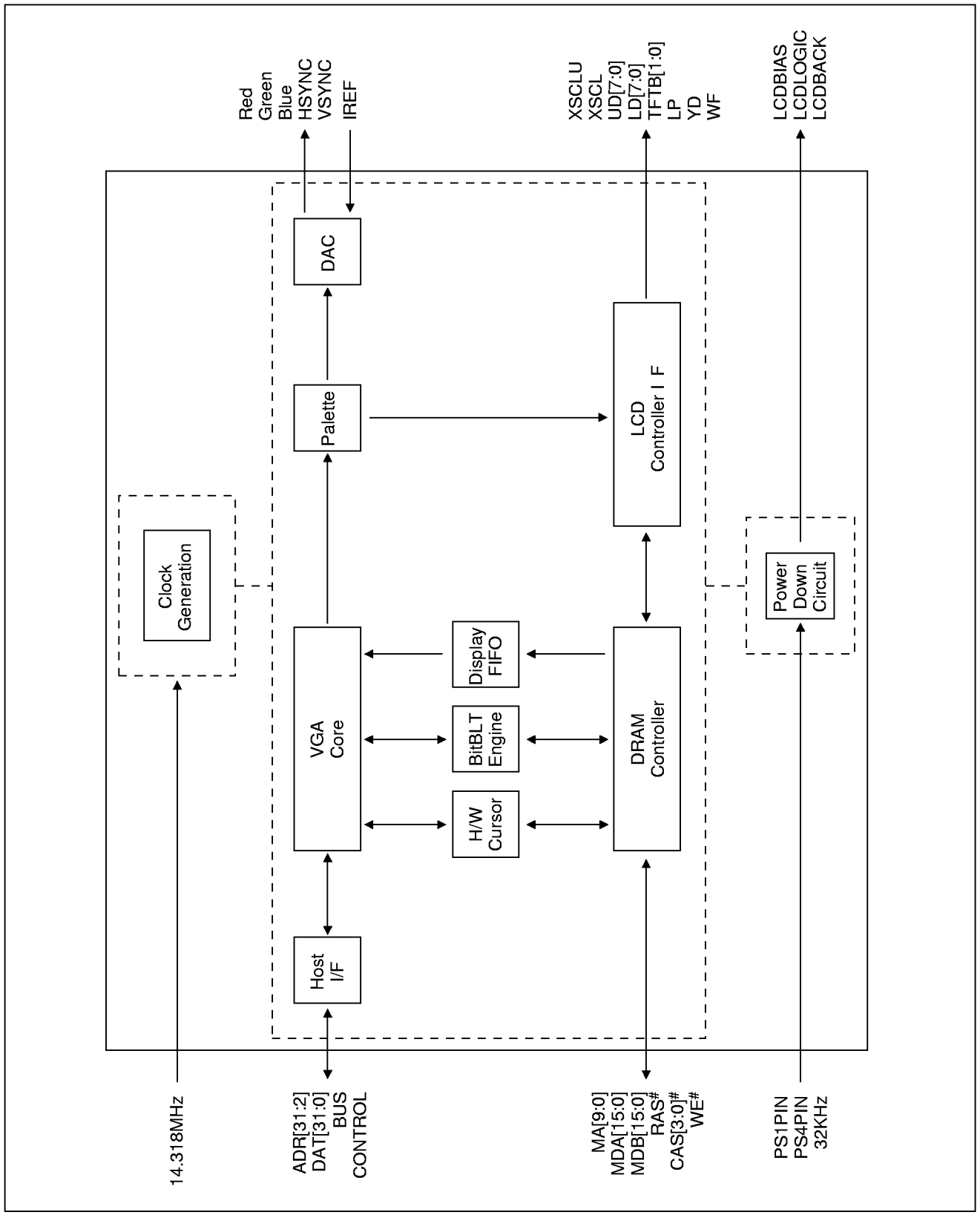
■ PCI BUS SYSTEM BLOCK DIAGRAM



■ 486DX-33 LOCAL BUS SYSTEM BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DIAGRAM



■ FUNCTIONAL BLOCK DESCRIPTION

● Host Interface

The Host interface can be programmed to interface to any of the following three standards: 486DX local bus interface, VL-Bus interface, and PCI interface, It has a one-stage buffer for zero wait-state write operation.

● Clock Generator

The clock generator contains two PLL's that are separately programmed to produce the memory and pixel clocks from a single clock source. The reference clock is usually the 14.318MHz bus clock.

● VGA Core

The VGA Core contains the Sequencer, CRTC Controller, Graphics Controller, Attribute Controller, and the rest of the standard VGA circuitry.

● Hardware Cursor

The Hardware Cursor block generates a 64×64×2-bit hardware cursor or sprite that can be overlaid on the displayed image.

● BitBlt Engine

The Bit Block Transfer Engine performs read, write, and move blts, solid fills, destination inversions, and pattern fills. It performs all data alignment and masking at the blt boundary. It also performs text expansion to accelerate the writing of monochrome images. It operates in both 4-bit planar mode and 8-bit linear (packed-pixel) mode.

● Display FIFO

This is an 8 stage by 16-bit FIFO that is used to buffer the video data from display memory.

● VGA Palette

This block implements the standard 256×18VGA lookup table.

● DAC

This block functions as a triple 6-bit 65MHz DAC to drive the RGB outputs connected to the analog monitor.

● LCD Interface

This block contains frame rate modulation and dithering circuitry for a maximum of 64 shades of gray in monochrome single and dual panel modes. In color LCD mode, it uses frame rate modulation to generate 4K colors, and additional dithering techniques for a full 256K colors.

● Power Save Logic

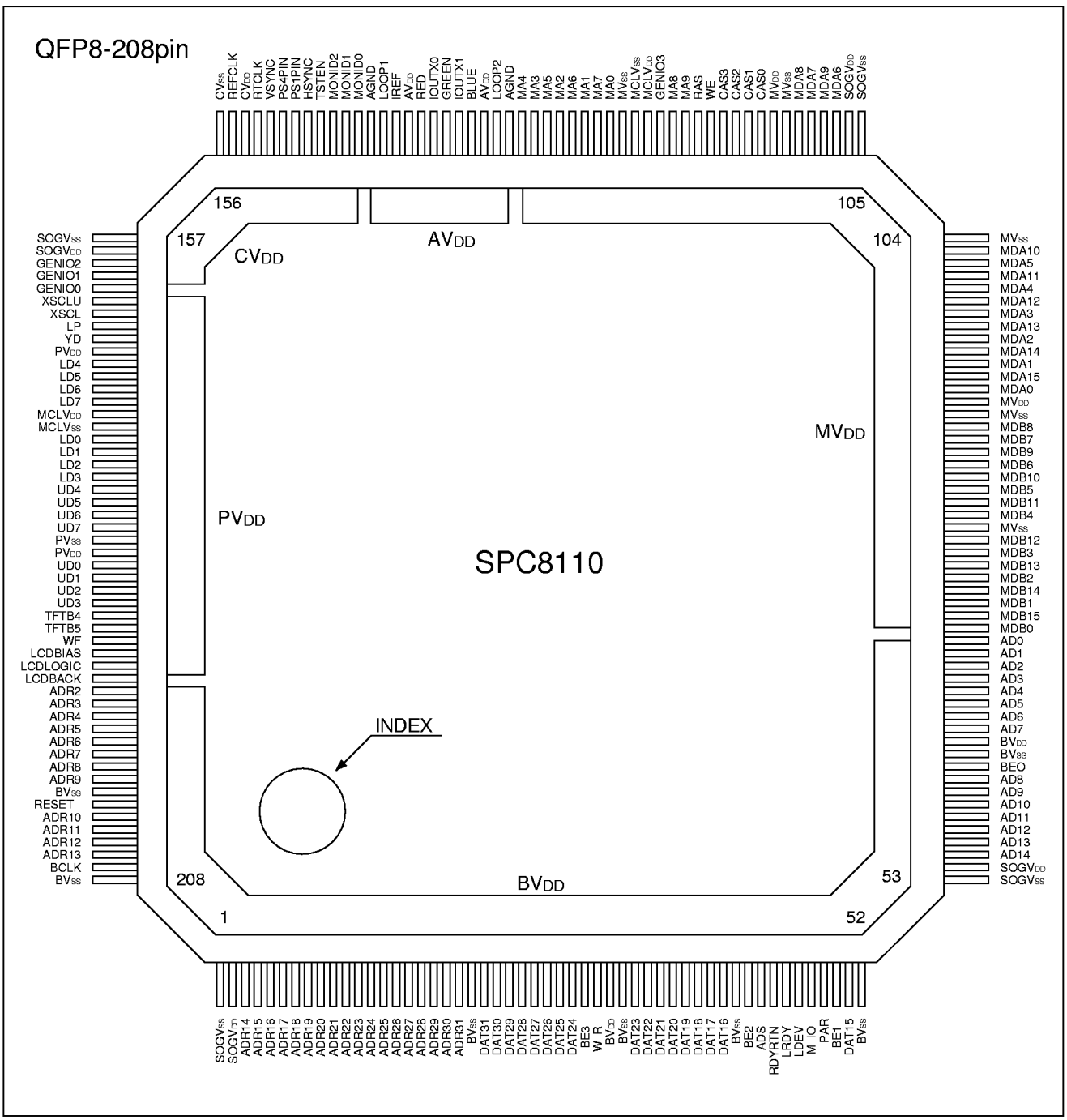
This block implements all the power down features of the chip.

■ SPC8110 VIDEO MODES (Standard Display Modes)

Mode Number (HEX)	Horizontal Pixels Addressable (characters)	Vertical Pixels Addressable (rows)	Horizontal Pixels Displayed (CRT)	Vertical Pixels Displayed	Monochrome LCD Gray Shades	CRT Gray Shades	CRT Frame Rate (Hz)
0	(40)	(25)	320	200	16	16	70
0+	(40)	(25)	320	350	16	16	70
0++	(40)	(25)	320	400	16	16	70
1	(40)	(25)	320	200	16	16	70
1+	(40)	(25)	320	350	16	16	70
1++	(40)	(25)	320	400	16	16	70
2	(80)	(25)	640	200	16	16	70
2+	80	(25)	640	350	16	16	70
2++	(80)	(25)	640	400	16	16	70
3	(80)	(25)	640	200	16	16	70
3+	(80)	(25)	640	350	16	16	70
3++	(80)	(25)	640	400	16	16	70
4	320	200	320	200	4	4	70
5	320	200	320	200	4	4	70
6	640	200	640	200	2	2	70
7	(80)	(25)	640	350	2	2	70
7+	720	400	640	400	2	2	70
0D	320	200	320	200	16	16	70
0E	640	200	640	200	16	16	70
0F	640	350	640	350	2	2	70
10	640	350	640	350	16	16	70
11	640	480	640	480	2	2	60
12	640	480	640	480	16	16	60
13	320	200	320	200	64	256	70
6A	800	600	800	600	16	16	72
100	640	400	640	400	64	256	72
101	640	480	640	480	64	256	72
102	800	600	800	600	n/a	16	72
103	800	600	800	600	n/a	256	72
104	1024	768	1024	768	—	16	60
105	1024	768	1024	768	—	256	60*
108	(80)	(60)	640	480	16	16	60
109	(132)	(25)	1056	350	16	16	70
10A	(132)	(43)	1056	350	n/a	16	70
10B	(132)	(50)	1056	400	n/a	16	70
10C	(132)	(60)	1056	480	n/a	16	70

*: Only available with 1024KB RAM

■ PIN CONFIGURATION



Note: Pin names correspond to the default VL-Bus™ configuration.
Pin placement subject to change.

■ PIN DESCRIPTION

● Key

A = Analog
I = Input
O = Output
I/O = Bidirectional
P = Power

● CPU-Intel486/VL-Bus Interface

Pin Name	I/O	Pin No.	Function
ADR[31:2]	I	20-3, 206-203, 200-193	VL-Bus Address inputs.
DAT[31:0]	I/O	22-29, 34-41, 51, 55-61, 65-72	VL-Bus Data inputs. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times.
BE[3:0]#	I	30, 43, 50, 62	VL-Bus byte enables.
W/R#	I	31	VL-Bus Write or Read Status.
M/IO#	I	48	VL-Bus Memory or I O Status.
ADS#	I	44	VL-Bus Address Date Strobe.
RDYRTN#	I	45	VL-Bus Ready Return.
BCLK	I	207	VL-Bus Local CPU Clock.
LRDY#	O	46	VL-Bus Local Ready.
LDEV#	O	47	VL-Bus Local Device.
RESET#	I	202	CPU Reset. The active low reset signal from the CPU clears all internal registers and forces all signals to their inactive state. On the rising edge of the RESET# the MDA[0..15] bus is latched in for configuration.

● PCI Bus Interface

Pin Name	I/O	Pin No.	Function
AD[31:0]	I/O	22-29, 34-41, 51, 55-61 65-72	PCI multiplexed Address and Data Bus. These lines are driven by the chip only during read cycles, and are in a hi-Z state at all other times.
C/BE[3:0]#	I	30, 43, 50, 62	PCI Bus Command and Byte Enables.
IDSEL	I	31	PCI Bus Initialization Device Select.
STOP#	I/O	48	PCI Bus Stop.
FRAME#	I	44	PCI Bus Cycle Frame.
IRDY#	I	45	PCI Bus Initiator Ready.
PAR	O	49	Parity. This line is driven by the chip only during read cycles, and is in a hi-Z state at all other times.
BCLK	I	207	PCI Bus Clock.
TRDY#	I/O	46	PCI Bus Target Ready.
DEVSEL#	O	47	PCI Bus Device Select.

Pin Name	I/O	Pin No.	Function
RST#	I	202	PCI Bus Reset. The active low reset signal from the CPU clears all internal registers and forces all signals to their inactive state.

● VL-Bus/PCI Bus Pin Mapping

VL-Bus Name	PCI Name	Pin No.
RESET#	RST#	202
RDYRTN#	IRDY#	45
ADR[31:2]	--	20-3, 206-203, 200-193
W/R#	IDSEL	31
LDEV#	DEVSEL#	47
DAT[31:0]	AD[31:0]	22-29, 34-41, 51, 55-61, 65-72

VL-Bus Name	PCI Name	Pin No.
BCLK	BCLK	207
--	PAR	49
M/IO#	STOP#	48
ADS#	FRAME#	44
LRDY#	TRDY#	46
BE[3:0]#	C/BE[3:0]#	30, 43, 50, 62

● Video Memory Interface

Pin Name	I/O	Pin No.	Function
MA[15:0]	O	119, 120, 126, 128, 130, 132, 131, 129, 127, 125	Multiplexed row/column address bits for video display memory.
MDA[15:0]	I/O	93, 95, 97, 99, 101, 103, 108, 110, 109, 107, 102, 100, 98, 96, 94, 92	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET# is low, or when the Sequencer is in a reset state. These pins are also used as configuration inputs.
MDB[15:0]	I/O	74, 76, 78, 80, 83, 85, 87, 89, 88, 86, 84, 82, 79, 77, 75, 73	Data bits for video display memory. The output drivers of these pins are placed into a high-impedance state when RESET# is low, or when the Sequencer is in a reset state.
RAS#	O	118	DRAM Row Address Strobe
CAS[0]# (CAS#)	O	113	DRAM Column Address Strobe for one of four bytes, or Column Address Strobe for all four bytes, as configured by Aux(index 03h) bit 7
CAS[3:1]# (WE[3:1]#)	O	116-114	DRAM Column Address Strobe for three of four bytes, or Write Enable Strobe for three of four bytes, as configured by Aux 0(index 03h) bit 7
WE# (WE[0]#)	O	117	DRAM Write Enable Strobe for all four bytes or Write Enable Strobe for one of four bytes, as configured by Aux(index 03h) bit 7

● Clock Inputs

Pin Name	I/O	Pin No.	Function
REFCLK	I	155	This pin is the reference clock used by the internal PLLs to generate all the necessary clocks. This must be stable during full operation. REFCLK may shut down only after the chip is totally powered down. Input frequency is typically 14.318MHz.
RTCLK	I	153	Real Time Clock. This input must be used to provide a low frequency clock for generating refresh. This clock must be approximately 32KHz and 50% duty cycle. (See Clock Input Requirements on page 39.)

● CRT Interface

Pin Name	I/O	Pin No.	Function
RED, GREEN, BLUE	AO	140, 138, 136	Analog outputs from the Video DAC. Internal comparator for monitor sense available on the GREEN.
HSYNC	O	149	Horizontal Sync. This output is driven to indicate the horizontal retrace period.
VSYNC	O	152	Vertical Sync. This output is driven to indicate the vertical retrace period.
IREF	AI	142	Current reference input for the Video DAC.
MONID[2:0]	I	147-145	Monitor ID bits. Connected to the CRT to identify the monitor type.

● Miscellaneous

Pin Name	I/O	Pin No.	Function
TSTEN	I	148	When high this pin sets the SPC8110 into either boundary pin SCAN or pin output drive test, depending on the state of PSIPIN.
GENIO[3:0]	I/O	121, 159, 161, 160	General purpose I/O pins. Output state of these pins is programmable to control external devices. See Auxiliary Register 34h. GENIO[1] purposely omitted
LOOP1	I	143	Connects to Loop Filter Capacitor for PLL1
LOOP2	I	134	Connects to Loop Filter Capacitor for PLL2
IOUTX[1:0]	O	137, 139	Balanced current output for the DAC.

● Power Save Mode Control

Pin Name	I/O	Pin No.	Function
PS1PIN	I	150	Pin used to initiate a power save mode 1. The polarity of this pin is programmable and has a default polarity of active low.
PS4PIN	I	151	Pin used to initiate a power save mode 4. The polarity of this pin is programmable and has a default polarity of active low.

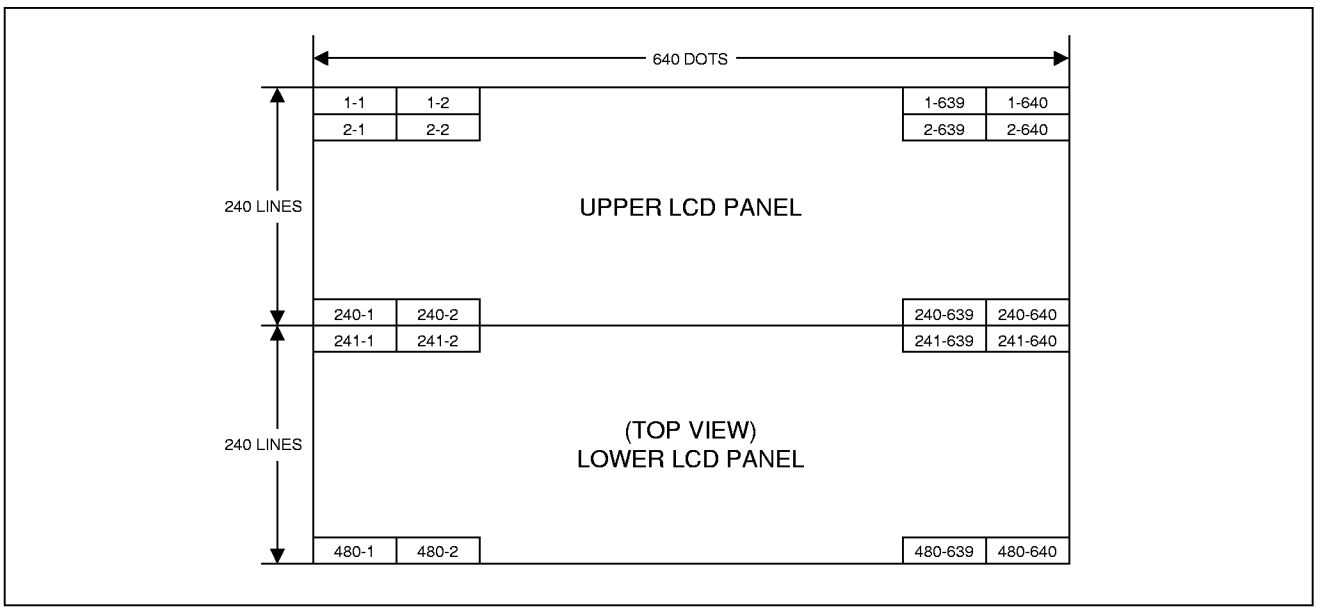
● Power Supply

Pin Name	I/O	Pin No.	Function
SOGVDD	P	158, 106, 54, 2	VDD supply for 3.3V core logic.
MVDD	P	112, 91	VDD supply for memory pins.
BVDD	P	32, 64	VDD supply for bus interface pins.
CVDD	P	154	VDD supply for control interface pins.
PVDD	P	166, 182	VDD supply for panel interface pins.
AVDD	P	135, 141	Analog power supply.
SOGVSS	P	157, 105, 53, 1	VSS supply for 3.3V core logic.
MVSS	P	111, 124, 104,90, 81	VSS supply for memory pins.
BVSS	P	201, 208, 21, 42, 52, 33, 63	VSS supply for bus interface pins.
CVSS	P	156	VSS supply for control interface pins.
PVSS	P	181	VSS supply for panel interface pins.
AGND	P	133, 144	Analog Ground.
MCLVDD	P	122, 171	VDD supply for MCL logic.
MCLVSS	P	123, 172	VSS supply for MCL logic.

● LCD Panel Interface

Pin Name	I/O	Pin No.	Function
YD	O	165	Vertical Scanning Start Pulse output. A logic 1 on this signal, sampled by the LCD module on the falling edge of LP, is used by the panel row drivers (Y drivers) to indicate the start of the vertical frame.
LP	O	164	Latch Pulse Output. The falling edge of this signal is used to latch a row of display date in the LCD module ⑦s column driver shift registers and to turn on the row driver(Y driver) for that line.
XSCL	O	163	Shift Clock for LCD data. Display data is clocked out of the chip on the rising edge of this signal, to be shifted into the LCD panel module column drivers(X drivers) on each falling edge.
XSCLU	O	162	Second Shift Clock for some color LCD displays.
UD[7:0] LD[7:0]	I/O	180-177, 186-183, 170-167, 176-173	Panel display data bus. The data format depends on the specific panel connected. For 8-bit panels, the upper nibble of UD[7:4] and LD[7:4] are tri-stated.
TFTB[5:4]	O	188-187	TFT display data bus for the two LSBs of the color blue. For non-TFT panels, these tow pins are tri-stated.
LCDBIAS	O	190	LCD power control for the LCD bias circuitry. Active polarity is defined by the state of MDA[3] on the rising edge of RESET#.
LCDBACK	O	192	LCD power control for the LCD back light. Active polarity is defined by the state of MDA[1] on the rising edge of RESET#.
LCDLOGIC	O	191	LCD power control for the LCD logic circuitry. Active polarity is defined by the state of MDA[2] on the rising edge of RESET#.
WF	O	189	LCD Backplane Bias signal. Output toggling frequency is programmable in an auxiliary register. For TFT panels, this pin outputs the display enable signals.

■ LCD PANEL PIXELS



■ D.C. CHARACTERISTICS

● Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	V_{SS} – 0.3 to 7.0	V
V_{IN}	Input Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
V_{OUT}	Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
T_{STG}	Storage Temperature	– 65 to 150	°C
T_{SOL}	Solder Temperature/Time	260 for 10 sec. max at lead	°C

● Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
HV$_{DD}$	Supply Voltage	V_{SS} = 0V	4.5	5.0	5.5	V
LV$_{DD}$	Supply Voltage	V_{SS} = 0V	3.0	3.3	3.6	V
V_{IN}	Input Voltage	V_{SS}	V_{SS}	--	V_{DD}	V
T_{OPR}	Operating Temperature		0	25	70	°C
I_{OPR}	Average Power Consumption			381.7		mW

● Input Specifications

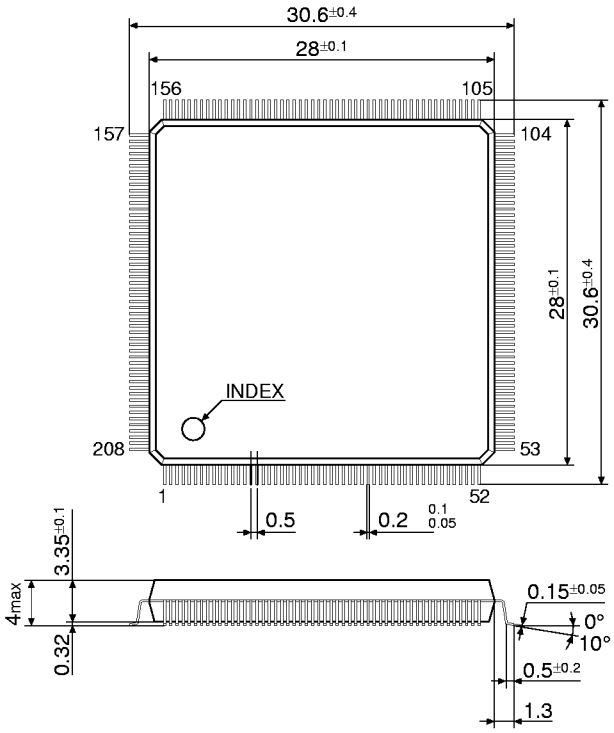
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage	V_{DD} = 4.5V / 3.0V	--	--	0.8	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.5V / 3.6V	2.0	--	--	V
HR$_{PD}$	Pull Down Resistance	V_{DD} = 5V	25	50	100	kΩ
LR$_{PD}$	Pull Down Resistance	V_{DD} = 3.3V	45	90	180	kΩ
V_{T+}	Positive-going Threshold CMOS Schmitt Trigger	V_{DD} = 5 / 3.3V			2.4	V
V_{T-}	Negative-going Threshold CMOS Schmitt Trigger	V_{DD} = 5 / 3.3V	0.6			V
HV$_{H}$	Hysteresis Voltage CMOS Schmitt Trigger	V_{DD} = 5 / 3.3V	0.1			V
C_{IN}	Clock Pin Capacitance	BCLK, RESET#, REFCLK, MONID[2:0], TSTEN, PS1PIN, PS4PIN, RTCLK		4		pF
C_{BID}	Input Pin Capacitance	all pins not listed in C_{IN}		10		pF
I_{L}	Input Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	µA

● Output Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Level Output Voltage Type 2 Type 3 Type 4	V_{DD} = 5 / 3.3V I_{OL} = 6mA I_{OL} = 12mA I_{OL} = 24mA			V_{SS} + 0.3	V
V_{OH}	High Level Output Voltage Type 2 Type 3 Type 4	V_{DD} = 5 / 3.3V I_{OL} = –2mA I_{OL} = –4mA I_{OL} = –8mA	V_{DD} – 0.3			V
I_{OZ}	Off-state Leakage Current	V_{DD} = MAX V_{IH} = V_{DD} V_{IL} = V_{SS}	–1		1	μA

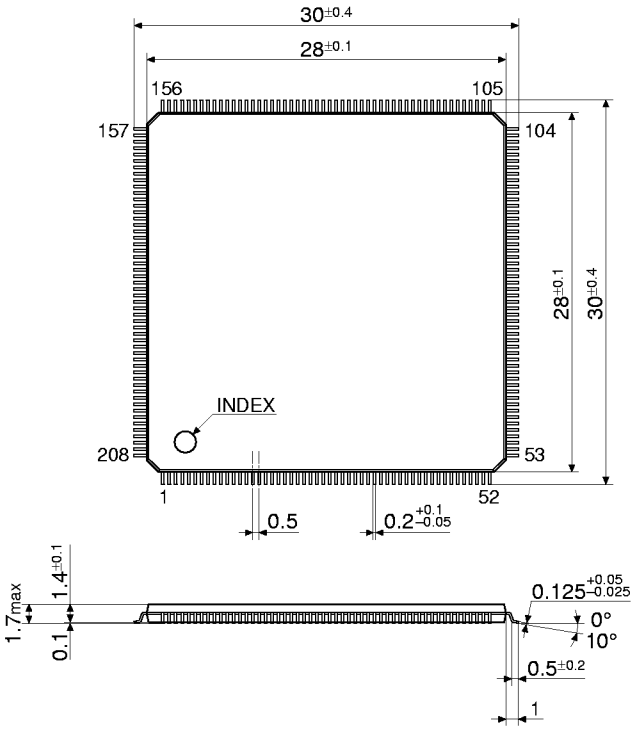
■ PACKAGE DIMENSIONS

Plastic QFP8-208 pin S1



Unit : mm

Plastic QFP22-208 pin



Unit : mm