STEL-1177

Data Sheet

STEL-1177

32-Bit Resolution CMOS Phase and Frequency Modulated Numerically Controlled Oscillator

STANFORD TELECOM®

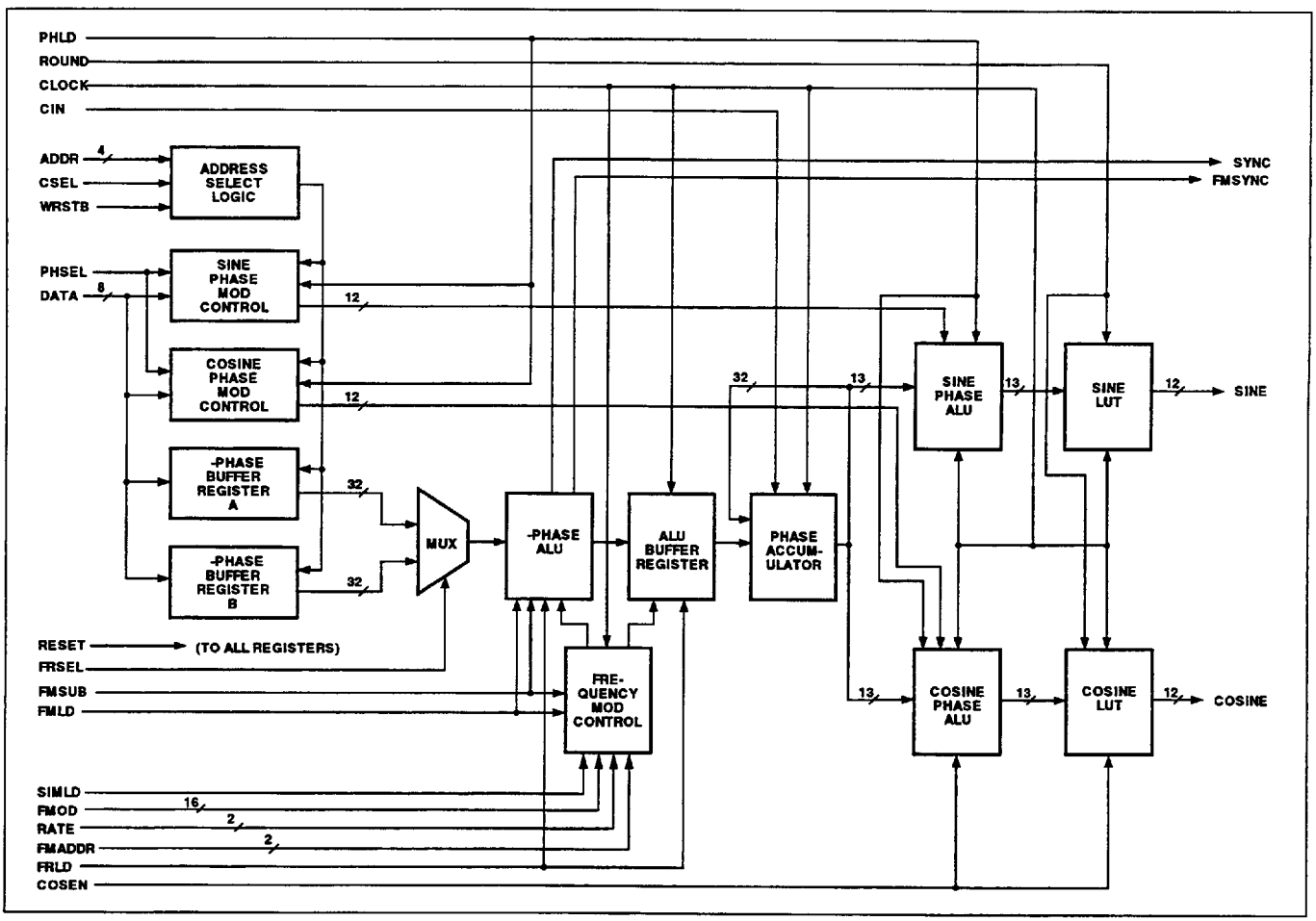
FEATURES

- **HIGH CLOCK FREQUENCY**
  - **60 MHz MAXIMUM OVER COMMERCIAL TEMPERATURE RANGE**
  - **40 MHz MAXIMUM OVER FULL MILITARY TEMPERATURE RANGE**
- **HIGH FREQUENCY RESOLUTION**
  - **32-BITS, 14 milli-Hz @ 60 MHz**
- **WIDE OUTPUT BANDWIDTH**
  - **0 TO 25 MHz @ 60 MHz CLOCK**
- **PRECISION PHASE MODULATION**
  - **12-BITS, 0.09° RESOLUTION, CAN BE USED FOR LINEAR PM OR PULSE-SHAPED PSK**
- **PRECISION FREQUENCY MODULATION**
  - **16 BITS RESOLUTION, CAN BE USED FOR LINEAR FM OR PULSE-SHAPED FSK**
- **QUADRATURE SIGNAL GENERATION**
  - **12-BIT OUTPUTS WITH INDEPENDENT PHASE MODULATION PER CHANNEL**
- **HIGH SPECTRAL PURITY**
  - **ALL SPURS < -75 dBc**
- **MICROPROCESSOR COMPATIBLE INPUTS**
- **LOW POWER DISSIPATION**
  - **COSINE CHANNEL CAN BE DISABLED TO REDUCE POWER**
- **84 PIN PLCC OR CLDCC PACKAGES AND 84 PIN CERAMIC PGA PACKAGE AVAILABLE**

TYPICAL APPLICATIONS

- **FREQUENCY SYNTHESIZERS**
- **FSK AND PSK MODULATORS**
- **DIGITAL SIGNAL PROCESSORS**
- **HIGH SPEED HOPPED FREQUENCY SOURCES**

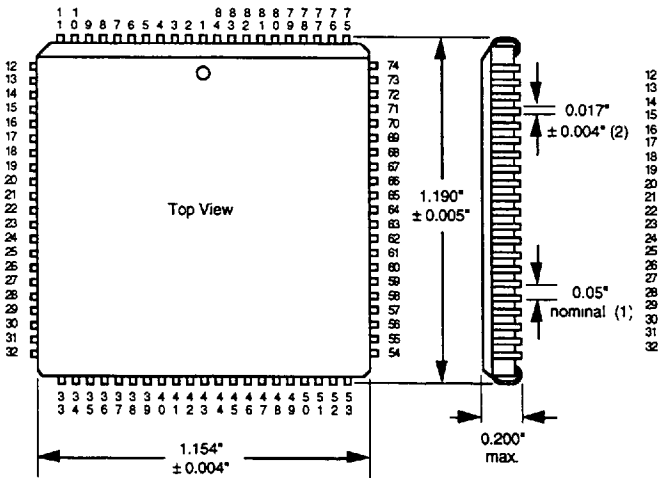
BLOCK DIAGRAM



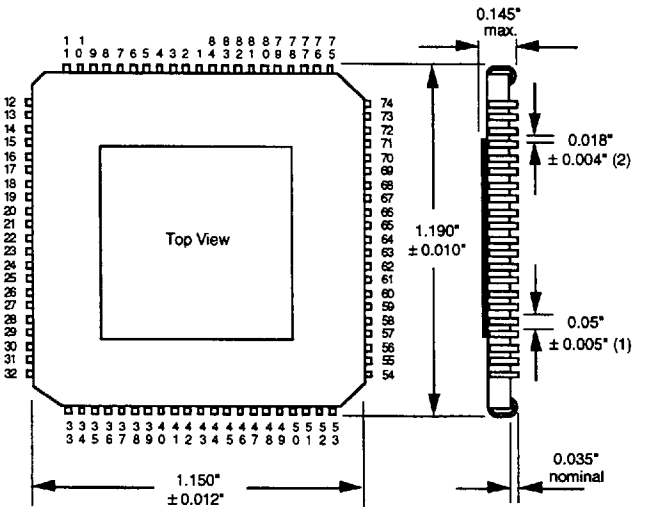
PIN CONFIGURATION

1. Plastic (PLCC) (/CM) or Ceramic (CLDCC) (/CC and /MC) Leaded Chip Carrier

Package:
84 pin PLCC
Thermal coefficient, qja = 30°/W

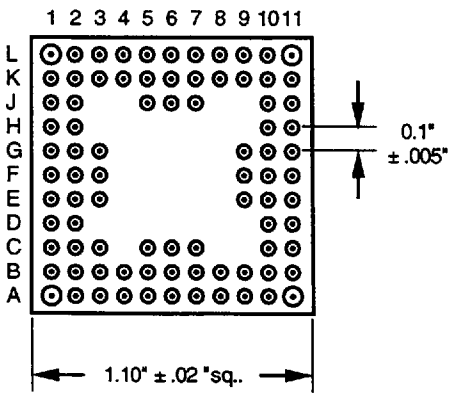


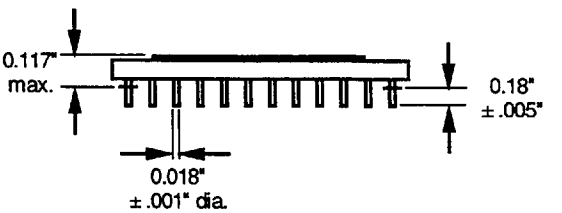
Package:
84 pin CLDCC
Thermal coefficient, qja = 34°/W



Notes:
1. Dimensions shown are for plastic package. Dimensions for ceramic package are similar.
2. Tolerances on pin spacing are not cumulative.

2. Ceramic Pin Grid Array (CPGA) (/CF and /MF)





Notes: 1. Tolerances on pin spacings are not cumulative.
2. Corner pins have integral standoffs which raise the package 0.07" (nominal) above the mounting surface.
3. Orientation determined by extra pin at location C3.
4. Thermal coefficient, θ_{ja} = 28°C/watt

PIN CONNECTIONS

1	(C6)	V_{SS}	22	(F3)	V_{SS}	43	(J6)	V_{SS}	64	(F9)	V_{SS}
2	(A6)	$FMOD_7$	23	(G3)	CLOCK	44	(J7)	COS_4	65	(F11)	$SINE_{10}$
3	(A5)	$FMOD_8$	24	(G1)	SIMLD	45	(L7)	COS_5	66	(E11)	$SINE_{11}$
4	(B5)	$FMOD_9$	25	(G2)	$ADDR_3$	46	(K7)	COS_6	67	(E10)	$RATE_0$
5	(C5)	$FMOD_{10}$	26	(F1)	$ADDR_2$	47	(L6)	COS_7	68	(E9)	$RATE_1$
6	(A4)	$FMOD_{11}$	27	(H1)	$ADDR_1$	48	(L8)	COS_8	69	(D11)	ROUND
7	(B4)	$FMOD_{12}$	28	(H2)	$ADDR_0$	49	(K8)	COS_9	70	(D10)	COSEN
8	(A3)	$FMOD_{13}$	29	(J1)	CSEL	50	(L9)	COS_{10}	71	(C11)	V_{SS}
9	(A2)	$FMOD_{14}$	30	(K1)	FRSEL	51	(L10)	COS_{11}	72	(B11)	FMLD
10	(B3)	$FMOD_{15}$	31	(J2)	V_{SS}	52	(K9)	V_{SS}	73	(C10)	FMSYNC
11	(A1)	V_{DD}	32	(L1)	V_{DD}	53	(L11)	V_{DD}	74	(A11)	V_{DD}
12	(B2)	$DATA_7$	33	(K2)	PHLD	54	(K10)	$SINE_{0(LSB)}$	75	(B10)	FMSUB
13	(C2)	$DATA_6$	34	(K3)	PHSEL	55	(J10)	$SINE_1$	76	(B9)	$FMADDR_0$
14	(B1)	$DATA_5$	35	(L2)	CIN	56	(K11)	$SINE_2$	77	(A10)	$FMADDR_1$
15	(C1)	$DATA_4$	36	(L3)	FRLD	57	(J11)	$SINE_3$	78	(A9)	$FMOD_0$
16	(D2)	$DATA_3$	37	(K4)	SYNC	58	(H10)	$SINE_4$	79	(B8)	$FMOD_1$
17	(D1)	$DATA_2$	38	(L4)	I.C.	59	(H11)	$SINE_5$	80	(A8)	$FMOD_2$
18	(E3)	$DATA_1$	39	(J5)	$COS_{0(LSB)}$	60	(F10)	$SINE_6$	81	(B6)	$FMOD_3$
19	(E2)	$DATA_0$	40	(K5)	COS_1	61	(G10)	$SINE_7$	82	(B7)	$FMOD_4$
20	(E1)	WRSTB	41	(L5)	COS_2	62	(G11)	$SINE_8$	83	(A7)	$FMOD_5$
21	(F2)	RESET	42	(K6)	COS_3	63	(G9)	$SINE_9$	84	(C7	$FMOD_6$

Numeric pin connections are for PLCC and CLDCC packages, alphanumeric connections in parentheses are for PGA package. Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

FUNCTIONAL DESCRIPTION

The STEL-1177 Modulated Numerically Controlled Oscillator (MNCO) uses digital techniques to provide a cost-effective solution for low noise signal sources. The NCO features high frequency resolution with exceptional spectral purity of outputs up to 25 MHz. The STEL-1177 also features both phase and frequency modulation at rates up to 25% of the clock frequency. Separate 12-bit sine and cosine outputs are provided which can be phase modulated independently. The cosine channel can be disabled when not in use, reducing the power consumption by approximately 30%. The device combines low power 1.5μ CMOS technology with a unique architectural design resulting in a power efficient, high-speed sinusoidal waveform generator able to achieve fine tuning resolution and exceptional spectral purity at clock frequencies up to 60 MHz. The NCO is designed to provide a simple interface to an 8-bit microprocessor bus.

The NCO maintains a record of phase which is accurate to 32 bits. At each clock cycle, the number stored in the 32-bit Δ-Phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine and cosine functions. The number in the Δ-Phase register represents the phase change for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{32}}$$

where: f_o is the frequency of the output signal

and: f_c is the clock frequency.

The sine and cosine functions are generated from the 13 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ-Phase Register, which may be programmed by an 8-bit microprocessor, and the frequency modulation value loaded on the **FMOD** bus. The carrier frequency and the frequency modulation can be updated independently or simultaneously, using an internal synchronization circuit which ensures glitch-free updates.

The NCO generates a sampled sine wave where the sampling function is the clock. The practical upper limit of the NCO output frequency is about 40% of the clock frequency due to spurious components that are created by sampling. Those components are at

frequencies greater than half the clock frequency, and become more difficult to remove by filtering as the output frequency approaches half the clock frequency.

The phase noise of the NCO output signal may be determined from the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 19 clock cycles. The dual Δ-Phase registers used in the STEL-1177 allow the frequency and frequency modulation to be updated as rapidly as every fourth clock cycle, i.e. at 25% of the clock frequency. The pipeline delay associated with the phase modulator is only 12 clock cycles, since the phase modulating function is at the output of the accumulator. The phase modulation may also be changed as rapidly as every fourth clock cycle, at 25% of the clock frequency, resulting in a maximum modulation rate of 15 MHz with a clock frequency of 60 MHz. Note that when a phase or frequency change occurs at the output the change is instantaneous, i.e., it occurs in one clock cycle, with complete phase coherence.

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK

This block controls the writing of data into the device via the **$DATA_{7-0}$** inputs. The data is written into the device on the rising edge of the **WRSTB** input, and the register into which the data is written is selected by the **$ADDR_{3-0}$** inputs. The **CSEL** input can be used to selectively enable the writing of data from the bus.

SIN/COS PHASE MODULATION BLOCK

This block includes the Phase Modulation Buffer Registers, and controls the source of the phase modulation (PM) data by means of the **PHSEL** input. When this signal is low, data from the **$DATA_{7-0}$** and **$ADDR_{3-0}$** inputs is written directly into the Phase ALUs after a falling edge on the **PHLD** input. The same PM data will be applied to both the Sine and Cosine Phase ALUs in this mode. When **PHSEL** is high, data is written into the Phase Modulation Buffer Registers from the **$DATA_{7-0}$** bus on the rising edge of the **WRSTB** input. The data will then be transferred into the Sine and Cosine ALUs after the next falling edge of **PHLD**. The sources of the PM data applied to the Sine and Cosine Phase ALUs will be the independent Sine and Cosine Phase Buffer Registers in this mode, so that different phase modulation can be applied to the sine and cosine channels.

Δ-PHASE BUFFER REGISTERS A & B BLOCK

The two Δ-Phase Buffer Registers are used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously as four bytes per 32-bit Δ-Phase word. The data is transferred from these registers into the Δ-Phase ALU after a falling edge on the **FRLD** input.

MUX BLOCK

This block is used to select which Δ-Phase Buffer Register is used as the source of frequency data for the Δ-Phase ALU, by means of the **FRSEL** input.

FREQUENCY MODULATION CONTROL BLOCK

This block controls the writing of the frequency modulation (FM) data on the **$FMOD_{15-0}$** bus into the FM Buffer Register, and the loading of this data into the Δ-Phase ALU. This data is multiplied by a factor of 2^0, 2^4, 2^8, or 2^{12}, according to the state of the **$FMADDR_{1-0}$** inputs, before being loaded into the Δ-Phase ALU. This gives a wide range of values for the maximum deviation and resolution. The writing of the FM data can be either manual or automatic. It is controlled by the **$RATE_{1-0}$** inputs, and the **FMLD** input or the **FMSYNC** output, depending on the mode selected. In addition, this block synchronizes the simultaneous updating of the carrier frequency data and FM data when the **SIMLD** input is high.

Δ-PHASE ALU BLOCK

This block controls the updating of the Δ-Phase word used in the Accumulator. The frequency data from the Mux Block is loaded into this block after a falling edge on the **FRLD** input, and the FM data from the Frequency Modulation Control block is loaded after a falling edge on the **FMLD** input. However, if the **SIMLD** input is high, the **FMLD** input will load both sets of data simultaneously. The FM data is added to or subtracted from the carrier frequency data, the add/subtract operation being selected by the **FMSUB** input. This block also generates the **SYNC** output, which indicates the instant at which any phase or frequency change made at the inputs affects the **$SINE_{11-0}$** and **COS_{11-0}** output signals, and also the **FMSYNC** output, which controls the loading of the FM data on the **$FMOD_{15-0}$** bus in the automatic mode.

ALU BUFFER REGISTER BLOCK

This block stores the output from the Δ-Phase ALU for use in the Phase Accumulator. It also controls the time alignment of this data whenever it is changed, so that glitch-free updating of the accumulator pipeline is achieved.

PHASE ACCUMULATOR BLOCK
This block forms the core of the NCO function. It is a high-speed, pipelined, 32-bit parallel accumulator, generating a new sum in every clock cycle. A carry input (the **CIN** input) allows the resolution of the accumulator to be expanded by means of an auxiliary NCO or phase accumulator. The overflow signal is discarded, since the required output is the modulo(2^{32}) sum only. This represents the modulo(2π) phase angle.

PHASE ALU BLOCKS
The two Phase ALUs perform the addition of the sine and cosine PM data to the Phase Accumulator output in the sine and cosine channels, respectively. The PM data words are both 12 bits wide, and these are added to the 13 most significant bits from the Phase Accumulator to form the modulated phase used to address the lookup tables.

SINE AND COSINE LOOKUP TABLE BLOCKS
These blocks are the sine and cosine memories. The 13 bits from the Phase ALUs are used to address these memories to generate the 12-bit $SINE_{11-0}$ and COS_{11-0} outputs. The Cosine LUT can be disabled when not in use, to conserve power, by means of the **COSEN** input.

INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 20 nsecs, and normal operation will resume after this signal returns high. The data on the $SINE_{11-0}$ and COS_{11-0} buses will then be invalid for 7 clock cycles, and thereafter will remain at the value corresponding to zero phase until new frequency or modulation (either frequency or phase) data is loaded with the **FRLD**, **FMLD**, or **PHLD** inputs after the **RESET** returns high.

CLOCK
All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 60 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 5 nanoseconds.

CSEL
The Chip Select input is used to control the writing of data into the chip. It is active low. When this input is high all data writing via the $DATA_{7-0}$ bus is inhibited.

$DATA_7$ through $DATA_0$
The 8-bit $DATA_{7-0}$ bus is used to program the two 32-bit Δ-Phase Registers and the two 12-bit Phase Modulation Registers. $DATA_0$ is the least significant bit of the bus. The data programmed into the Δ-Phase registers in this way determines the carrier frequency of the NCO.

$ADDR_3$ through $ADDR_0$
The four address lines $ADDR_{3-0}$ control the use of the $DATA_{7-0}$ bus for writing frequency data to the Δ-Phase Buffer Registers, and phase data to the Phase Buffer Registers, as shown in the table:

$ADDR_3$	$ADDR_1$	$ADDR_0$	Register Field
0	0	0	Δ-Phase Bits 0 (LSB)–7
0	0	1	Δ-Phase Bits 8–15
0	1	0	Δ-Phase Bits 16–23
0	1	1	Δ-Phase Bits 24–31
1	0	0	Sine Bits 0(LSB)–3*
1	0	1	Sine Bits 4-11*
1	1	0	Cosine Bits 0(LSB)–3*
1	1	1	Cosine Bits 4-11*

$ADDR_3$	$ADDR_2$	Register Selected
0	0	Δ-Phase Buffer Register 'A'
0	1	Δ-Phase Buffer Register 'B'
1	X	Phase Buffer Registers

* Note: The Phase Buffer Registers are 12-bit registers. When the least significant bytes of these registers are selected ($ADDR_{3-0}$ =1XX0), $DATA_{7-4}$ is written into Bits 3–0 of the registers. In all cases, it is not necessary to reload unchanged bytes, and the byte loading sequence may be random.

WRSTB
The Write Strobe input is used to latch the data on the $DATA_{7-0}$ bus into the device. On the rising edge of the **WRSTB** input, the information on the 8-bit data bus is transferred to the buffer register selected by the $ADDR_{3-0}$ bus.

FRSEL
The Frequency Register Select line is used to control the mux which selects the Δ-Phase Buffer Register in use. When this signal is high Δ-Phase Buffer Register 'A' is selected as the source for the Δ-Phase ALU, and the frequency corresponding to the data stored in this register will be generated by the NCO after the next falling edge on the **FRLD** input. When this line is low, Δ-Phase Buffer Register 'B' is selected as the source.

FRLD
The Frequency Load input is used to control the transfer of the data from the Δ-Phase Buffer Registers to the Δ-Phase ALU. The data at the output of the Mux Block must be valid during the clock cycle following the falling edge of **FRLD**. The data is then transferred during the subsequent cycle. The frequency of the NCO output will change 19 clock cycles after the **FRLD** command due to pipelining delays.

PHSEL
The Phase Source Select input selects the sources of data for the Phase ALUs. When it is high the sources are the Sine and Cosine Phase Buffer Registers. They are loaded from the $DATA_{7-0}$ bus by setting address line $ADDR_3$ high, as shown in the tables. When **PHSEL** is low, the sources for the phase modulation data are the $DATA_{7-0}$ and $ADDR_{3-0}$ inputs, and the data will be loaded independently of the states of **WRSTB** and **CSEL**. The data on these 12 lines is presented directly as a parallel 12-bit word to both Phase ALUs, allowing high-speed phase modulation. The 12-bit value is latched into the Phase ALUs by means of the **PHLD** input. The data on the $ADDR_{3-0}$ lines is mapped onto Phase Bits 3 to 0 and the data on the $DATA_{7-0}$ lines are mapped onto Phase Bits 11 to 4 in this case. When using the parallel phase load mode **CSEL** and/or **WRSTB** should remain high to ensure that the phase data is not written into the phase and frequency buffer registers of the STEL-1177.

PHLD
The Phase Load input is used to control the latching of the Phase Modulation data into the Phase ALUs. The 12-bit data at the output of the Phase Modulation Control Block must be valid during the clock cycle following the falling edge of **PHLD**. The data is then transferred during the subsequent cycle. The 12-bit phase data is added to the 12 most significant bits of the accumulator output, so that the MSB of the phase data represents a 180° phase change. The source of this data will be determined by the state of **PHSEL**. The phase of the NCO output will change 12 clock cycles after the **PHLD** command, due to pipelining delays.

$FMOD_{15}$ through $FMOD_0$
The Frequency Modulation bus is a 16-bit bus on which the FM data is loaded into the STEL-1177. The data should be a 16-bit unsigned number.

FMSUB
The FM Subtract input controls the Add/Subtract operation of the Δ-Phase ALU. When it is high the FM data on the $FMOD_{15-0}$ bus will be subtracted from the carrier frequency, and when it is low the FM data will be added to the carrier frequency. In this way the FM data can be treated as a 17-bit signed-magnitude number, where the **FMSUB** signal is the sign bit. **FMSUB** is latched at the same time as $FMOD_{15-0}$.

$FMADDR_1$ through $FMADDR_0$
The two inputs $FMADDR_{1-0}$ set the deviation of the frequency modulation by controlling the significance of the FM data in relation to the carrier frequency data. The FM data word will be multiplied by 2^0, 2^4, 2^8, or 2^{12} according to the state of $FMADDR_{1-0}$, and the consequent resolution and maximum values of the deviation are shown in the table below. The values shown are for a clock frequency of 60 MHz.

FM-$ADDR_1$	FM-$ADDR_0$	Mult. factor of FM data	Maximum deviation	Resol-ution
0	0	2^0	± 915 Hz	14 mHz
0	1	2^4	± 14.6 KHz	0.22 Hz
1	0	2^8	± 234 KHz	3.6 Hz
1	1	2^{12}	± 3.75 MHz	57 Hz

FMLD
The FM Load input controls the writing of the frequency modulation data on the $FMOD_{15-0}$ bus and the **FMSUB** input into the device. When $RATE_{1-0}$= 00 the data at the output of the Frequency Modulation Control Block must be valid during the clock cycle following the falling edge of **FMLD**. The data is then transferred during the subsequent cycle. When $RATE_{1-0}$= 01, 10 or 11 are selected the FM data will be loaded automatically without the use of the **FMLD** input. Note that **FMLD** must be held low during automatic operation, otherwise the loading will be inhibited.

SIMLD
The Simultaneous Load input allows the carrier frequency data from the Mux Block and the FM data to be updated simultaneously. When **SIMLD** is low, only the FM data will be updated after a falling edge on **FMLD**. When this input is high, both the FM data and carrier frequency data will be updated simultaneously. When **SIMLD** is low at least four clock cycles are required between falling edges of **FMLD** and **FRLD** to ensure glitch-free changes in the outputs.

$RATE_{1-0}$
The $RATE_{1-0}$ signals control the rate at which the FM data on the $FMOD_{15-0}$ bus is added to or subtracted from the carrier frequency, as shown in the table below:

$RATE_1$	$RATE_0$	Modulation Update Rate
0	0	Manual, with **FMLD** signal
0	1	Every 4th clock cycle
1	0	Every 8th clock cycle
1	1	Every 16th clock cycle

CIN
The Carry Input is an arithmetic carry to the least significant bit of the Accumulator. Normal operation of the NCO requires that **CIN** be set at a logic 0. When CIN is set at a logic 1 the effective value of the Δ-Phase register is increased by one. This allows the resolution of the accumulator to be expanded for higher frequency resolution.

ROUND
The **ROUND** input controls the precision of the $SINE_{11-0}$ and COS_{11-0} outputs. When the **ROUND** input is set high, the sine and cosine signals appearing on the $SINE_{11-0}$ and COS_{11-0} buses are accurate to 12 bits. In some instances it may be desirable to use only the 8 MSBs of these outputs. In such circumstances the outputs appearing on the $SINE_{11-0}$ and COS_{11-0} buses can be rounded to present a more accurate 8-bit representation of the signal by setting the **ROUND** input low.

COSEN
The Cosine Enable input controls the power supply to the Cosine Lookup Table. When it is low the cosine lookup table in the STEL-1177 is disabled, and only the $SINE_{11-0}$ outputs will be valid. This reduces the power consumption of the device by approximately 30%.

OUTPUT SIGNALS

$SINE_{11-0}$
The signal appearing on the $SINE_{11-0}$ outputs is derived from the 13 most significant bits of the Phase Accumulator. The 12-bit sine function is presented in offset binary format. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 (801_H). When the phase modulation is zero the value of the output for a given phase value follows the relationship:

$$SINE_{11-0}=2047 \times \sin(360 \times (phase+0.5)/8192)°+2048$$

The result is accurate to within 1 LSB. However, when **ROUND** is set low, the value appearing on the $SINE_{11-0}$ outputs will be rounded and will follow the relationship:

$$SINE_{11-4}=127 \times \sin(360 \times (phase+0.5)/8192)°+128$$

The data appearing on the $SINE_{3-0}$ outputs will not be meaningful under these circumstances.

COS_{11-0}
The signal appearing on the COS_{11-0} outputs is derived from the 13 most significant bits of the Phase Accumulator. The 12-bit cosine function is presented in offset binary format. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 4095 (FFF_H). When the phase modulation is zero the value of the output for a given phase value follows the relationship:

$$COS_{11-0}=2047 \times \cos(360 \times (phase+0.5)/8192)°+2048$$

The result is accurate to within 1 LSB. However, when **ROUND** is set low, the value appearing on the COS_{11-0} outputs will be rounded and will follow the relationship:

$$COS_{11-4}=127 \times \cos(360 \times (phase+0.5)/8192)°+128$$

The data appearing on the COS_{3-0} outputs will not be meaningful under these circumstances.

SYNC
The Sync output indicates the instant in time when the frequency, FM, or PM change made at the inputs affects the $SINE_{11-0}$ and COS_{11-0} output signals. The normally high **SYNC** output goes low for one clock cycle 19 clock cycles after an **FRLD** or **FMLD** command, and 12 clock cycles after a **PHLD** command, to indicate the end of the pipeline delay and the start of the new steady state condition.

FMSYNC
The FM Sync output indicates the instant in time when the FM data on the FMOD bus is written into the device. The **FMSYNC** output is normally high and goes low for one clock cycle at a frequency depending on the state of the $RATE_{1-0}$ inputs. In the automatic modulation modes ($RATE_{1-0} \neq 00$) the data on the $FMOD_{15-0}$ bus will be written into the FM Buffer Register on the rising edge of the clock following the falling edge of **FMSYNC**. This signal can be used to synchronize the updating of the FM data externally.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

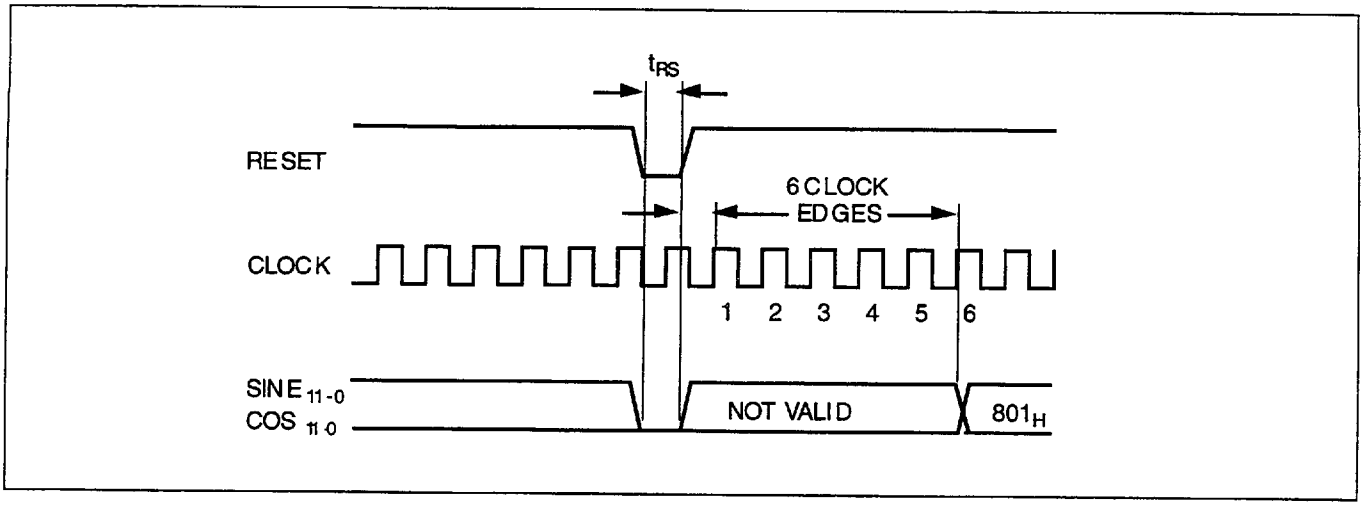
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units	
V_{DD}	Supply Voltage	+5 ± 5% +5 ± 10%	Volts Volts	(Commercial) (Military)
T_a	Operating Temperature (Ambient)	0 to +70 –55 to +125	°C °C	(Commercial) (Military)

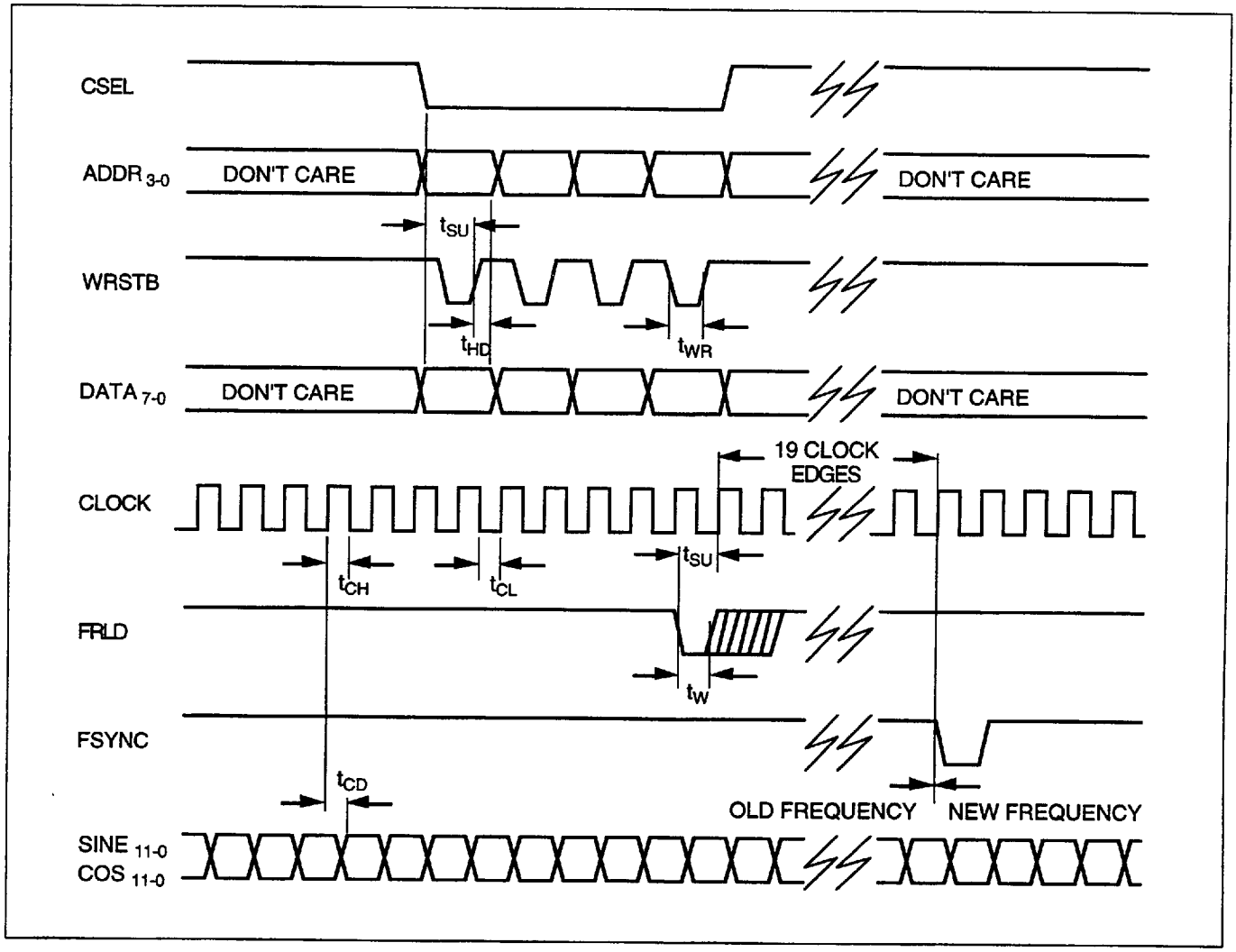
D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, VSS = 0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, VSS = 0 V, Ta = –55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational		7.0		mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**CIN** and **CSEL**, $V_{IN} = V_{DD}$
$I_{IH(min)}$	High Level Input Current			10	µA	All other inputs, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			–10	µA	**CIN** and **CSEL**, $V_{IN} = V_{SS}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	µA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

NCO RESET SEQUENCE

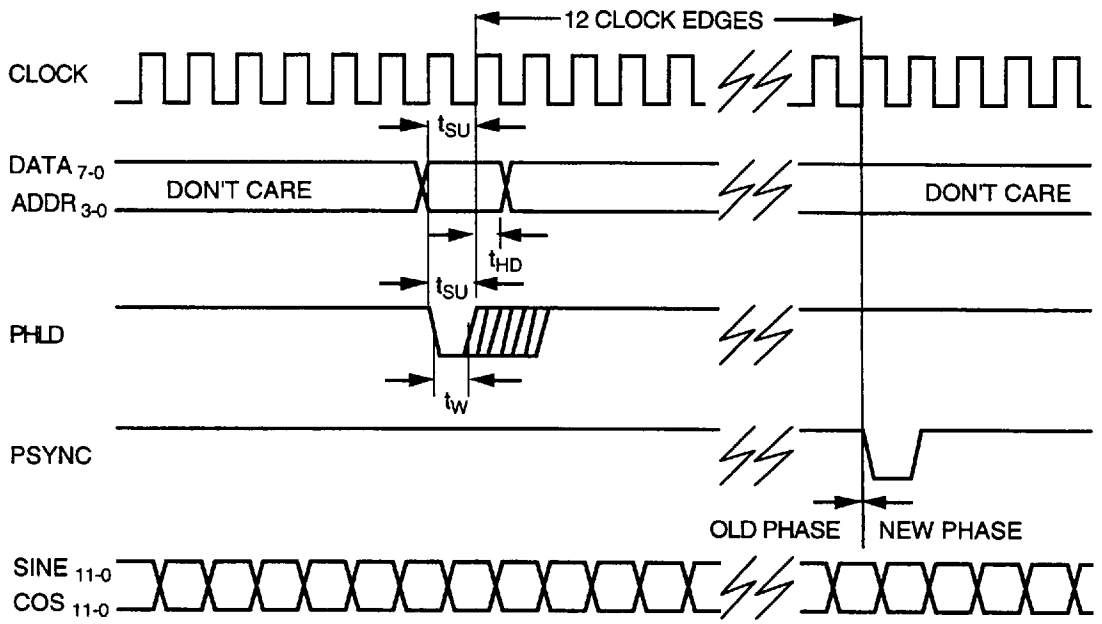


NCO FREQUENCY CHANGE SEQUENCE



NCO PHASE CHANGE SEQUENCE

1. PHSEL=0. DIRECT LOADING.



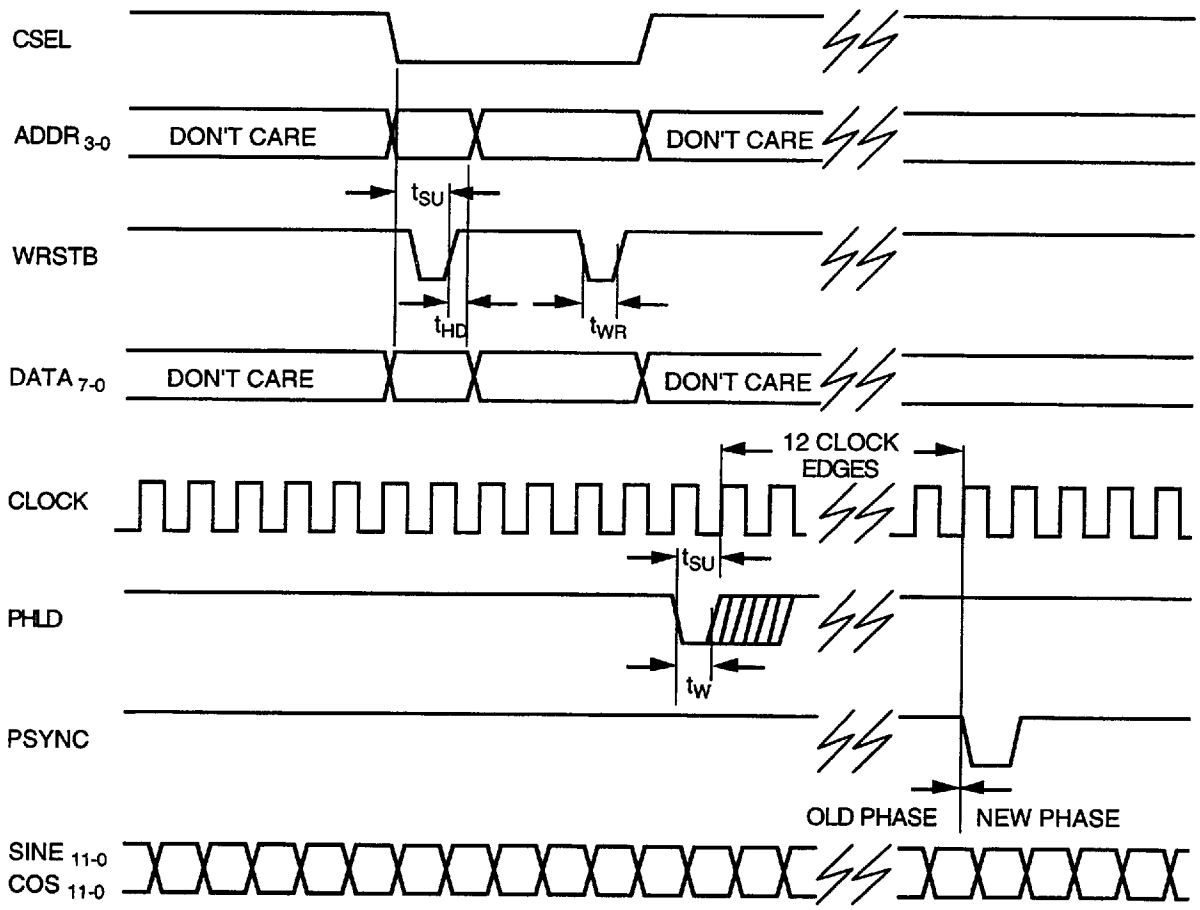
ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ± 10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

Symbol	Parameter	Commercial			Military			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{RS}	**RESET** pulse width	20			25			nsec.	
t_{SR}	**RESET** to **CLOCK** Setup	10			12			nsec.	
t_{SU}	**DATA, ADDR** or **CSEL** to **WRSTB** or **PHLD** Setup and **FRLD, PHLD, FMLD** or **FMOD** to **CLOCK** Setup	5			5			nsec.	
t_{HD}	**DATA, ADDR** or **CSEL** to **WRSTB** or **PHLD** Hold and **FRLD, PHLD, FMLD** or **FMOD** to **CLOCK** Hold	5			5			nsec.	

NCO PHASE CHANGE SEQUENCE

2. PHSEL=1. BUS LOADING.



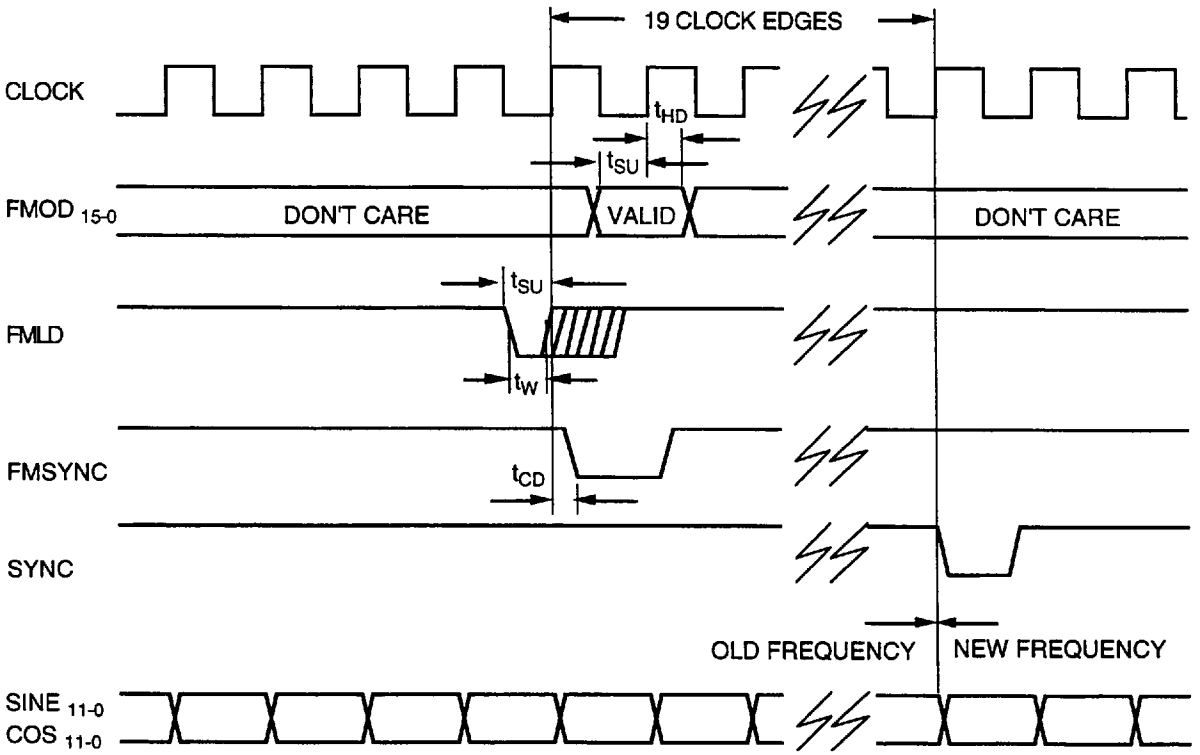
ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= 0° to 70° C, Chimerical
V_{DD}= 5.0 V ± 10%, V_{SS}=0 V, T_a=-55° to 125° C, Military)

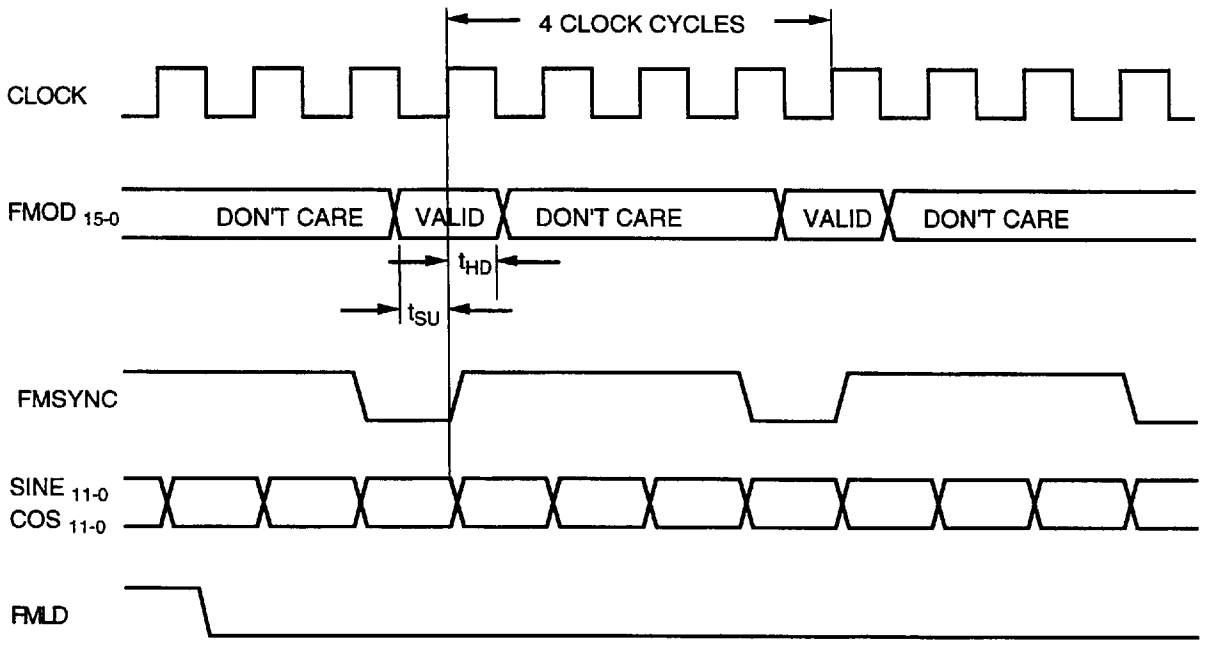
Symbol	Parameter	Commercial			Military			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{CH}	CLOCK high	5						nsec.	f_{CLK} = 60 MHz
					8			nsec.	f_{CLK} = 40 MHz
t_{CH}	CLOCK low	5						nsec.	f_{CLK} = 60 MHz
					8			nsec.	f_{CLK} = 40 MHz
t_W	WRSTB, FRLD, PHLD or FMLD pulse width	5			8			nsec.	
t_{CD}	CLOCK to output delay (All outputs)	7		12	3		20	nsec.	Load = 15 pF

NCO FREQUENCY MODULATION SEQUENCE

1. RATE = 00. MANUAL LOADING.

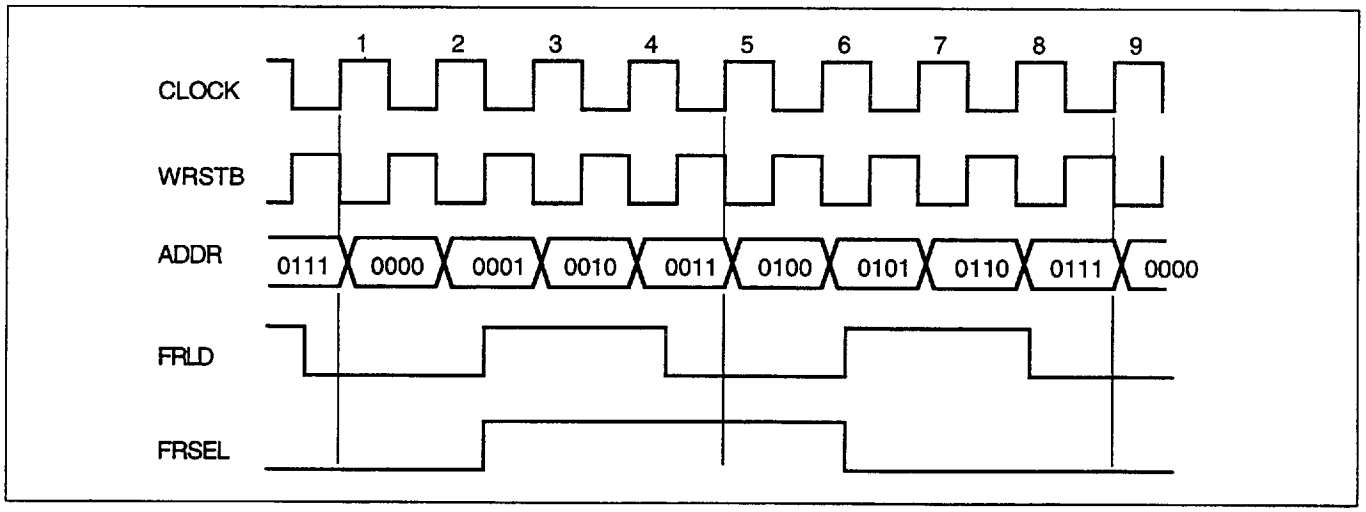


2. RATE ≠ 00. AUTOMATIC LOADING. (RATE = 01 shown)

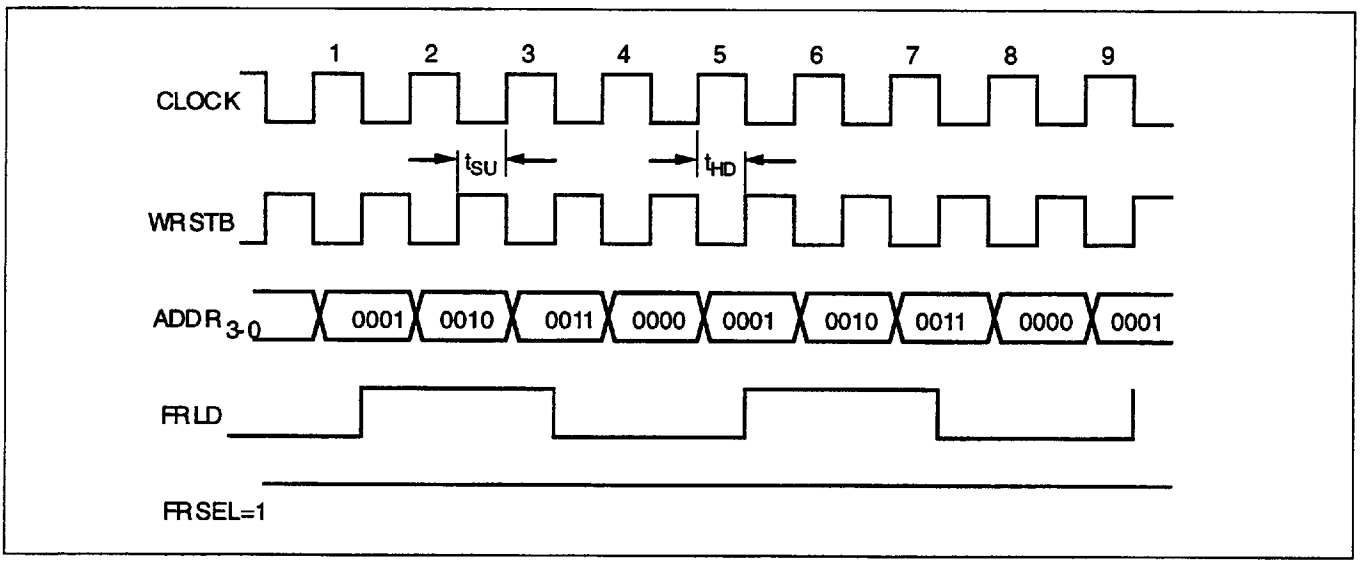


HIGH-SPEED FREQUENCY CHANGE

The frequency of the STEL-1177 NCO can be changed as rapidly as 25% of the clock frequency. This is done by synchronizing the writing to the two Δ-Phase Buffer Registers, and updating both every eight clock cycles. The timing for this procedure is shown below. Each Δ-Phase Buffer Register is loaded while the contents of the other are being transferred into the ALU Buffer Register. The sequence for a load cycle begins on the rising edge of the clock following a falling edge of **FRLD** (or a falling edge of **FMLD** if **SIMLD** is high). In the diagram below, Δ-Phase Buffer Register A is being loaded in clock cycles 1 through 4, while the contents of Δ-Phase Buffer Register B are being transferred, because **FRSEL** was low during the falling edge of **FRLD**. The reverse process happens during clock cycles 5 through 8, and the process then repeats starting in clock cycle 9. The **FRLD** signal can be used to clock a bistable latch to generate the **FRSEL** signal. The maximum update rate is 25%.



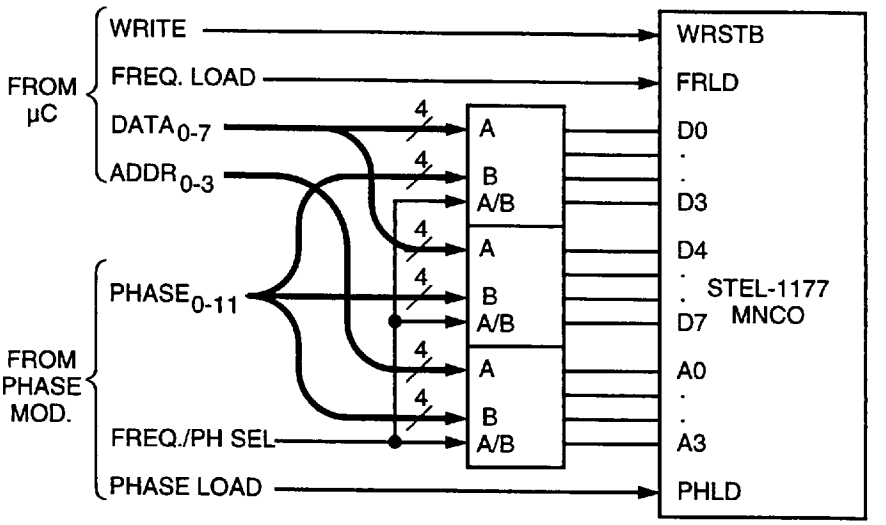
It is possible to update the frequency at up to 25% of the clock frequency using only one buffer register. The timing for this procedure is shown in the diagram below, and must be adhered to rigorously in order to assure adequate setup and hold times. The most critical factor is the setup time (t_{SU}) for the **WRSTB** relative to the clock (rising edge to rising edge). This must be 8 nsec. for correct operation. Since this may be slightly more than half the clock period at high speeds some advantage can be gained by generating the clock by inverting the **WRSTB** signal, rather than the other way around. This makes the propagation delay of the inverter used work for the timing requirements instead of against them, since the hold time requirement from the previous rising edge of the clock (t_{HD}) is 2 nsec.



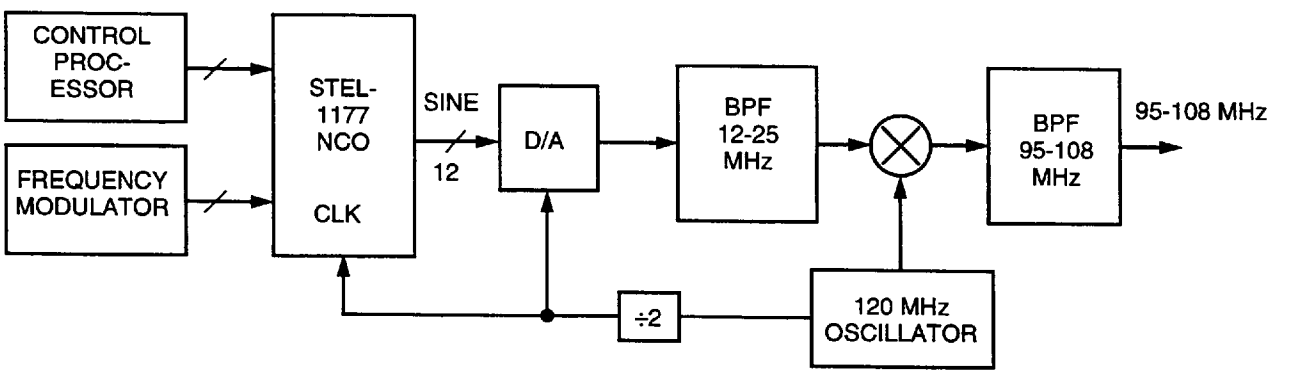
APPLICATIONS INFORMATION

USING THE STEL-1177 IN A HIGH-SPEED PHASE MODULATOR

By routing the data and address lines from the microcontroller via 2:1 multiplexers (e.g. 74HC157) the MNCO can be set up from the microcontroller and then phase modulated at high-speed from an external source. The **PHSEL** line should be set to a logic 0 to enable this mode of operation. The system shown modulates all 12 bits. In a typical PSK system only 1 to 4 bits of modulation will be used, simplifying the system considerably.



APPLICATION EXAMPLE - A HIGH-LINEARITY FM CARRIER GENERATOR



The STEL-1177 can be used for high-linearity frequency modulation. The FM port has 16-bit resolution and linearity, and this can be used to generate a very high-quality signal for FM broadcasting in the 88-108 MHz frequency band. The audio signal can be digitized at a very high sampling rate, either directly or by interpolation, to maximize the performance capability of the system.

SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

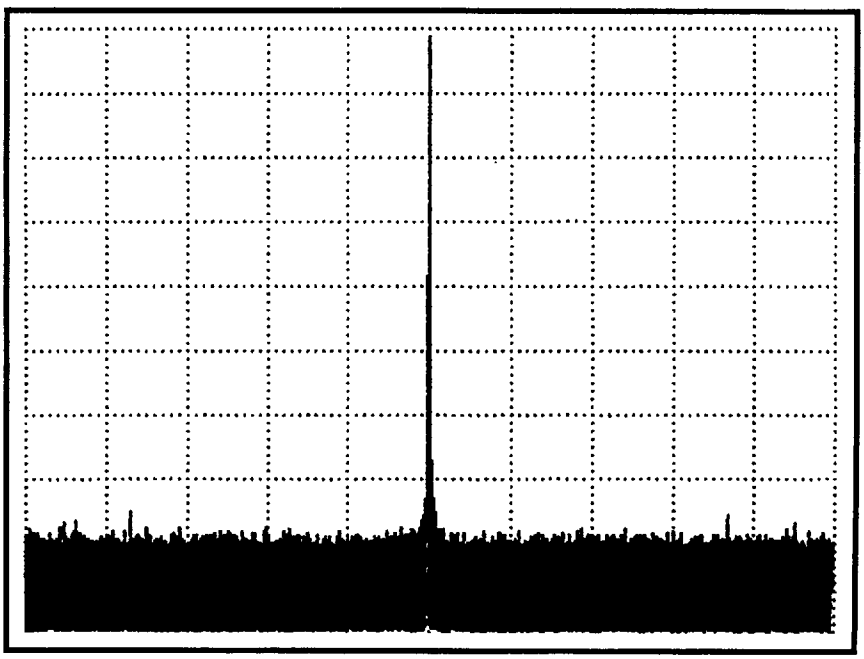
The sine and cosine signals generated by the STEL-1177 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically at least 75 dB down. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of

the NCO approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 60 MHz and the output frequency is programmed to 6.789 MHz. This 10-bit DAC gives better performance than any of the currently available 12-bit DACs at clock frequencies higher than 10 or 20 MHz. The maximum non-harmonic spur level observed over the entire useful output frequency range in this case is –74 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	6.7 MHz
Frequency Span:	10.0 MHz
Reference Level:	–5 dBm
Resolution Bandwidth:	1 KHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div
Output frequency:	6.789 MHz
Clock frequency:	60 MHz



FOR FURTHER INFORMATION

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