

82961KA PAGE PRINTER CONTROLLER

- **High Integration i960® Page Printer Controller⁽¹⁾**
 - Direct Interface to 32-bit 80960KA or KB⁽²⁾ Embedded Processors
- **Direct Non-Impact Printer Video Interface**
 - Automatic DMA Burst DRAM Access to Transmit Video Image
 - Internal Phase Lock Loop
 - Top and Left Margin, Page Height and Width
- **Direct Generic Printer Engine Interface to TEC, Canon, Ricoh and Okidata Printer Engines**
- **Programmable ROM/EPROM Interface**
 - Direct Interface to Two Banks
 - Expandable to Eight Banks
 - Programmable ROM Size and Wait States
- **Programmable System Timer**
- **Programmable DRAM Interface**
 - Direct Interface to Four Banks
 - Programmable DRAM Size and Wait States
 - Page Mode Cache to Reduce Wait States on First Access
 - Transparent Refresh of DRAM Banks
 - Interfaces to 16- and 32-bit DRAM Systems
- **Programmable I/O Control**
 - Chip-Select, Access Time, Recovery Time
 - Wait State Control for Eight External Devices
- **Burst Interface Support for i960 KA/KB Bus**
- **Automatic Data Conversion from 16-bit Font Cartridge to 32-bit i960 Embedded Processor Format**
- **Low-Cost 132-Lead Plastic Quad Flat Pack (PQFP)**

Intel's 82961KA page printer controller is the first member of a new family of page printer companion peripherals that address the need for high integration and cost reduction. It is designed to interface Intel's 80960K-series of embedded processors to a variety of non-impact or laser printer mechanisms. The 82961KA controller contains complete DRAM, ROM and I/O controllers, the associated logic required to control virtually all non-impact printer mechanisms, a programmable wait state generator and programmable chip select generation logic. The 82961KA controller—coupled with an 80960Kx plus DRAM, ROM and the appropriate I/O—forms the nucleus for a cost-effective non-impact printer controller.

Designs that employ the 82961KA controller provide substantial system performance improvements. The 82961KA device decouples DRAM and video output subsystems from the synchronous 80960KA/KB bus to achieve increased performance. The 82961KA device's unique programmable video output controller manages virtually every aspect of memory address generation, timing and control once the device begins to produce the video output signal.

1. The 82961KA i960 Page Printer Controller is based on the single-chip controller architecture created by Peerless Systems Corp.

2. Throughout this data sheet, 80960Kx refers to the 80960KA and KB processors.

82961KA

Page Printer Controller

CONTENTS	PAGE	CONTENTS	PAGE
1.0 PURPOSE	3-331	5.0 ABSOLUTE MAXIMUM RATINGS	3-342
2.0 82961KA FUNCTIONAL OVERVIEW	3-331	6.0 TARGETED DC CHARACTERISTICS	3-343
3.0 PACKAGE INFORMATION	3-332	7.0 TARGETED AC CHARACTERISTICS	3-344
3.1 Package Introduction	3-332	7.1 Targeted L-Bus Timing Specifications	3-350
3.2 Pin Descriptions	3-332	7.2 L-Bus Operational Waveforms ...	3-352
3.3 82961KA PQFP Pinout	3-337	7.3 Targeted DRAM Controller Timing Specifications	3-353
3.4 Mechanical Data	3-339	7.4 DRAM Controller Operational Waveforms	3-354
3.5 Package Thermal Specification ..	3-339	7.5 ROM and I/O Controller Operational Waveforms	3-362
3.6 Package Dimensions and Mounting	3-340	7.6 Targeted Printer Video and Communications Timing Specifications	3-368
4.0 ELECTRICAL SPECIFICATIONS ..	3-341		
4.1 Power and Grounding	3-341		
4.2 Power Decoupling Recommendations	3-341		
4.3 Connection Recommendations ..	3-341		

CONTENTS

PAGE

FIGURES

Figure 1	82961KA Block Diagram	3-332
Figure 2	82961KA 132-Lead Plastic Quad Flat Pack (PQFP) Package	3-340
Figure 3	82961KA PQFP Package (Top View)	3-340
Figure 4	Network and Simple Termination Examples	3-341
Figure 5	Typical Supply Current (I_{CC}) vs. Frequency (f_C)	3-344
Figure 6	Typical Supply Current (I_{CC}) vs. Supply Voltage (V_{CC})	3-344
Figure 7	AC Test Loads	3-345
Figure 8	Output Valid Delay (t_{OV}) vs. Load Capacitance	3-345
Figure 9	Clock Input Waveforms	3-346
Figure 10	Synchronous Input/Output Waveforms	3-349
Figure 11	Reset Timing	3-349
Figure 12	L-Bus Relative Timings	3-351
Figure 13	L-Bus Operation	3-352
Figure 14	Internal Register Read/Write	3-352
Figure 15	DRAM Relative Timings	3-353
Figure 16	DRAM Non-Page Read Cycle	3-355
Figure 17	DRAM Non-Page Write Cycle	3-355
Figure 18	DRAM $\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	3-356
Figure 19	DRAM Page Read/Write	3-356
Figure 20	Static Column Mode Read Cycle	3-357
Figure 21	DRAM Page Hit	3-358
Figure 22	DRAM Page Miss	3-359
Figure 23	DRAM 16-Bit Page Mode Read Cycle	3-360
Figure 24	DRAM Aligned 16-Bit Page Mode Write Cycle	3-361
Figure 25	DRAM Non-Aligned 16-Bit Write Cycle	3-361
Figure 26	ROM Burst Read	3-363
Figure 27	I/O Aligned Read or Write	3-364
Figure 28	I/O Packed Read	3-365
Figure 29	I/O Packed Write	3-366

CONTENTS

PAGE

Figure 30	I/O Address Transition in Burst Mode	3-367
Figure 31	I/O Auto-Poll Cycle	3-367
Figure 32	Printer Video Interface Timing	3-370
Figure 33	Printer Communications Interface Timing (82961KA Supplies CCLK)	3-371
Figure 34	Printer Communications Interface Timing (CCLK Supplied Externally)	3-371

TABLES

Table 1	Pin Description Nomenclature	3-332
Table 2	L-Bus Interface Signals	3-333
Table 3	Memory Interface Signals	3-334
Table 4	ROM Signals	3-335
Table 5	I/O Interface Signals	3-335
Table 6	Printer Video Interface Signals	3-335
Table 7	Printer Communications Interface Signals	3-336
Table 8	Processor Control Signals	3-336
Table 9	PQFP Pin Name with Package Location (Signal Order)	3-337
Table 10	PQFP Pin Name with Package Location (Pin Order)	3-338
Table 11	82961KA PQFP Package Thermal Characteristics	3-339
Table 12	Absolute Ratings	3-342
Table 13	Targeted Operating Conditions	3-342
Table 14	Targeted DC Characteristics	3-343
Table 15	Input Clock Specifications	3-346
Table 16	Synchronous Input and Output Specifications	3-347
Table 17	L-Bus Relative Timing Specifications	3-350
Table 18	DRAM Controller Relative Timings	3-353
Table 19	DRAM Controller Programmable Timings	3-354
Table 20	ROM and I/O Controller Programmable Timings	3-362
Table 21	Printer Video Interface Timings	3-368
Table 22	Printer Communications Interface Timings	3-369

1.0 PURPOSE

This data sheet describes the 82961KA page printer controller. It provides the information required to begin designing with the 82961KA printer controller. It contains functional and physical descriptions, electrical characteristics and specifications, absolute maximum ratings and package and pin definitions.

2.0 82961KA FUNCTIONAL OVERVIEW

The 82961KA integrates onto a single chip all the "glue" or support logic required in a 80960Kx processor design with a high performance interface to non-impact printers. 82961KA functional blocks are:

- 80960K-Series L-Bus Interface
- ROM Interface
- DRAM Interface
- I/O Interface
- Printer Video Interface
- Printer Communication Interface
- System Timer

The 82961KA is the first member of a new family of page printer companion peripherals. It is intended to

operate in the non-impact printer environment. However, many of its features make it extremely well-suited for other applications. The 82961KA provides a direct interface between the Intel 80960Kx microprocessor and system memory, communication channels and printer engine.

The 82961KA is designed for flexibility, ease of use and optimum performance while employing a minimal number of external components. A page printer's host communication environment can range from a simple serial or parallel port to a complete Ethernet implementation. To support this vast range, the 82961KA is not limited to any specific communication mechanism. Instead, the 82961KA generates chip-selects and control signals that allow the user to easily connect standard communication devices to the 80960Kx. Additionally, the 82961KA can be used in other operating environments to enhance Intel 80960Kx microprocessors by providing memory interfaces and peripheral timing controls.

In the most simplistic implementations, the system consists of clock and reset generation, an 80960Kx microprocessor, peripheral communications with interface devices, the 82961KA, ROM devices, DRAM devices with series damping resistors, minimal printer interface logic, along with the usual oscillators, connectors and PC board.

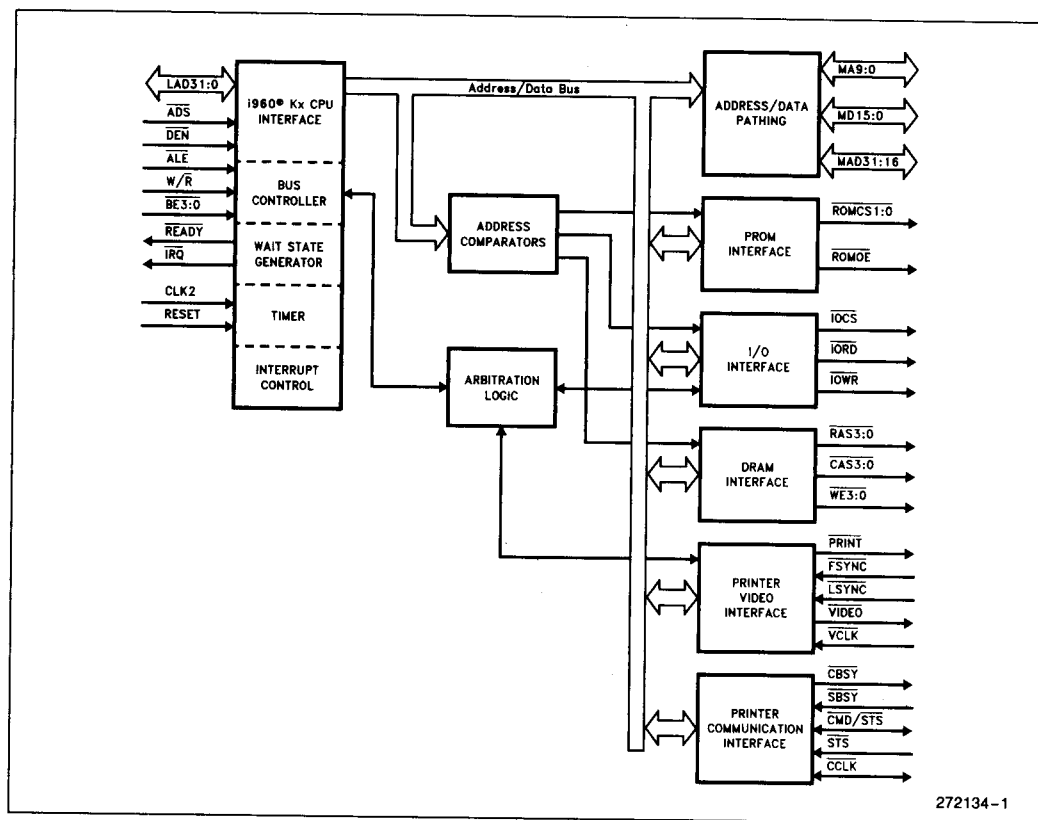


Figure 1. 82961KA Block Diagram

3.0 PACKAGE INFORMATION

3.1 Package Introduction

This section describes the 82961KA pins, pinouts, and thermal characteristics in the 132-pin Plastic Quad Flat Pack (PQFP). For complete package specifications and information, refer to the Intel Packaging Specification (Order No. 231369).

3.2 Pin Descriptions

82961KA pins are described in this section. Table 1 presents the legend for interpreting pin descriptions contained in the following tables. Table 2 defines pins associated with the L-Bus. Tables 3, 4 and 5 define pins associated with memory and I/O interface signals. Table 6 defines pins associated with the printer video interface. Table 7 defines printer communications interface signals. Table 8 defines pins associated with basic processor configuration and control.

Table 1. Pin Description Nomenclature

Symbol(1)	Description
I	Pin is input only
O	Pin is output only
I/O	Pin can be either an input or output
L	Signal is active LOW
L(P)	Signal is active LOW and the signal's sense is programmable
H	Signal is active HIGH
TS	Signal is tristate
OD	Signal is open-drain output
ST	Signal is Schmitt trigger input

NOTE:

1. **Bold** indicates a pin; non-bold indicates a signal.

Table 2. L-Bus Interface Signals

Name	Type	Description
LAD31:0	I/O H TS	LOCAL ADDRESS/DATA BUS carries 32-bit physical address and data to and from memory, I/O devices or internal registers. During an address cycle, bits 31:2 contain a physical word address and bits 1:0 contain a burst size. During a data cycle, bits 31:0 contain read or write data. Burst size is an encoded number where 00 represents one word and 11 represents four words.
ALE	I L	ADDRESS LATCH ENABLE indicates the transfer of a physical address. ALE is asserted during an address cycle and deasserted before a data cycle begins.
ADS	I L	ADDRESS/DATA STATUS indicates an address state. It is asserted during an address cycle and deasserted during a following data cycle. For a burst transaction, ADS is asserted again every data cycle where READY was asserted in the previous cycle.
W/R	I	WRITE/READ specifies, during an address cycle, whether the operation is a write or a read. Valid during entire memory, register or I/O operation.
DEN	I L	DATA ENABLE indicates a transfer on the LAD lines. Asserted during all data cycles.
READY	O OD	READY indicates data on the LAD signals can be sampled or removed. If READY is not asserted during a data transfer, the data cycle is extended to next cycle by inserting a wait state and ADS is not asserted in the next cycle.
BE3:0	I L	BYTE ENABLE: BE signals specify data bytes on the bus which take part in the current data cycle. BE0 corresponds to LAD7:0. BE3 corresponds to LAD31:24. BE signals are pipelined. BE signals corresponding to the first data transfer of a burst are asserted during address cycle. BE signals corresponding to subsequent data transfers of a burst are asserted in the data cycle of the current data transfer.
IRQ	O L OD	INTERRUPT REQUEST indicates an interrupt to the 80960Kx processor. When the 82961KA interrupt is cleared, the signal goes inactive for two bus cycles before it can be reasserted.

Table 3. Memory Interface Signals

Name	Type	Description
MD15:0	I/O H TS	MEMORY DATA signals contain the two least significant data bytes for I/O and DRAM memory operations. MD7:0 contain the least significant byte; MD15:8 contain the second most significant byte. If DRAM is configured as 16 bits wide, or the I/O channel being accessed is packed, MD7:0 also contain the third most significant byte and MD15:8 also contain the most significant byte. During a DRAM write operation, only those bytes with a corresponding write enable signal asserted are driven by the 82961KA.
MAD31:29	I/O H TS	MEMORY ADDRESS/DATA signals are multi-purpose depending on the device that is selected: ROM MAD31 is not used. MAD30:39 signals output an encoded address range select and are driven high or low. I/O Signals output an encoded address range selected. DRAM Signals contain data bits 29–31 when DRAM is in 32-bit configuration. When DRAM is in 16-bit configuration, these signals are unused and are floated. During a DRAM write operation, only those bytes with a corresponding write enable signal asserted are driven by the 82961KA.
MAD28:16	I/O H TS	MEMORY ADDRESS/DATA signals are multi-purpose depending on the device selected: ROM MAD16 is not used. MAD25:17 output address bits 02–08, 17, 19. MAD28:26 are not used and are driven high or low. I/O Signals output address bits 01–08, 17, 19, 21–23. DRAM Signals contain data bits 16–28 with DRAM in 32-bit configuration. When DRAM is in 16-bit configuration, signals are unused and are floated. During a DRAM write operation, only those bytes with a corresponding write enable signal asserted are driven by the 82961KA.
MA9:0	O H	MEMORY ADDRESS signals are multi-purpose depending on the device selected: ROM Signals output address bits 09–16, 18, 20. I/O Signals output address bits 09–16, 18, 20. DRAM Signals output multiplexed address bits 00-09. The number of address bits actually multiplexed on these signals depends on the DRAM bank accessed and the programmed size for that bank. Use MA7:0 for 64 Kbit x 16/32 DRAM; use MA8:0 for 256 Kbit x 16/32 DRAM; use MA9:0 for 1 Mbit x 16/32 DRAM.
RAS3:0	O L	ROW ADDRESS STROBE signals, used for DRAM accesses, are asserted when MA9:0 signals contain a valid row address. RAS0 corresponds to the first DRAM bank; RAS3 corresponds to the fourth DRAM bank. In page mode the RAS signal of the accessed bank remains asserted after completion of the memory operation, and is deasserted for a bank when a page miss occurs.
CAS3:0	O L	COLUMN ADDRESS STROBE signals, used for DRAM accesses, are asserted when MA9:0 signals contain a valid column address. CAS0 corresponds to the first DRAM bank; CAS3 corresponds to the fourth DRAM bank. Only one of the four CAS signals is asserted during a memory operation.
WE3:0	O L	WRITE ENABLE signals, used for DRAM accesses, are asserted during write operations. For 32-bit wide DRAM, WE0 corresponds to the least significant byte MD7:0 and WE3 corresponds to the most significant byte MD31:24. WE0 also corresponds to the 80960Kx BE0 signals and WE3 corresponds to the BE3 signal. Only those WE signals with a corresponding asserted BE signal are asserted. For 16-bit wide DRAM, WE0 corresponds to both the least significant byte, and the third most significant byte, which uses MD7:0. WE1 corresponds to both the second most significant byte and the most significant byte, which uses MD15:8. WE0 also corresponds to BE0 and BE2; WE1 corresponds to BE1 and BE3. For 16-bit wide DRAM, DRAM accesses are performed in two 16-bit accesses; WE2 and WE3 are unused and are deasserted.

Table 4. ROM Signals

Name	Type	Description
ROMCS1:0	I/O L TS	ROM CHIP SELECT signals indicate an access to one of the eight ROM banks. ROMCS0 is used for ROM banks 0–3; ROMCS1 for ROM banks 4–7. While ROMCS0 or ROMCS1 is asserted, the encoded address range select signals MAD30:29 determine the particular ROM bank to be accessed. MAD30:29 signals are guaranteed to be valid during the entire time that ROMCS1:0 is asserted. ROMCS0 and ROMCS1 are never asserted at the same time. These signals are valid during the entire memory operation. During reset, ROMCS0 is used as an input to indicate DRAM bus width. If this pin is low during reset, DRAM is configured as a 16-bit bus. If this pin is high, DRAM is configured as a 32-bit bus. This pin is either pulled up (for a 32-bit bus) or pulled down (for a 16-bit bus) through a 10 KΩ resistor. During reset, ROMCS1 is used as an input to clear ROM bank 0 size field to zero, disabling it. This allows external ROM and control circuit at address zero. If pin is low during reset, ROM bank 0 is disabled. If pin is high, ROM bank 0 is enabled as normal. This pin is either pulled up (enabled) or pulled down (disabled) through a 10 KΩ resistor.
ROMOE	O L	ROM OUTPUT ENABLE corresponds to the $\overline{\text{DEN}}$ signal and is asserted during all data cycles to any of the eight ROM banks.

Table 5. I/O Interface Signals

Name	Type	Description
IOCS	O L	I/O CHIP SELECT indicates an access to one of the eight I/O device address ranges in an auto-poll cycle. It is asserted at the beginning of an I/O operation and remains asserted for a programmed duration of I/O device select. While IOCS is asserted, encoded address range select signals MAD31:29 determine the particular I/O channel to be accessed. MAD31:29 signals are guaranteed to be valid during the entire time that IOCS is asserted.
IOWR	O L	I/O WRITE indicates a write operation to one of the eight I/O device address ranges. It is asserted a programmed duration after IOCS is asserted and remains asserted for a programmed duration. It is asserted for I/O write operations only.
IORD	O L	I/O READ indicates a read operation to one of the eight I/O device address ranges in an auto-poll cycle. It is asserted a programmed duration after IOCS is asserted and remains asserted for a programmed duration. It is asserted for I/O read operations only.

Table 6. Printer Video Interface Signals

Name	Type	Description
PRINT	O L(P)	PRINT REQUEST indicates printer engine should begin print operation. PRINT signal is a copy of an internal register bit and follows the programming of this bit. For non-printer applications, signal can be used as a general purpose output.
FSYNC	I L(P) ST	FRAME SYNC indicates printer engine began to print and medium is positioned at top of page. When signal is asserted, the 82961KA controller begins sampling LSYNC signal.
LSYNC	I L(P) ST	LINE SYNC indicates printer engine began to move the medium and imaging circuitry is positioned at left page position. Each time this signal is asserted, the 82961KA controller counts down the top margin size or initiates a scanline transfer of video data.

Table 6. Printer Video Interface Signals (Continued)

Name	Type	Description
VIDEO	O L(P)	VIDEO is the digital serial video data stream. It is driven after each assertion of LSYNC signal after any top margin size is counted. By default, a high on this signal indicates "white space" and low indicates "black space".
VCLK	I L(P)	VIDEO CLOCK is the video shift rate clock. If the printer engine supplies a video shift rate clock, it is presented on this pin. If the printer engine does not supply a video shift rate clock, an 8x video shift rate clock must be presented on this pin and the 82961KA must be programmed for phase locked loop operation. In phase locked loop operation, the internal video shift rate clock is locked to LSYNC signal active edge. By default, when programmed for 1x operation the video shift rate clock falling edge shifts a bit of video data.

Table 7. Printer Communications Interface Signals

Name	Type	Description
CBSY	O L OD	COMMAND BUSY indicates 82961KA has command to transmit to the printer engine. CBSY is asserted when 82961KA's printer command register is written; it remains asserted until all command data is sent.
SBSY	I L ST	STATUS BUSY indicates the printer engine has status to transmit to the 82961KA. When signal is asserted, 82961KA assembles a printer engine status byte in the 82961KA's printer status register using eight transitions of CCLK . Note that CCLK may come from the 82961KA or the printer engine, depending on programmed CCLK mode.
CMD/STS	I/O L TS	COMMAND/STATUS DATA is programmable to be either command data output to printer engine or bidirectional command/status data to/from the printer. Command data is an 8-bit serial command stream to a printer engine. After CBSY is asserted by writing the 82961KA's printer command register, each command bit is presented on this signal, accompanied by a transition of the CCLK signal.
STS	I L ST	STATUS DATA is an 8-bit serial status from the printer engine. After SBSY is asserted, the printer engine presents each status bit on this signal with each CCLK transition from the 82961KA controller. SBSY must be deasserted and reasserted to begin a second 8-bit status message.
CCLK	I/O L TS	COMMAND CLOCK is programmable to be either an input clock from the printer engine or an output clock to the printer engine. It causes the printer engine to assemble an 8-bit command or transmit an 8-bit status one bit at a time with each transition of this signal. Each command bit is shifted on a falling edge of CCLK and each status bit is sampled on a rising edge of CCLK .

Table 8. Processor Control Signals

Name	Type	Description
CLK2	I	SYSTEM CLOCK provides the fundamental timing for the 82961KA. It is twice the frequency of an 80960Kx address or data cycle.
RESET	I ST	RESET clears 82961KA internal logic and initializes all internal registers.
V_{CC}	I	SYSTEM POWER connections consist of eight pins; it is strongly recommended that these are connected externally to a V_{CC} board plane.
V_{SS}	I	SYSTEM GROUND consists of 10 pins; it is strongly recommended that these are connected externally to a V_{SS} board plane.

3.3 82961KA PQFP Pinout

Tables 9 and 10 list 82961KA pin names and package location. See Section 4, Electrical Specifications for specifications and recommended connections.

Table 9. PQFP Pin Name with Package Location (Signal Order)

L-Bus		L-Bus (Continued)		Memory (Continued)		Memory (Continued)	
Name	Location	Name	Location	Name	Location	Name	Location
LAD31	128	DEN	117	MD3	51	MAD28	92
LAD30	129	READY	126	MD4	52	MAD29	93
LAD29	130	BE3	121	MD5	53	MAD30	94
LAD28	131	BE2	122	MD6	54	MAD31	95
LAD27	132	BE1	123	MD7	56		
LAD26	1	BE0	124	MD8	57	DRAM	
LAD25	2	IRQ	125	MD9	59	Name	Location
LAD24	4			MD10	60	WE3	33
LAD23	5	I/O		MD11	61	WE2	34
LAD22	6	Name	Location	MD12	62	WE1	35
LAD21	7	IOCS	96	MD13	63	WE0	36
LAD20	8	IOWR	97	MD14	64	RAS3	37
LAD19	9	IORD	98	MD15	65	CAS3	38
LAD18	11			MA0	66	RAS2	40
LAD17	12	Printer Video		MA1	67	CAS2	41
LAD16	13	Name	Location	MA2	68	RAS1	43
LAD15	15	VIDEO	109	MA3	69	CAS1	44
LAD14	16	PRINT	110	MA4	70	RAS0	45
LAD13	17	VCLK	111	MA5	71		
LAD12	18	LSYNC	112	MA6	73	ROM	
LAD11	19	FSYNC	113	MA7	74	Name	Location
LAD10	20			MA8	75	ROMOE	99
LAD9	21	Printer Comm		MA9	76	ROMCS1	100
LAD8	23	Name	Location	MAD16	77	ROMCS0	101
LAD7	24	STS	102	MAD17	78		
LAD6	25	SBSY	104	MAD18	80	Control	
LAD5	27	CCLK	105	MAD19	81	Name	Location
LAD4	28	CMD/STS	107	MAD20	82	CLK2	114
LAD3	29	CBSY	108	MAD21	84	RESET	116
LAD2	30			MAD22	85		
LAD1	31	Memory		MAD23	86	Vcc	
LAD0	32	Name	Location	MAD24	88	14, 26, 49, 58, 72, 103, 115, 127	
ALE	119	CAS0	46	MAD25	89		
ADS	118	MD0	47	MAD26	90	Vss	
W/R	120	MD1	48	MAD27	91	3, 10, 22, 39, 42, 55, 79, 83, 87, 106	
		MD2	50				

Table 10. PQFP Pin Name with Package Location (Pin Order)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	LAD26	34	WE $\overline{2}$	67	MA1	100	ROMCS $\overline{1}$
2	LAD25	35	WE $\overline{1}$	68	MA2	101	ROMCS $\overline{0}$
3	V $\overline{SS}$	36	WE $\overline{0}$	69	MA3	102	STS
4	LAD24	37	RAS $\overline{3}$	70	MA4	103	V $\overline{CC}$
5	LAD23	38	CAS $\overline{3}$	71	MA5	104	SBSY
6	LAD22	39	V $\overline{SS}$	72	V $\overline{CC}$	105	CCLK
7	LAD21	40	RAS $\overline{2}$	73	MA6	106	V $\overline{SS}$
8	LAD20	41	CAS $\overline{2}$	74	MA7	107	CMD/STS
9	LAD19	42	V $\overline{SS}$	75	MA8	108	CBSY
10	V $\overline{SS}$	43	RAS $\overline{1}$	76	MA9	109	VIDEO
11	LAD18	44	CAS $\overline{1}$	77	MAD16	110	PRINT
12	LAD17	45	RAS $\overline{0}$	78	MAD17	111	VCLK
13	LAD16	46	CAS $\overline{0}$	79	V $\overline{SS}$	112	LSYNC
14	V $\overline{CC}$	47	MD0	80	MAD18	113	FSYNC
15	LAD15	48	MD1	81	MAD19	114	CLK2
16	LAD14	49	V $\overline{CC}$	82	MAD20	115	V $\overline{CC}$
17	LAD13	50	MD2	83	V $\overline{SS}$	116	RESET
18	LAD12	51	MD3	84	MAD21	117	DEN
19	LAD11	52	MD4	85	MAD22	118	ADS
20	LAD10	53	MD5	86	MAD23	119	ALE
21	LAD9	54	MD6	87	V $\overline{SS}$	120	W/R
22	V $\overline{SS}$	55	V $\overline{SS}$	88	MAD24	121	BE $\overline{3}$
23	LAD8	56	MD7	89	MAD25	122	BE $\overline{2}$
24	LAD7	57	MD8	90	MAD26	123	BE $\overline{1}$
25	LAD6	58	V $\overline{CC}$	91	MAD27	124	BE $\overline{0}$
26	V $\overline{CC}$	59	MD9	92	MAD28	125	IRQ
27	LAD5	60	MD10	93	MAD29	126	READY
28	LAD4	61	MD11	94	MAD30	127	V $\overline{CC}$
29	LAD3	62	MD12	95	MAD31	128	LAD31
30	LAD2	63	MD13	96	IOCS	129	LAD30
31	LAD1	64	MD14	97	IOWR	130	LAD29
32	LAD0	65	MD15	98	IORD	131	LAD28
33	WE $\overline{3}$	66	MA0	99	ROMOE	132	LAD27

3.4 Mechanical Data

Package Dimensions and Mounting

The 82961KA is available in a 132-lead plastic quad flat pack (PQFP). The plastic package uses fine-pitch gull wing leads arranged in a single row along the perimeter of the package with 0.025 inch (0.64 mm) spacing.

The PQFP is normally surface mounted to take best advantage of the plastic package's small footprint and low cost. In some applications, however, designers may prefer to use a socket, either to improve heat dissipation or reduce repair costs.

Pin Assignment

Figures 2 and 3 show the top view of the PQFP; notice that the pins are numbered in order from 1 to 132 around the package's perimeter. Tables 9 and 10 list the function of each pin in the PQFP.

It is strongly recommended that V_{CC} and GND connections be made to multiple V_{CC} and GND pins. Each V_{CC} and GND pin should be connected to the appropriate voltage or ground and externally strapped close to the package. We recommend that you include separate power and ground planes in your circuit board for power distribution.

3.5 Package Thermal Specification

The 82961KA is specified for operation when case temperature is within the range 0°C to $+85^{\circ}\text{C}$ (PQFP). The case temperature should be measured at the top center of the package as shown in Table 11.

The ambient temperature can be calculated from θ_{JC} and θ_{JA} by using the following equations:

$$T_J = T_C + P \cdot \theta_{JC}$$

$$T_A = T_J - P \cdot \theta_{JA}$$

$$T_C = T_A + P \cdot [\theta_{JA} - \theta_{JC}]$$

Table 11. 82961KA PQFP Package Thermal Characteristics

PQFP Thermal Resistance— $^{\circ}\text{C}/\text{Watt}$							
Parameter	Airflow—ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case	9	9	9	9	9	9	9
θ Case-to-Ambient (No Heatsink)	22	19	18	16	11	9	8

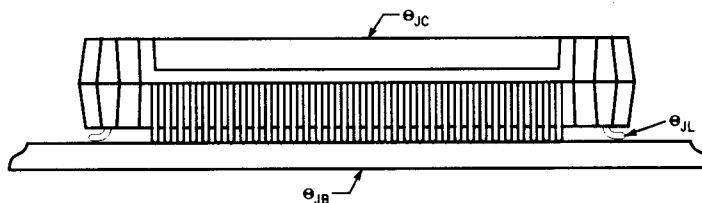
NOTES:

1. This table applies to 82961KA PQFP soldered directly into board.

2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$.

3. $\theta_{JL} = 18^{\circ}\text{C}/\text{Watt}$

$\theta_{JB} = 18^{\circ}\text{C}/\text{Watt}$



272134-36

3

Values for θ_{ja} and θ_{jc} are given in Table 11 for the PQFP for various airflows. Note that the θ_{ja} for the PGA package can be reduced by adding a heatsink, while a heatsink is not generally used with the plastic package since it is intended to be surface mounted. The maximum allowable ambient temperature

(T_A) permitted without exceeding T_C is shown by the charts in Figure 6.

The curves assume the maximum permitted supply current (I_{CC}) at each speed, V_{CC} of 5.0V, and a T_{CASE} of +85°C (PQFP).

3.6 Package Dimensions and Mounting

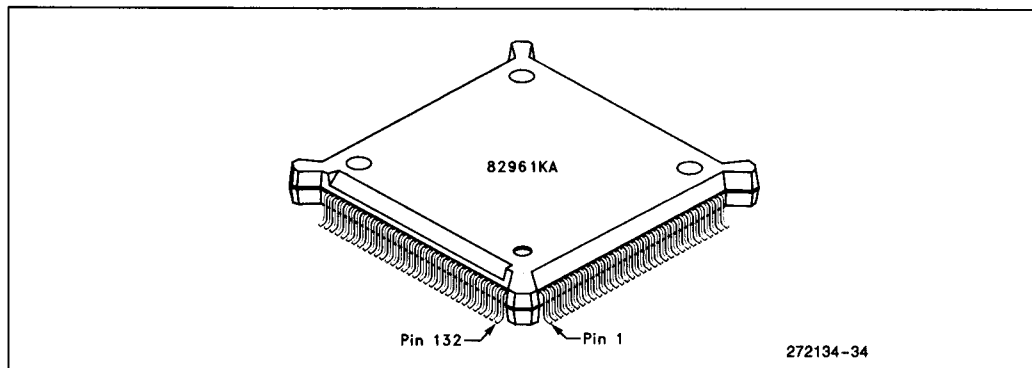


Figure 2. 82961KA 132-Lead Plastic Quad Flat Pack (PQFP) Package

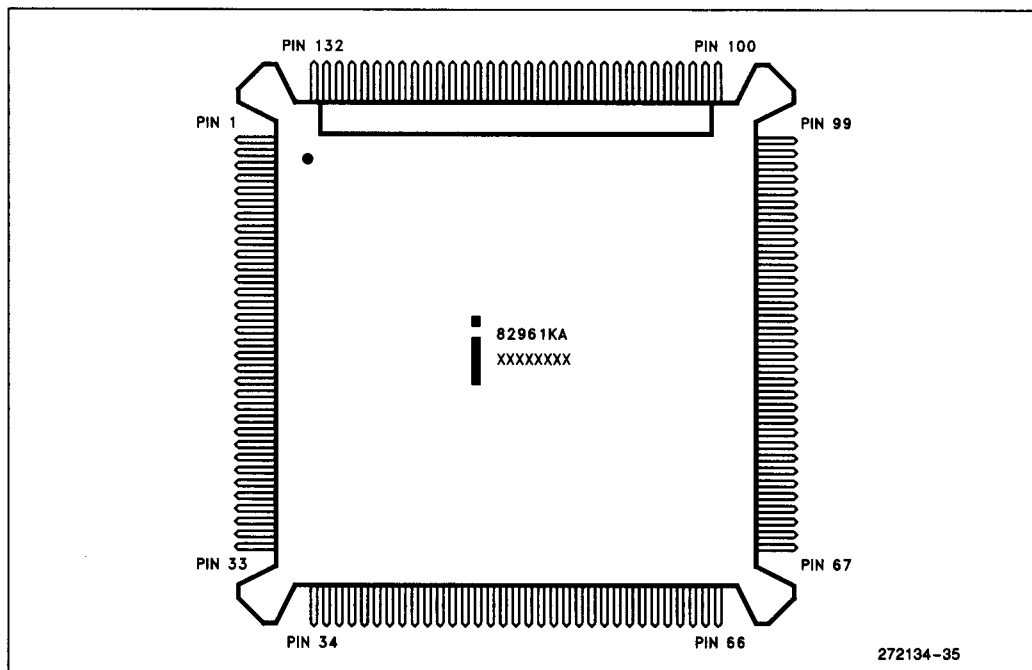


Figure 3. 82961KA PQFP Package (Top View)

4.0 ELECTRICAL SPECIFICATIONS

4.1 Power and Grounding

Power and ground capacitors must be made to all 82961KA power and ground pins. On the circuit board, all V_{CC} pins must be strapped closely together. Similarly, all V_{SS} pins should be strapped closely together. It is strongly recommended that V_{CC} pins are connected to a common power plane and V_{SS} pins are connected to a common ground plane in the PC board.

4.2 Power Decoupling Recommendations

Decoupling capacitors should be placed near the 82961KA. The 82961KA can cause transient power surges when multiple, loaded outputs switch simultaneously. Proper power decoupling is required to avoid "ground lift" or "ground bounce" induced by these power surges.

4.3 Connection Recommendations

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the PC board traces between the processor and decoupling capacitors as much as possible.

For reliable operation, always connect unused inputs to an appropriate signal level. **No unused input pin should be left floating.** Connect unused pins directly to V_{SS} or to V_{CC} through a pull-up resistor.

Recommended value of the pull-up resistor is approximately 20 K Ω for each pin tied high.

Output drivers for $\overline{RAS3:0}$, $\overline{CAS3:0}$, $\overline{WE3:0}$ and $\overline{MA9:0}$ are designed to directly drive the heavy capacitive loads of DRAM arrays. To prevent outputs from ringing in the system, it is necessary to match the output driver's output impedance to that of the DRAM array. This is accomplished by placing a resistor in series with each signal. Place the series resistor near the 82961KA. Resistor value is dependent on DRAM loading and is best determined by experimentation at the prototype level.

All open-drain outputs require a pull-up termination connected to the output pin. Signals $\overline{READY}$, $\overline{IRQ}$ and $\overline{CSBY}$ are open-drain outputs on the 82961KA.

While in most cases a simple pull-up resistor is adequate, a network consisting of pull-up and pull-down resistors may be necessary for the $\overline{READY}$ pin, since timing on this signal is critical.

Figure 4 shows recommendations for low and high current drive network which assumes the circuit board has a characteristic impedance of 100 Ω . The resistor network should bias the output to a valid HIGH level ($V_{IH} \geq 2.0V$). To minimize signal reflection, termination should be placed close to the end of the PC board trace. Pull-up and pull-down resistor value should be chosen such that network impedance closely matches the characteristic impedance of the PC board trace.

Figure 4 also shows a simple pull-up termination which can be used to terminate the open-drain outputs.

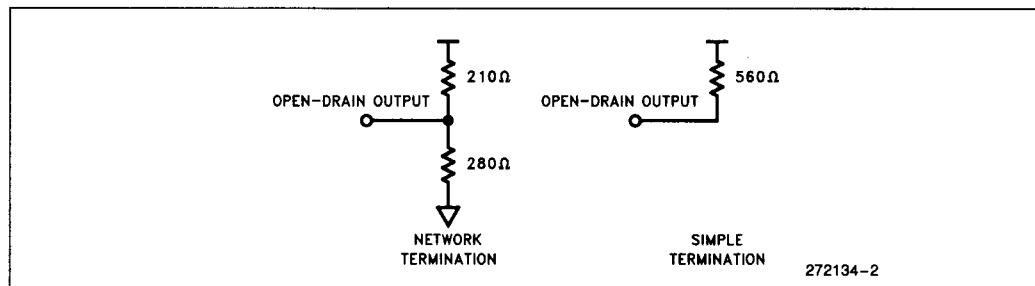


Figure 4. Network and Simple Termination Examples

3

5.0 ABSOLUTE MAXIMUM RATINGS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 12. Absolute Ratings

KU82961KA-20, -16 (20, 16 MHz Specification)				
Parameter/Description	Absolute Ratings			
	Min	Max	Units	Conditions
Storage Temperature	−65	150	°C	
Case Temperature Under Bias	−65	110	°C	
Supply Voltage with Respect to V_{SS}	−0.5	6.5	V	
Voltage on Other Pins with Respect to V_{SS}	−0.5	$V_{CC} + 0.5$	V	

Table 13. Targeted Operating Conditions

KU82961KA-20, -16 (20, 16 MHz Specification)					
Symbol	Parameter/Description	Min	Max	Units	Conditions
V_{CC}	Supply Voltage KU82961KA-20 KU82961KA-16	4.75	5.25	V	(Note 1)
		4.5	5.5		(Note 2)
f_C	Input Clock (CLK2) Frequency KU82961KA-20 KU82961KA-16	1	40	MHz	(Note 1)
		1	32		(Note 2)
T_C	Case Temperature Under Bias KU82961KA-20 KU82961KA-16	0	85	°C	(Note 1)
		0	85		(Note 2)

NOTES:

- 82961KA-20 is tested with voltage supplies set to $\pm 5\%$.
- 82961KA-16 is tested with voltage supplies set to $\pm 10\%$.

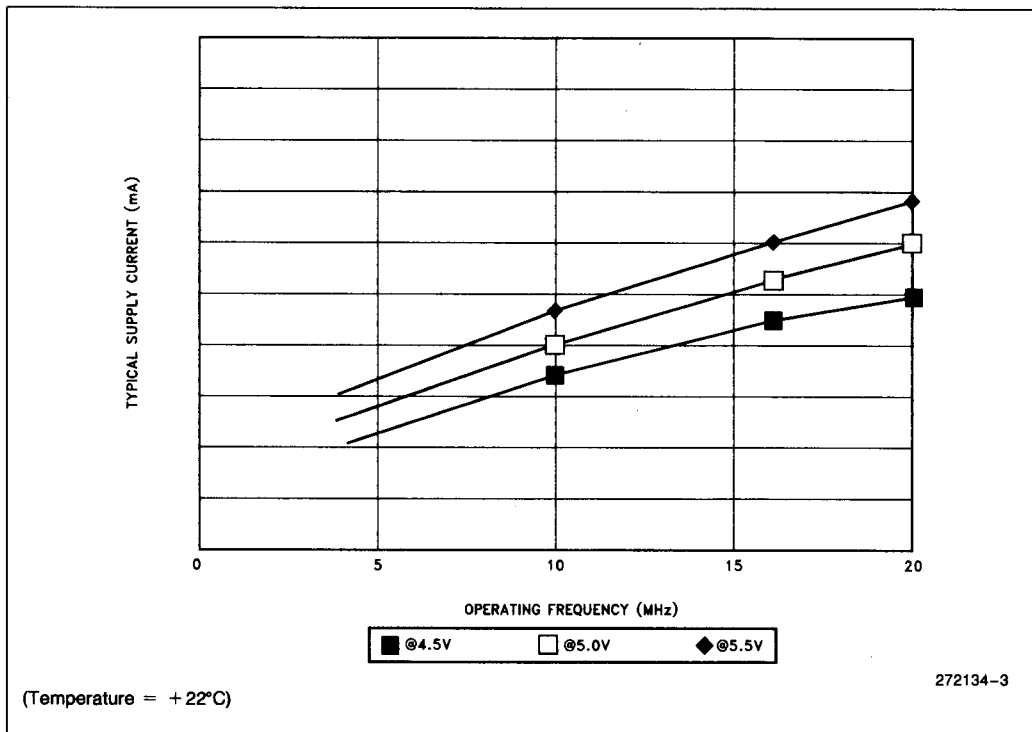
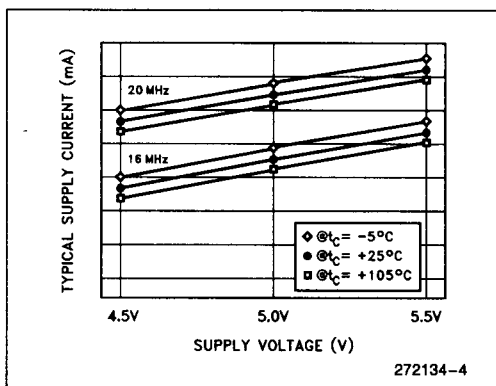
6.0 TARGETED DC CHARACTERISTICS

Table 14. Targeted DC Characteristics

82961KA-20, -16 (20, 16 MHz Specification)					
Symbol	Parameter/Description	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.3	0.8	V	(Note 1)
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V	(Note 1)
V_{OL}	Output Low Voltage		0.45	V	(Note 2)
V_{OH}	Output High Voltage	2.4		V	(Note 3)
I_{CC}	Power Supply Current 82961KA-20 82961KA-16		250 200	mA mA	(Note 4)
I_{LI}	Input Leakage Current		± 10	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{LO}	Output Leakage Current		± 10	μA	$0.45 \leq V_O \leq V_{CC}$
C_{IN}	Input Capacitance		8	pF	$f_C = 1 \text{ MHz}^{(5)}$
C_{IO}	I/O or Output Capacitance		10	pF	$f_C = 1 \text{ MHz}^{(5)}$

NOTES:

1. RESET, FSYNC, LSYNC, SBSY, and STS are Schmitt trigger inputs. Hysteresis on these pins is approximately 200 mV, but is not tested for each device.
2. V_{OL} is measured under the following conditions:
 $I_{OL} = 6 \text{ mA}$ LAD31:0, MAD31:16, MD15:0, $\overline{IOCS}$, $\overline{IORD}$, $\overline{IOWR}$, ROMOE, ROMCS1:0,
RAS3:0, CAS3:0, WE3:0, MA9:0
 $I_{OL} = 12 \text{ mA}$ CCLK, CMD/STS, CBSY, VIDEO, PRINT
 $I_{OL} = 24 \text{ mA}$ READY, IRQ
3. V_{OH} is measured under the following conditions:
 $I_{OH} = 6 \text{ mA}$ LAD31:0, MAD31:16, MD15:0, $\overline{IOCS}$, $\overline{IORD}$, $\overline{IOWR}$, ROMOE, ROMCS1:0,
RAS3:0, CAS3:0, WE3:0, MA9:0
 $I_{OH} = 12 \text{ mA}$ CCLK, CMD/STS, VIDEO, PRINT
 V_{OH} is not measured for open-drain outputs, IRQ, READY, and CBSY
4. Measured at worst case frequency, V_{CC} , and temperature, with device operating and outputs loaded to the test conditions shown in Figure 5.
5. Capacitance values are not tested.

Figure 5. Typical Supply Current (I_{CC}) vs Frequency (f_c)Figure 6. Typical Supply Current (I_{CC}) vs Supply Voltage (V_{CC})

7.0 TARGETED AC CHARACTERISTICS

AC Specifications presented in this document are tested with loading on output pins as shown in Figure 7. Output test load (C_L) is never less than 50 pF unless specifically stated in the AC Specifications.

Figure 8 shows output valid delay as a function of load capacitance. Output valid delays given in the AC Specifications must be adjusted using data in Figure 8 when pin loading in the system exceeds test load, C_L . Derating information is verified at all operating conditions using a sampling of components which represent process extremes. Derating information is not tested for each device.

AC Specifications relating to outputs are measured at the 1.5V crossing point of the output signal unless otherwise indicated. Input signals are driven during test with a rise and fall time of ≤ 2 ns. AC Specifications relating to inputs are measured from the 1.5V crossing point of the input waveform.

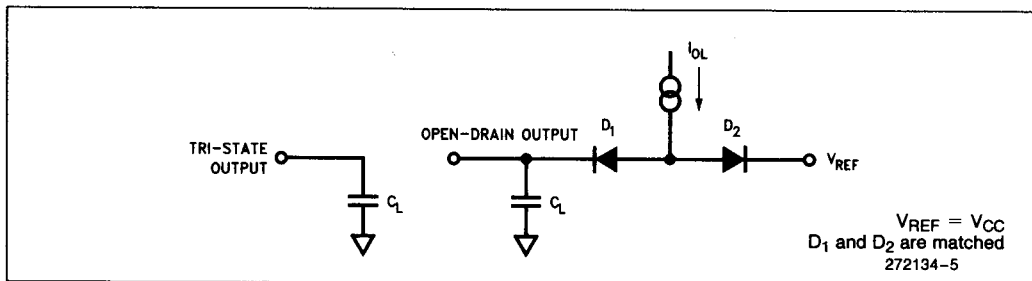


Figure 7. AC Test Loads

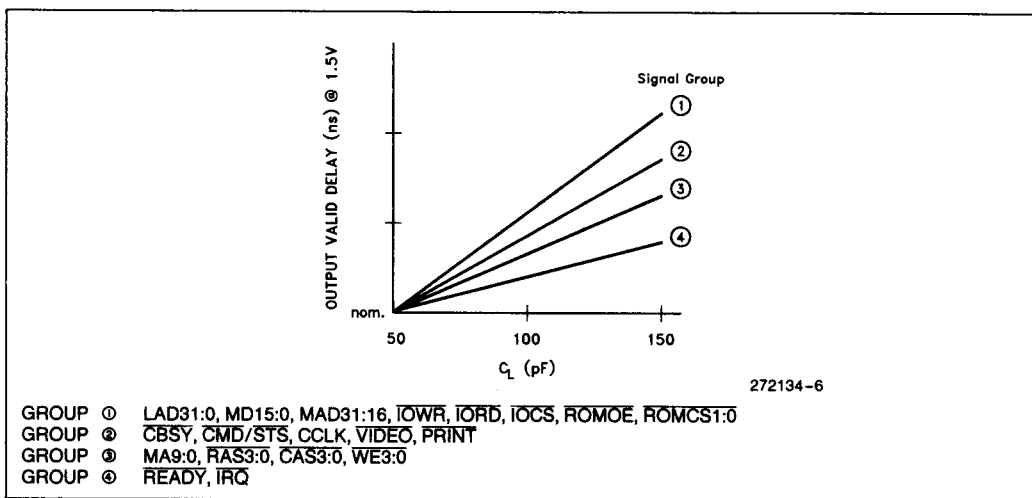


Figure 8. Output Valid Delay (t_{OV}) vs Load Capacitance

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Table 15. Input Clock Specifications

Symbol	Parameter/Description	Min	Max	Units	Conditions
82961KA-20 (20 MHz Specification)					
f_C	CLK2 Frequency	1	40	MHz	(Note 1)
t_C	CLK2 Period	25	1000	ns	(Note 1)
t_{CH}	CLK2 High Time	10		ns	(Note 1)
t_{CL}	CLK2 Low Time	10		ns	(Note 1)
t_{CR}	CLK2 Rise Time		6	ns	(Note 1)
t_{CF}	CLK2 Fall Time		6	ns	(Note 1)
82961KA-16 (16 MHz Specification)					
f_C	CLK2 Frequency	1	32	MHz	(Note 1)
t_C	CLK2 Period	31.25	1000	ns	(Note 1)
t_{CH}	CLK2 High Time	12.5		ns	(Note 1)
t_{CL}	CLK2 Low Time	12.5		ns	(Note 1)
t_{CR}	CLK2 Rise Time		6	ns	(Note 1)
t_{CF}	CLK2 Fall Time		6	ns	(Note 1)

NOTE:

1. See Figure 7 for waveforms and specifications.

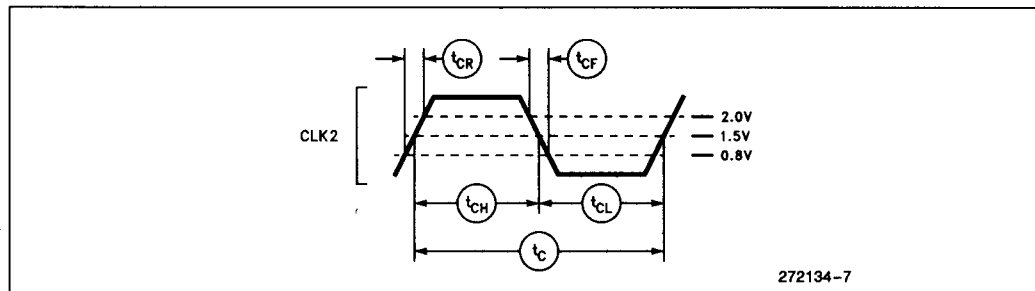


Figure 9. Clock Input Waveforms

Table 16. Synchronous Input and Output Specifications

Symbol	Parameter/Description	Min	Max	Unit	Conditions
82961KA-20 (20 MHz Specification)					
t _{OV} t _{OH}	Output Valid Delay (Maximum Value) Output Hold Delay (Minimum Value)				
t _{OV1} , t _{OH1}	LAD31:0	5	37	ns	Notes 1, 3, 7
t _{OV2} , t _{OH2}	LAD31:0 (register read only)	5	59	ns	Notes 1, 2, 7
t _{OV3} , t _{OH3}	IRQ	5	37	ns	Notes 1, 2
t _{OV4} , t _{OH4}	READY	5	37	ns	Notes 1, 2
t _{OV5} , t _{OH5}	MD15:0	5	33	ns	Notes 1, 3, 10
t _{OV6} , t _{OH6}	MAD31:16 (I/O cycles only)	5	34	ns	Notes 1, 3, 9
t _{OV7} , t _{OH7}	MAD31:16 (ROM cycles only)	5	31	ns	Notes 1, 2, 9
t _{OV8} , t _{OH8}	MAD31:29 (auto-poll only)	5	37	ns	Notes 1, 6, 9
t _{OV9} , t _{OH9}	MA9:0	5	32	ns	Notes 1, 4, 8
t _{OV10} , t _{OH10}	RAS3:0, CAS3:0	5	26	ns	Notes 1, 4
t _{OV11} , t _{OH11}	WE3:0	5	34	ns	Notes 1, 5
t _{OV12} , t _{OH12}	ROMCS1:0, ROMOE	5	24	ns	Notes 1, 2
t _{OV13} , t _{OH13}	IOCS, IORD, IOWR	5	27	ns	Notes 1, 3
t _{OV14} , t _{OH14}	IOCS, IORD (auto-poll only)	5	31	ns	Notes 1, 3
t _{OV15} , t _{OH15}	PRINT		28	ns	Notes 1, 2
t _{OF}	Output Float Delay				
t _{OF1}	MD15:0		33	ns	Notes 1, 11
t _{OF2}	MAD31:16		37	ns	Notes 1, 11
t _{IS}	Input Setup Time				
t _{IS1}	ADS, W/R, BE3:0, DEN	42		ns	Notes 1, 2
t _{IS2}	LAD31:0	10		ns	Notes 1, 2, 12
t _{IS3}	MD15:0	8		ns	Notes 1, 3, 13
t _{IS4}	MAD31:16	8		ns	Notes 1, 3, 14
t _{IS5}	RESET	0		ns	Notes 1, 3
t _{IS6}	ROMCS1:0 (on RESET)	0		ns	Notes 1, 3
t _{IH}	Input Hold Time				
t _{IH1}	ADS, W/R, BE3:0, DEN	2		ns	Notes 1, 2
t _{IH2}	LAD31:0	2		ns	Notes 1, 2, 12
t _{IH3}	MD15:0	8		ns	Notes 1, 3, 13
t _{IH4}	MAD31:16	10		ns	Notes 1, 3, 14
t _{IH5}	RESET	5		ns	Notes 1, 3
t _{IH6}	ROMCS1:0 (on RESET)	8		ns	Notes 1, 3
82961KA-16 (16 MHz Specification)					
TBD					

NOTES:

1. See Figure 8 for waveforms and specifications.
2. Signal is synchronous to the CLK2 A edge.
3. Signal is synchronous to the CLK2 A or C edge.
4. Signal is synchronous to any rising or falling edge of CLK2 (CLK2 A, B, C or D edge).
5. Signal is synchronous to the CLK2 B edge.
6. Signal is synchronous to the CLK2 C edge.
7. LAD31:0 are synchronous outputs when presenting data for an internal register read, or any I/O read cycle in which rising $\overline{\text{IOR}}$ precedes rising $\overline{\text{IOCS}}$. LAD15:0 are synchronous outputs for the first half of a packed I/O or DRAM access. For all other accesses, data is driven on LAD31:0 combinatorially, and is described by the t_{MDLD} parameter.
8. MA9:0 signals are synchronous outputs when presenting the DRAM row address when a page miss or a video FIFO read occurs, or when switching from the DRAM row address to the DRAM column address. MA1:0 are synchronous during DRAM burst cycles, and MA7 is synchronous during 16-bit cycles. For all other accesses, MA9:0 are driven combinatorially as described by the t_{LAMA} parameter.
9. MAD31:16 signals are synchronous outputs for all I/O and PROM accesses. For DRAM accesses these signals are driven combinatorially as described by the t_{LDMD} parameter.
10. MD15:0 outputs are synchronous outputs during the second half of a packed I/O or DRAM write access. For all other accesses, data is driven combinatorially as described by the t_{LDMD} parameter.
11. For DRAM write accesses, each byte in the MAD31:16 and MD15:0 bus is enabled only when the corresponding write enable (WE3:0) signal is active. Bytes in this bus which are not selected are floated to avoid contention on the DRAM data bus. At the end of a DRAM access the data bus (MAD31:16, MD15:0) stays valid until the CLK2 A edge of the T_r state, and float when WE3:0 are deasserted at the CLK2 B edge of the T_r state.
- For I/O and ROM accesses, MAD31:16 signals are enabled in the first T_w state of an access synchronous to the CLK2 A edge. After ROM accesses, MAD31:16 are floated in the T_r state, synchronous to the CLK2 A edge. After I/O accesses, the MAD31:29 signals are floated later on the CLK2 C edge, preventing glitches in external decoding logic. Note for I/O, the MAD28:16 signals are also floated on the CLK2 C edge, but only stay valid until the CLK2 A edge of the T_r state.
12. LAD31:0 are synchronous inputs only for internal register writes.
13. MD15:0 are synchronous inputs on the first half of a packed I/O or DRAM read access, any I/O access in which rising $\overline{\text{IOR}}$ precedes rising $\overline{\text{IOCS}}$, auto-poll accesses, and when the video FIFO is being filled.
14. MAD31:16 are synchronous inputs only when the video FIFO is being filled.

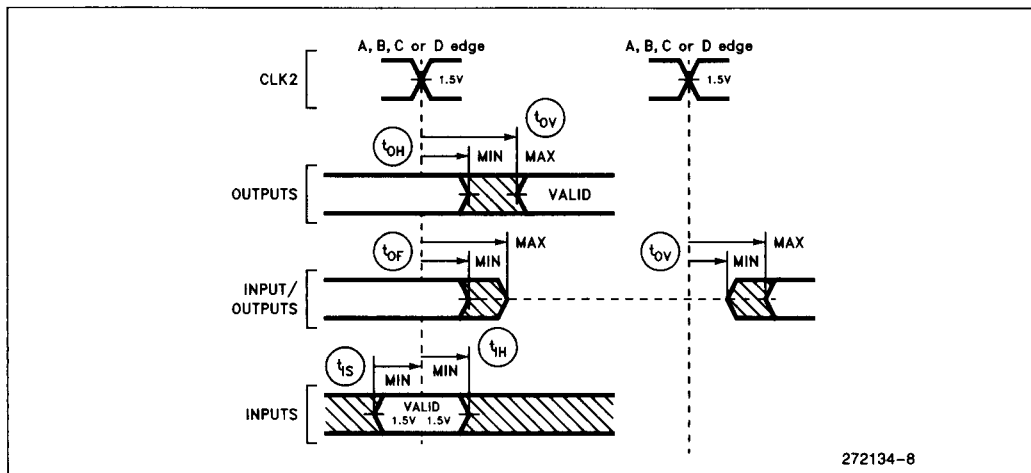


Figure 10. Synchronous Input/Output Waveforms

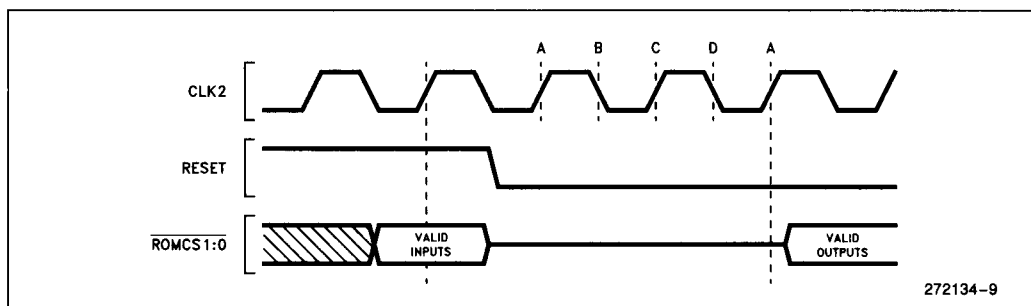


Figure 11. Reset Timing

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7.1 Targeted L-Bus Timing Specifications

Table 17. L-Bus Relative Timing Specifications

Symbol	Parameter/Description	Min	Max	Units	Conditions
82961KA-20 (20 MHz Specification)					
t_{AVLH}	LAD Address Valid to $\overline{ALE}$ High	5		ns	Note 1
t_{LHAX}	LAD Address Hold from $\overline{ALE}$ High	3		ns	Note 1
t_{LLLH}	$\overline{ALE}$ Low to $\overline{ALE}$ High	10		ns	Note 1
t_{ELQD}	$\overline{DEN}$ Low to LAD Data Bus Driven		28	ns	Note 1
t_{EHQF}	$\overline{DEN}$ High to LAD Data Floating		28	ns	Note 1
t_{LAMA}	Local Address to Memory Address		52	ns	Note 1
t_{LDMD}	Local Data to Memory Data	5	22	ns	Note 1
t_{MDLD}	Memory Data to Local Data	5	22	ns	Note 1
t_{RHRL}	RESET High to RESET Low	41		2x Clocks ⁽²⁾	Note 1
82961KA-16 (16 MHz Specification)					
TBD					

NOTES:

1. See Figure 10 for waveforms and specifications.
2. A 2x clock cycle is equal to a CLK2 period, t_c .

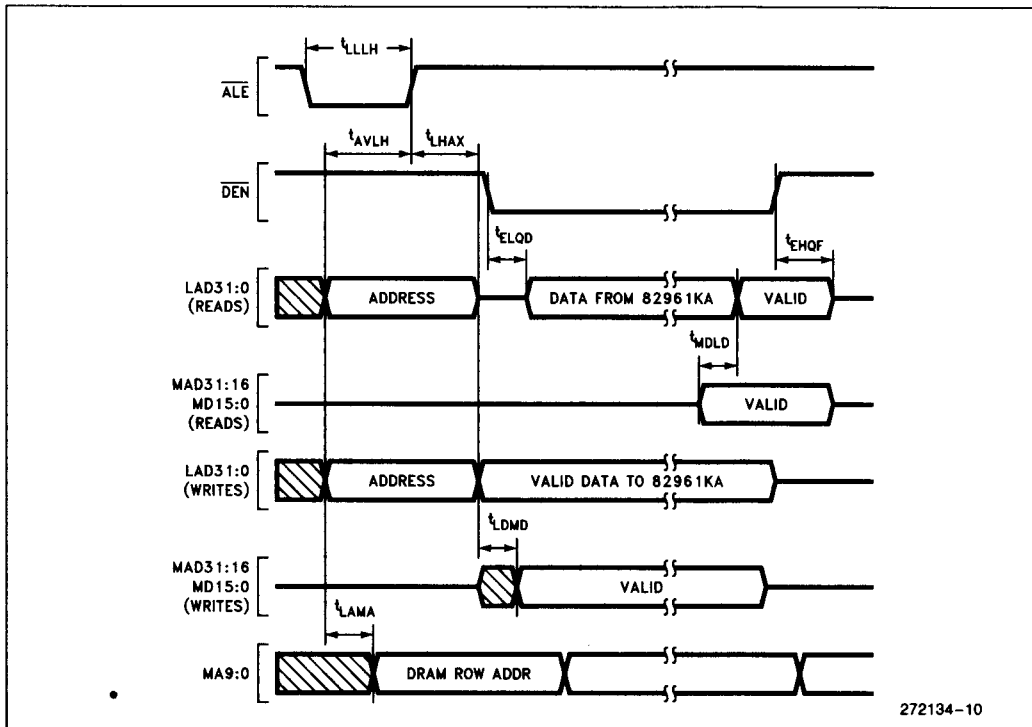


Figure 12. L-Bus Relative Timings

7.2 L-Bus Operational Waveforms

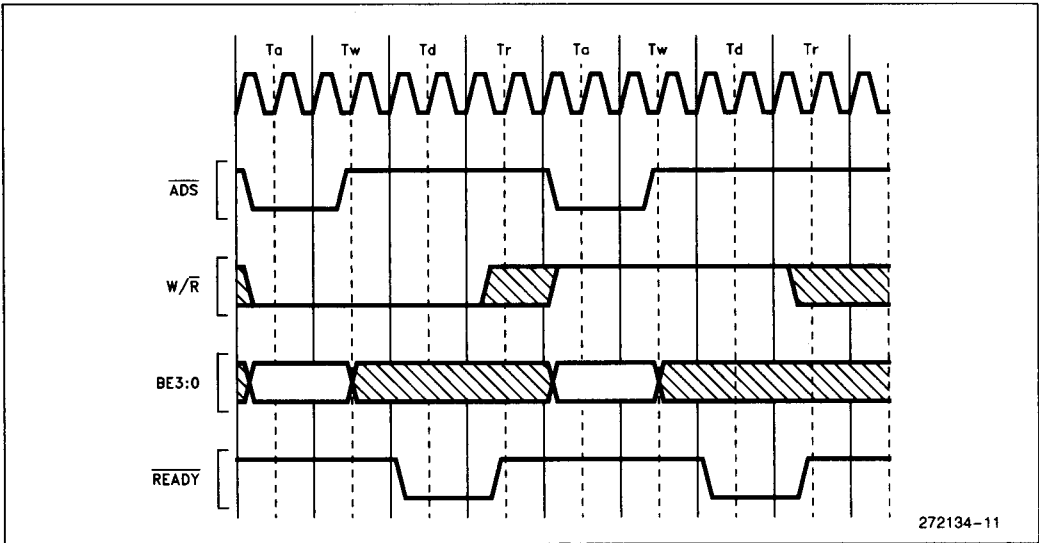


Figure 13. L-Bus Operation

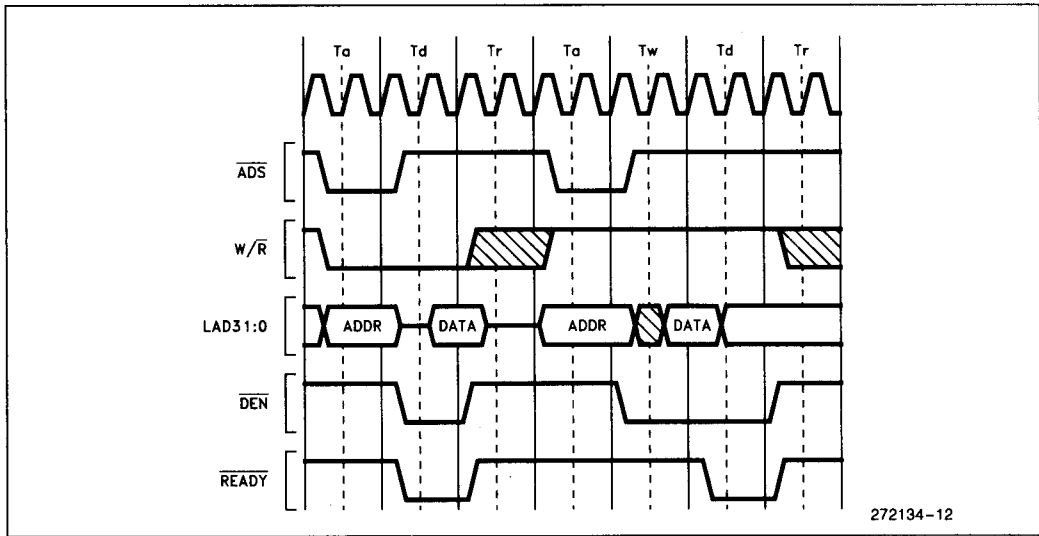


Figure 14. Internal Register Read/Write

7.3 Targeted DRAM Controller Timing Specifications

Table 18. DRAM Controller Relative Timings

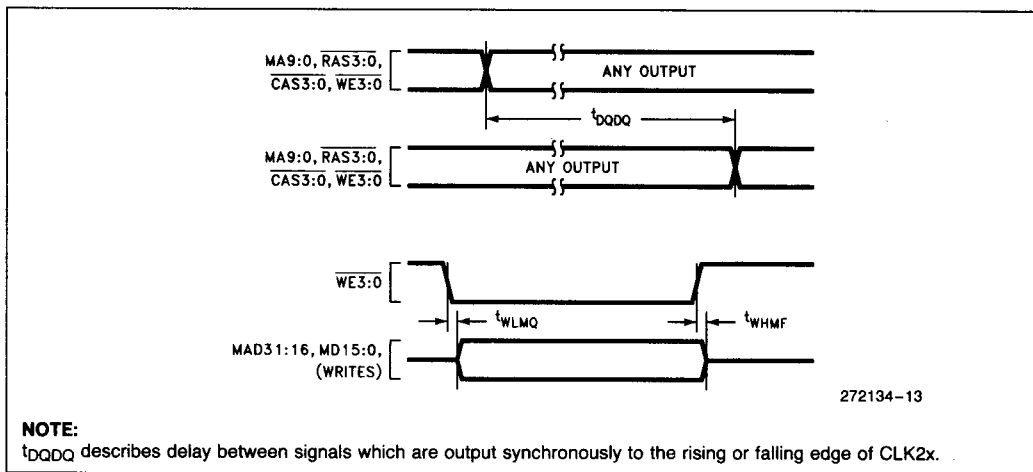
82961KA-20, -16 (20, 16 MHz Specification)					
Symbol	Parameter/Description	Min	Max	Units	Conditions
t_{DQDQ}	Output to Output Delay	$n4x * (t_c/2) \pm 4$		ns	(Notes 1, 2, 3)
t_{WLMQ}	$\overline{WE3:0}$ Low to Memory: data bus enabled	+ 4		ns	(Notes 1, 4)
t_{WHMF}	$\overline{WE3:0}$ High to Memory: data bus float	+ 4		ns	(Notes 1, 4)

NOTES:

- See Figure 15 for waveforms and specifications.
- The t_c parameter refers to the CLK2 period. The value for t_c is given in Table 15. $n4x$ is the number of 4x clock cycles between DRAM outputs. The number of 4x clock cycles is selected by programming the DRAM controller.
- When the value for $n4x$ is an odd number, an error term is required if the CLK2 duty cycle is asymmetric. For example, if CLK2 has a 40%–60% duty cycle, the falling edge varies $\pm 10\%$ from a perfect 50% duty cycle. The error term in this case, which is added to the DRAM timing, is calculated as follows:

$$\text{Error} = \pm (0.10) (t_c)$$

- For non-aligned DRAM writes, each byte in the transfer is enabled and disabled onto the MAD31:16 and MD15:0 data bus by the corresponding $\overline{WE}$. This guarantees no contention between the 82961KA and DRAM for bytes not selected for a particular write cycle.



NOTE:

t_{DQDQ} describes delay between signals which are output synchronously to the rising or falling edge of CLK2x.

Figure 15. DRAM Relative Timings

7.4 DRAM Controller Operational Waveforms

The following bus waveforms describe the operation of the DRAM controller on the 82961KA. The DRAM controller provides registers to configure timings and

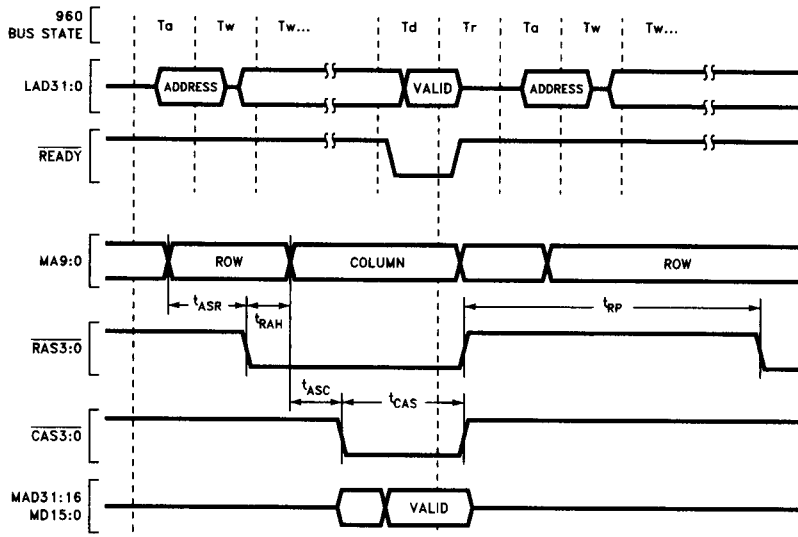
to optimize the DRAM interface to many varieties of DRAM designs (for example, fast-page vs. static column mode DRAMs). The DRAM Operations Waveforms show only the timing parameters which may be adjusted by programming the 82961KA. These parameters are described in Table 19.

Table 19. DRAM Controller Programmable Timings

Symbol	Description	Min	Max	Units
t_{ASR}	Row Address Setup to $\overline{RAS3:0}$ Active	2	15	4x Clocks
t_{RAH}	Row Address Hold after $\overline{RAS3:0}$ Active	2	15	4x Clocks
t_{ASC}	Column Address Setup to $\overline{CAS3:0}$ Active	1	15	4x Clocks
t_{CASrd}	$\overline{CAS3:0}$ Pulse Width for Reads	1	15	4x Clocks
t_{CASwr}	$\overline{CAS3:0}$ Pulse Width for Writes	1	15	4x Clocks
t_{CPrd}	$\overline{CAS3:0}$ Precharge for Reads	0	15	4x Clocks
t_{CPwr}	$\overline{CAS3:0}$ Precharge for Writes	2	15	4x Clocks
t_{RP}	$\overline{RAS3:0}$ Precharge	2	15	4x Clocks
t_{RPC}	$\overline{RAS3:0}$ Hold to $\overline{CAS3:0}$ Precharge (Refresh)	0	7	2x Clocks
t_{CSR}	$\overline{CAS3:0}$ Setup Time (Refresh)	0	7	2x Clocks
t_{CHR}	$\overline{CAS3:0}$ Hold Time (Refresh)	0	7	2x Clocks

NOTE:

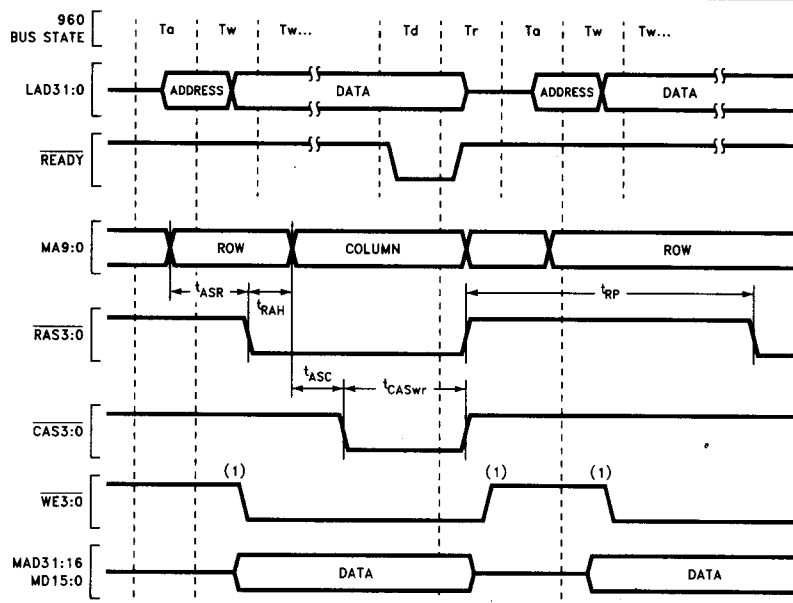
A 4x clock is equal to $0.5 (t_c)$, or half the CLK2 period. A 2x clock is equal to t_c , or the CLK2 period. When the value for $n4x$ is an odd number, an error term is required if the CLK2 duty cycle is asymmetric. For example, if CLK2 has a 40%–60% duty cycle, the falling edge varies $\pm 10\%$ from a perfect 50% duty cycle. The error term in this case, which is added to the DRAM timing, is calculated as follows: Error = $\pm (0.10) (t_c)$.



NOTE:
1. $\overline{WE}3:0 = \text{HIGH}$

272134-14

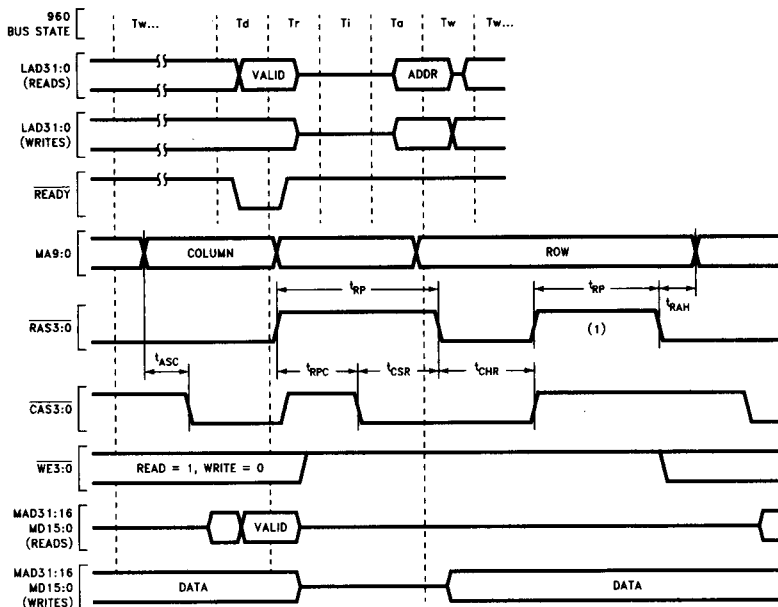
Figure 16. DRAM Non-Page Read Cycle



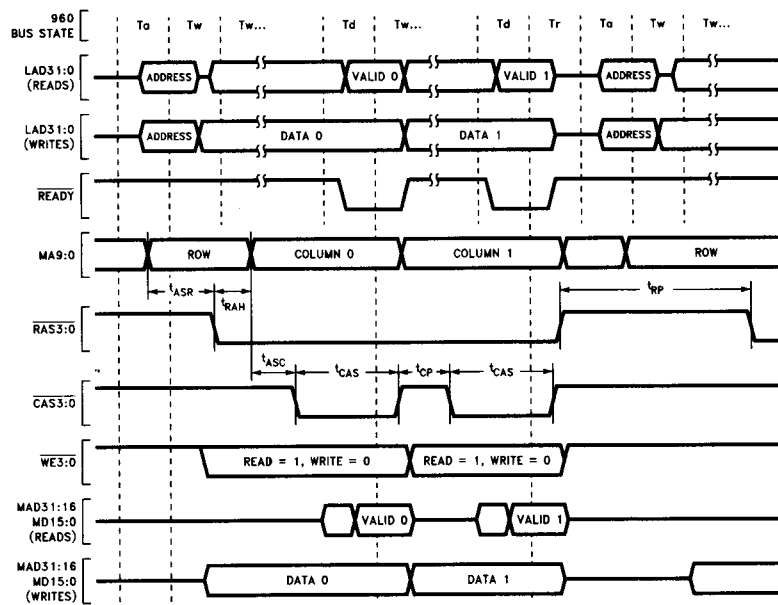
NOTE:
1. $\overline{WE}3:0$ Synchronous to CLK2 B-edge.

272134-15

Figure 17. DRAM Non-Page Write Cycle



272134-16

NOTE:1. Assumes $t_{RP} \geq t_{ASR}$.**Figure 18. DRAM CAS-before-RAS Refresh Cycle**

272134-17

Figure 19. DRAM Page Read/Write

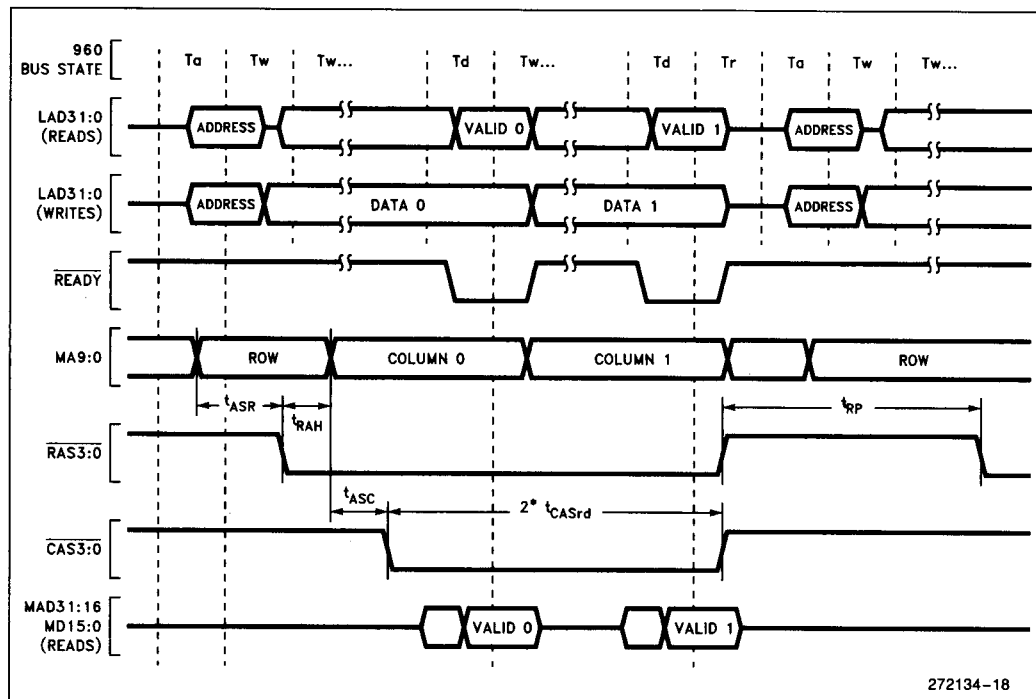
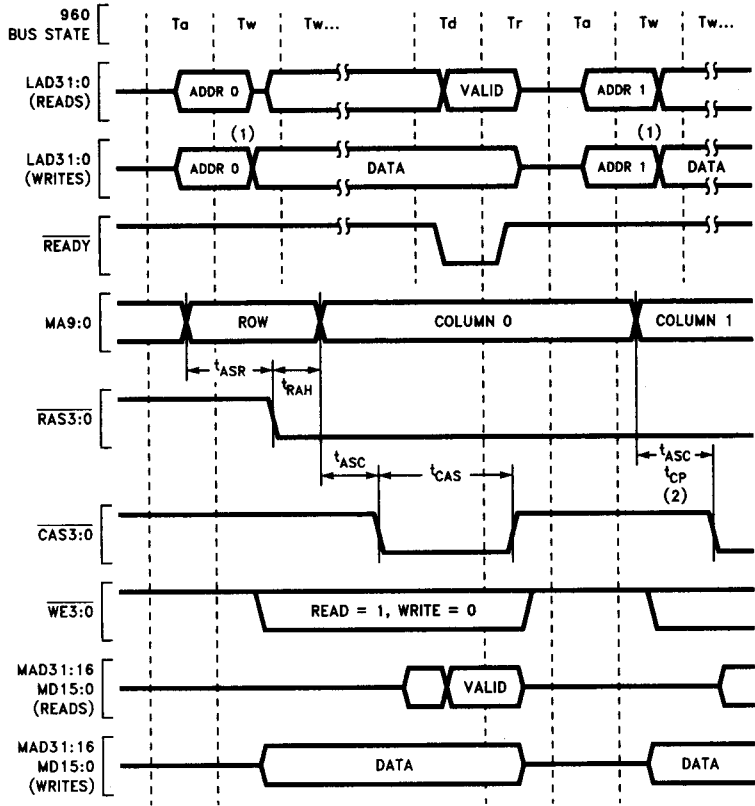


Figure 20. Static Column Mode Read Cycle



272134-19

NOTES:

1. Address 0 and Address 1 are in the same DRAM page.
2. Timing shown is greater of t_{ASC} and t_{CP} .

Figure 21. DRAM Page Hit

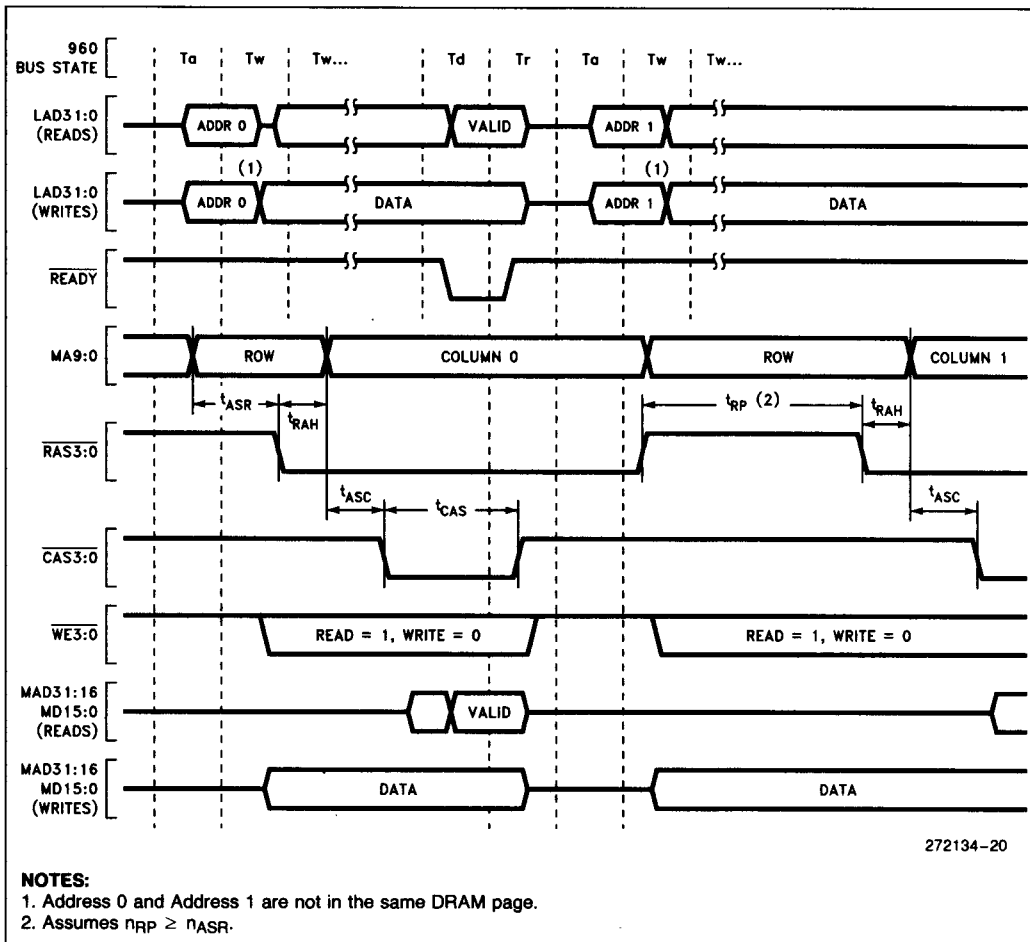
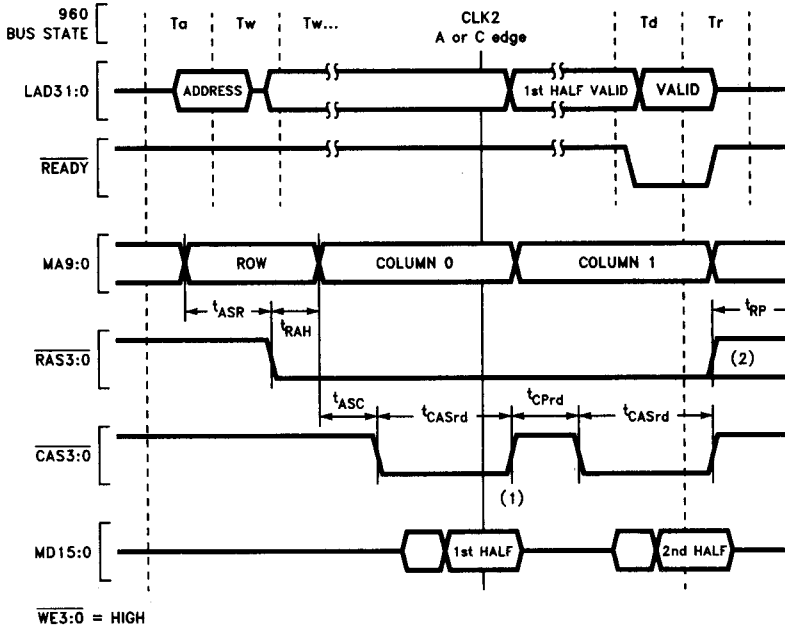


Figure 22. DRAM Page Miss

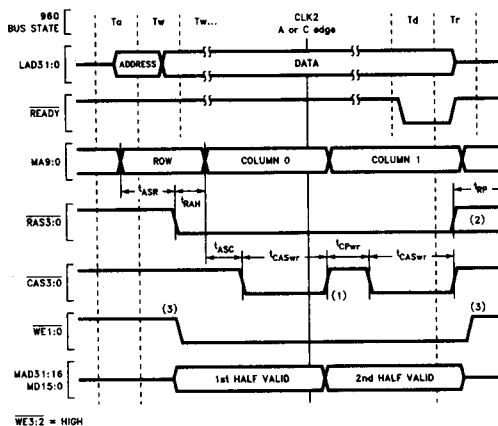


272134-21

NOTES:

1. Rising CAS3:0 synchronous to CLK2 A- or C-edge on 1st half of packed read.
2. RAS3:0 remains active if page cache is enabled.

Figure 23. DRAM 16-Bit Page Mode Read Cycle



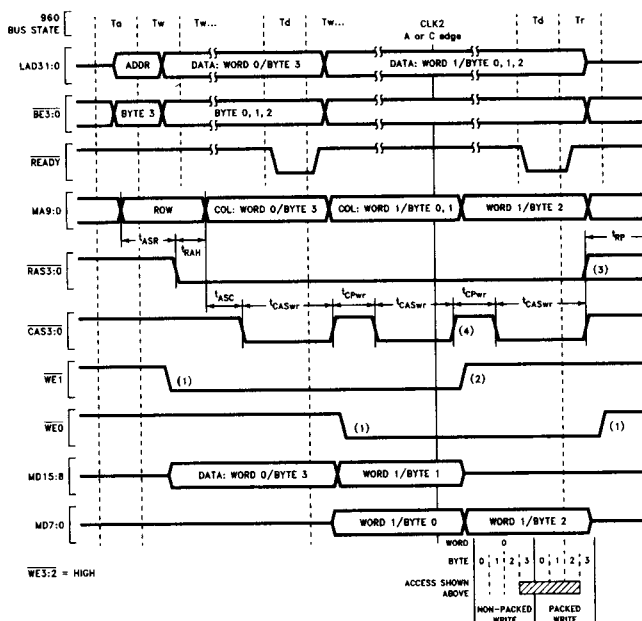
272134-22

NOTES:

1. Rising $\overline{\text{CAS}}3:0$ synchronous to CLK2 A- or C-edge on 1st half of packed write.
2. $\overline{\text{RAS}}3:0$ remains active if page cache is enabled.
3. $\overline{\text{WE}}1:0$ synchronous to CLK2 B-edge.

Figure 24. DRAM Aligned 16-Bit Page Mode Write Cycle

3



272134-23

NOTES:

1. $\overline{\text{WE}}1:0$ synchronous to CLK2 B-edge.
2. $\overline{\text{WE}}1:0$ synchronous to CLK2 B- or D-edge following rising $\overline{\text{CAS}}3:0$.
3. $\overline{\text{RAS}}3:0$ remains active if page cache is enabled.
4. $\overline{\text{CAS}}3:0$ rising edge synchronous to CLK2 A- or C-edge for first half of packed write.

Figure 25. DRAM Non-Aligned 16-Bit Write Cycle

7.5 ROM and I/O Controller Operational Waveforms

The following bus waveforms describe the operation of the ROM and I/O controller on the 82961KA. The ROM and I/O controller provides registers to configure timings and to optimize the ROM and I/O

interface to many varieties of ROM and I/O. The ROM and I/O Operations Waveforms show only the timing parameters which may be adjusted by programming the 82961KA. These parameters are described in Table 20.

Table 20. ROM and I/O Controller Programmable Timings

Symbol	Description	Min Value	Max Value	Min Timing	Max Timing	Units
τ_{ROMRDY}	READY Timing for ROM Accesses	0	15	1	16	1x Clocks
τ_{RDWT}	$\overline{\text{IOR}}\overline{\text{D}}$ Wait High Time	0	31	0	32	1x Clocks
τ_{RDACC}	$\overline{\text{IOR}}\overline{\text{D}}$ Access Low Time	0	31	1	32	1x Clocks
τ_{WRWT}	$\overline{\text{IOWR}}$ Wait High Time	0	31	0	31	1x Clocks
τ_{WRACC}	$\overline{\text{IOWR}}$ Access Low Time	0	31	1	32	1x Clocks
τ_{IOREC}	I/O Recovery Time	0	31	0	31	1x Clocks
τ_{IOCS}	$\overline{\text{IOCS}}$ Low Period	1	31	2	32	1x Clocks

NOTE:

A 1x clock is equal to $2 \cdot (t_{\text{C}})$, or twice the CLK2 period.

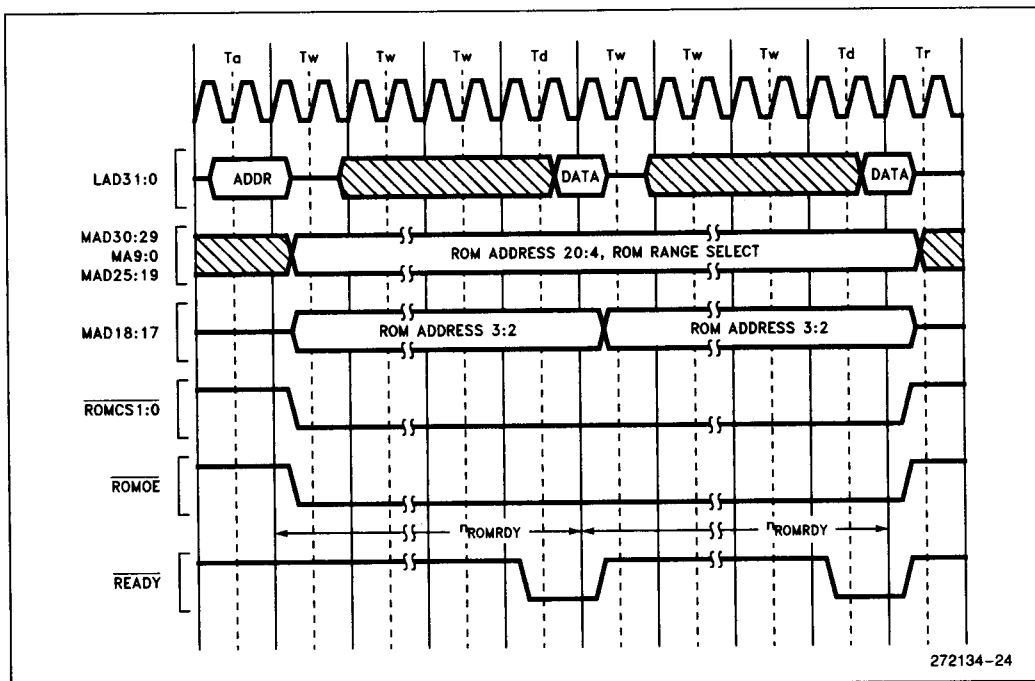


Figure 26. ROM Burst Read

3

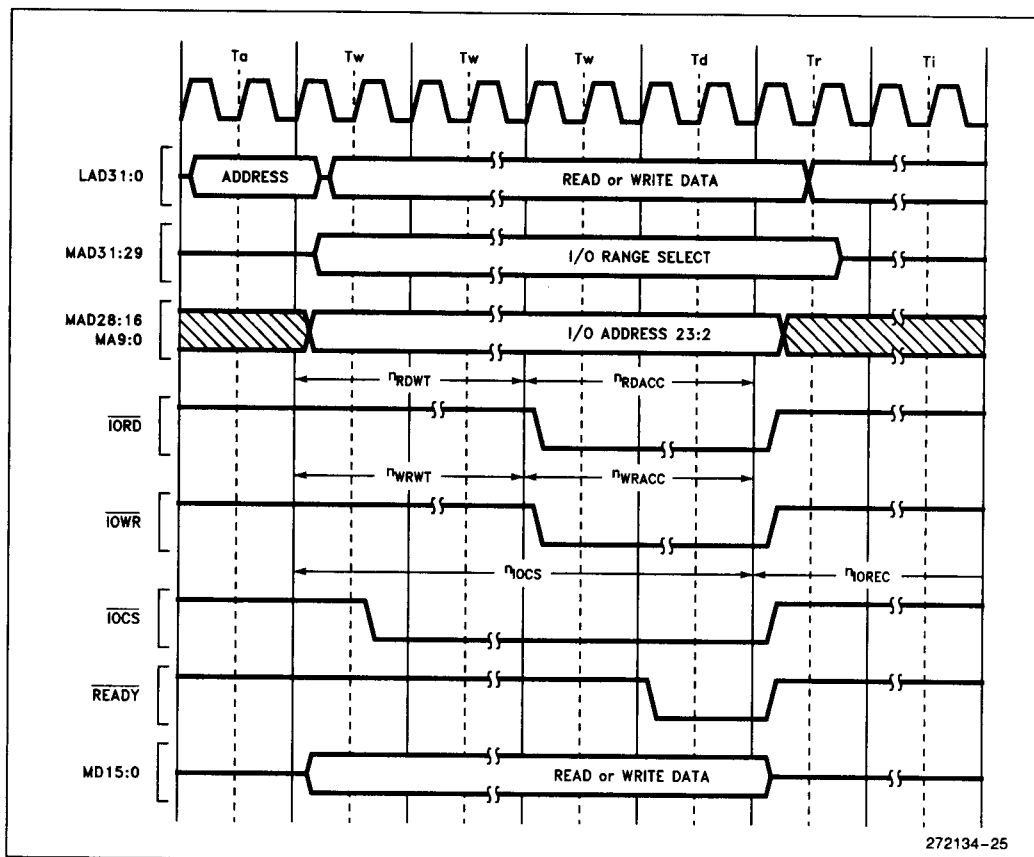


Figure 27. I/O Aligned Read or Write

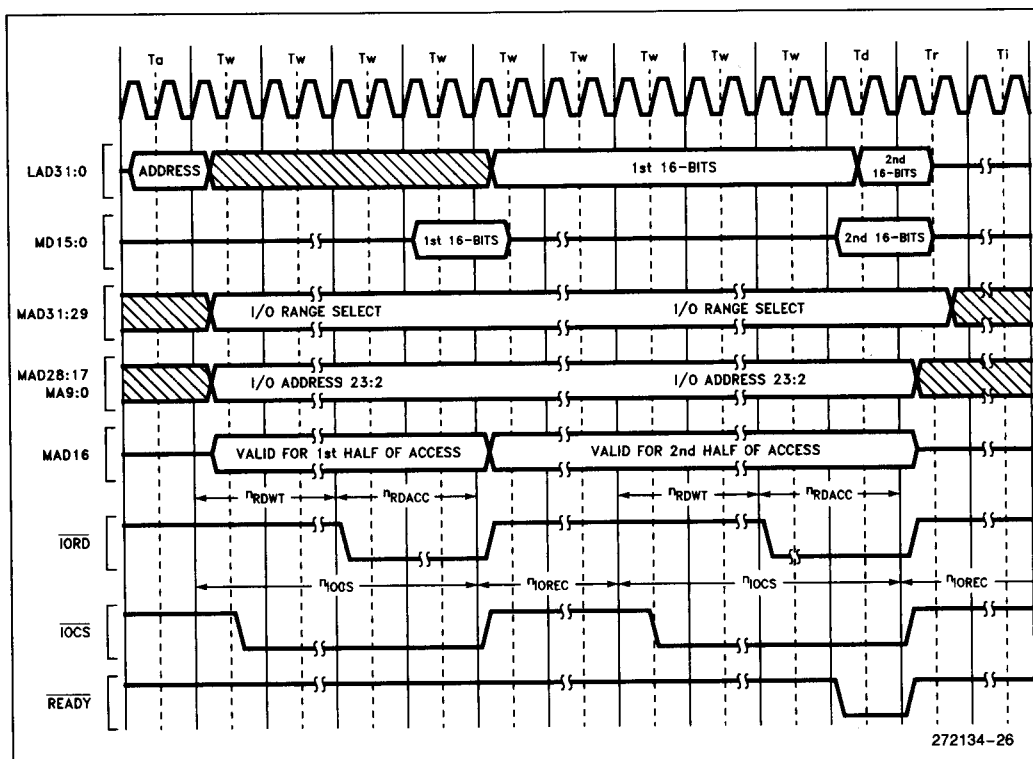


Figure 28. I/O Packed Read

3

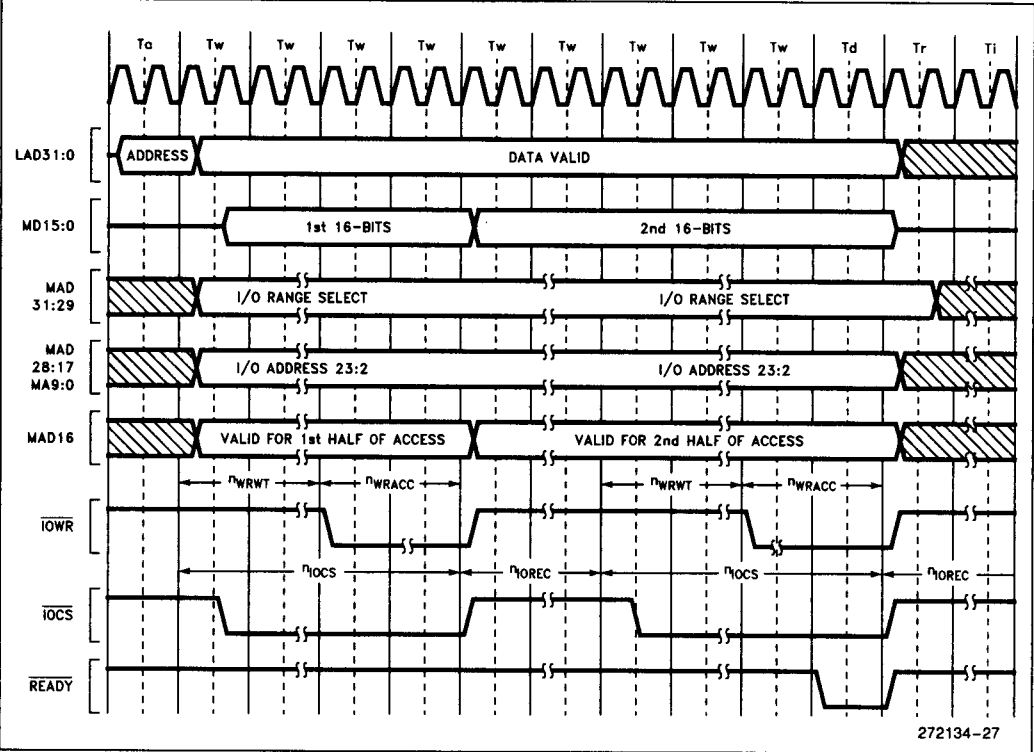


Figure 29. I/O Packed Write

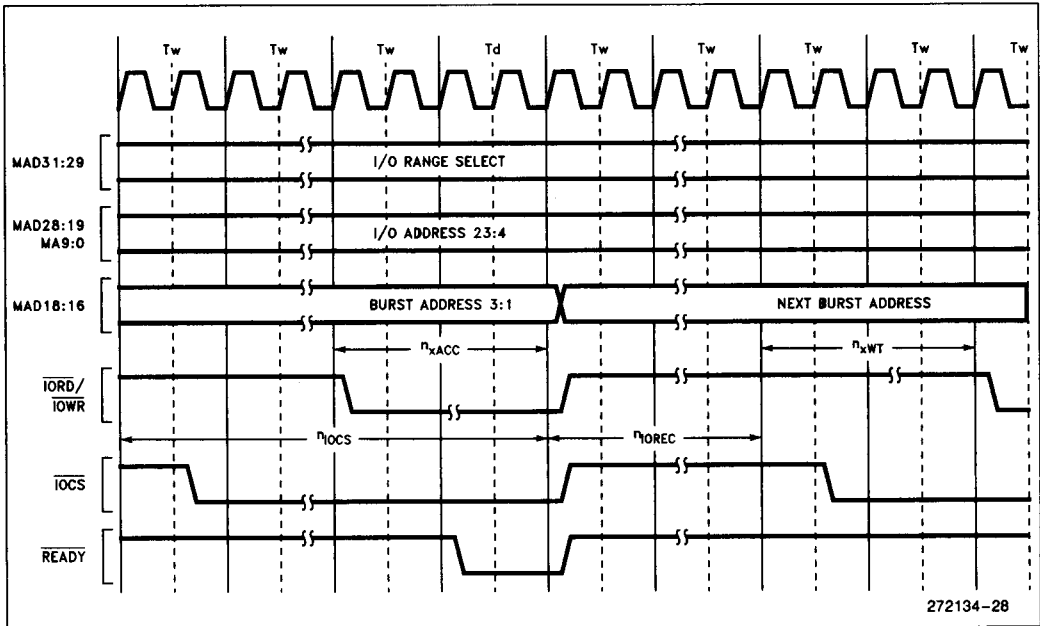


Figure 30. I/O Address Transition in Burst Mode

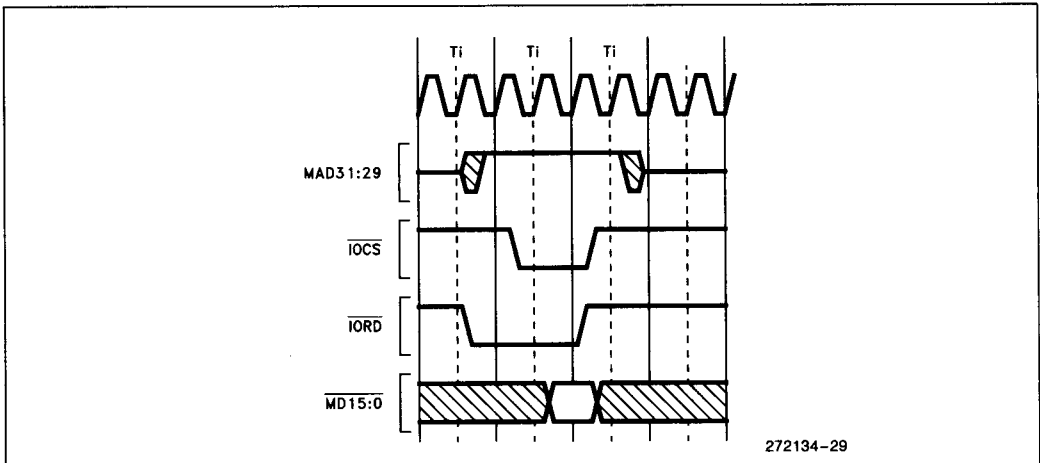


Figure 31. I/O Auto-Poll Cycle

7.6 Targeted Printer Video and Communications Timing Specifications

Table 21. Printer Video Interface Timings

82961KA-20, -16, -10 (20, 16, 10 MHz Specification)					
Symbol	Parameter/Description	Min	Max	Units	Conditions
t _{VC1}	VCLK Frequency, 1x Clock Mode		25	MHz	(Note 1)
t _{VC8}	VCLK Frequency, 8x Clock Mode		66	MHz	(Note 1)
t _{VCH}	VCLK High Time			ns	(Note 1)
t _{VCL}	VCLK Low Time			ns	(Note 1)
t _{OV1}	VIDEO Output Valid, 1x Clock Mode		27	ns	(Note 1)
t _{OV8}	VIDEO Output Valid, 8x Clock Mode		30	ns	(Note 1)
t _{VIS}	LSYNC Input Setup, 1x Clock Mode	0		ns	(Note 1)
t _{VIH}	LSYNC Input Hold, 1x Clock Mode	9		ns	(Note 1)
t _{VW1}	FSYNC Input Pulse Width, 1x Clock Mode	2		t _{VC1}	(Note 1)
t _{VW8}	LSYNC, FSYNC Input Pulse Width, 8x Clock Mode	16		t _{VC8}	(Note 1)

NOTE:

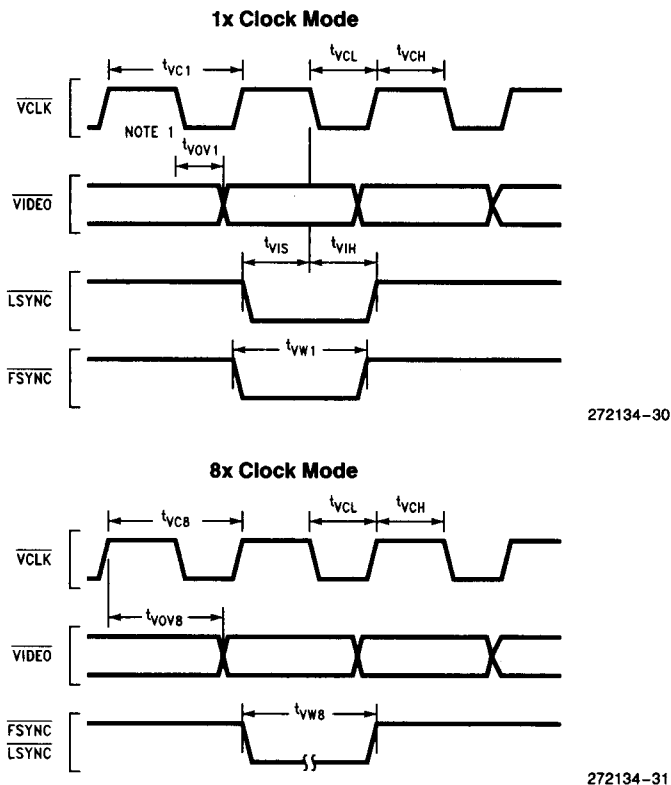
1. See Figure 30 for waveforms and specifications.

Table 22. Printer Communications Interface Timings

Symbol	Parameter/Description	Min	Max	Units	Conditions
82961KA Supplies CCLK					
t _{PV}	CMD Output Valid Delay		4	2x Clocks	(Note 1)
t _{PS}	STS Input Setup	0		ns	(Note 1)
t _{PH}	STS Input Hold	4		2x Clocks	(Note 1)
t _{PSC}	SBSY Valid to CCLK Driven	0	6	2x Clocks	(Note 1)
	Programmable Parameters				
n _{PCK}	CCLK High and Low Time	1	4096	16 2x Clocks	(Notes 1, 2)
CCLK Supplied Externally					
t _{PV}	CMD Output Valid Delay		8	2x Clocks	(Note 1)
t _{PS}	STS Input Setup	0		2x Clocks	(Note 1)
t _{PH}	STS Input Hold	8		2x Clocks	(Note 1)
t _{PC}	CCLK Period	16		2x Clocks	(Note 1)
t _{PCH}	CCLK High Time	8		2x Clocks	(Note 1)
t _{PCL}	CCLK Low Time	8		2x Clocks	(Note 1)
t _{PCS}	SBSY Setup to CCLK Valid	0		2x Clocks	(Note 1)
	Programmable Parameters				
n _{PF}	CMD and CBSY Float Time	1	4096	16 2x Clocks	(Notes 1, 2)

NOTES:

- See Figures 31 and 32 for waveforms and specifications.
- n_{PCK} and n_{PF} are programmed through the CCLK divisor register; parameter is programmed in (n*16) 2x clocks.

**NOTE:**

1. t_{VPV1} is referenced to the edge of $\overline{VCLK}$ that is programmed for video data output.

Figure 32. Printer Video Interface Timing

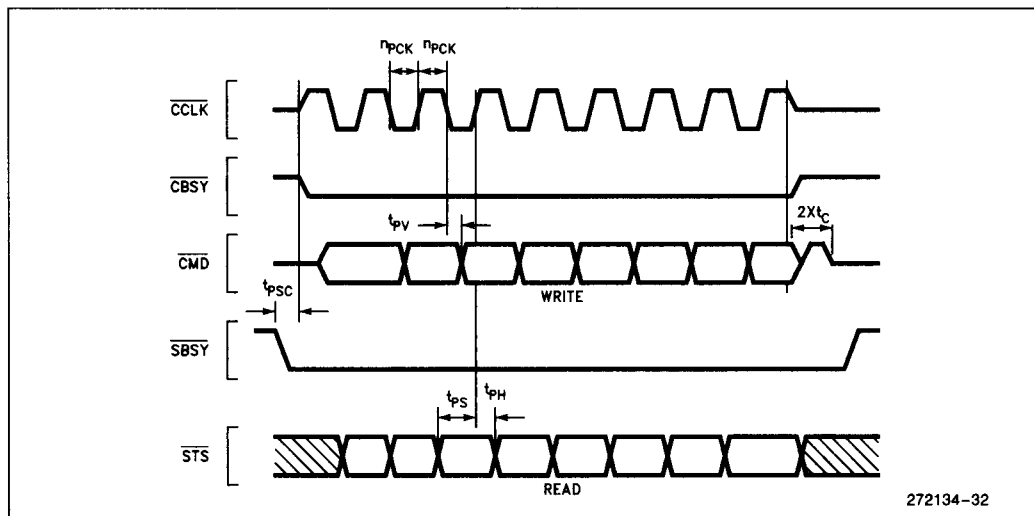


Figure 33. Printer Communications Interface Timing (82961KA Supplies CCLK)

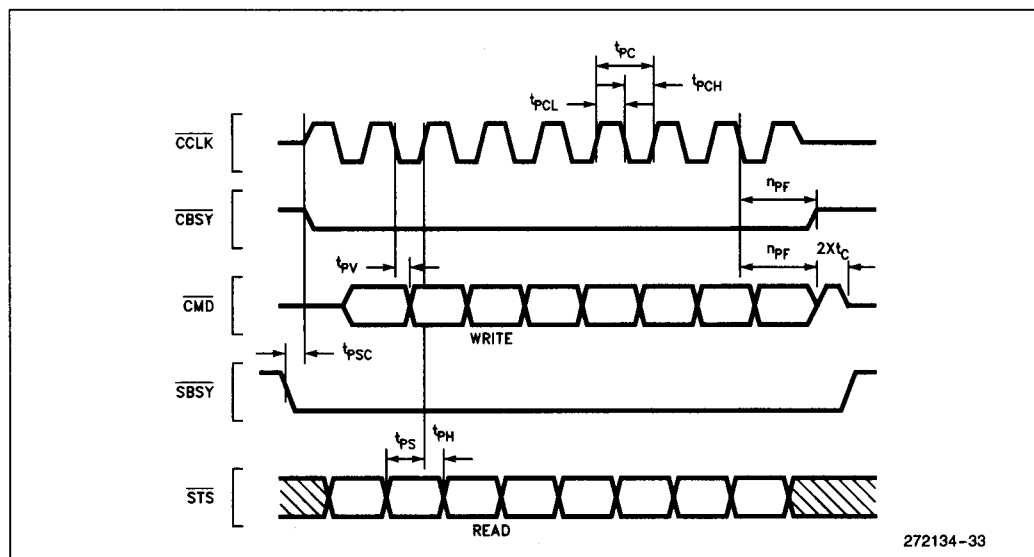


Figure 34. Printer Communications Interface Timing (CCLK Supplied Externally)