

2N5196-2N5199

Dual N-Channel JFET

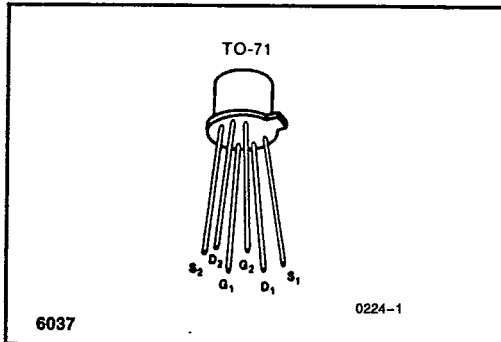
General Purpose Amplifier



T-29-27

2N5196-2N5199

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted)
 Gate-Source or Gate-Drain Voltage (Note 1) -50V
 Gate Current (Note 1) 50mA
 Storage Temperature Range -65°C to $+200^\circ\text{C}$
 Operating Temperature Range -55°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10sec) $+300^\circ\text{C}$

	One Side	Both Sides
Power Dissipation ($T_A = 85^\circ\text{C}$) ...	250mW	500mW
Derating	2.6mW/ $^\circ\text{C}$	4.3mW/ $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

TO-71
2N5196
2N5197
2N5198
2N5199

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{GSS}	Gate Reverse Current	$V_{GS} = -30V, V_{DS} = 0$		-25	pA
		$T_A = 150^\circ\text{C}$		-50	nA
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0$	-50		V
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 20V, I_D = 1\text{nA}$	-0.7	-4	
V_{GS}	Gate-Source Voltage	$V_{DG} = 20V, I_D = 200\mu\text{A}$	-0.2	-3.8	
I_G	Gate Operating Current			-15	pA
		$T_A = 125^\circ\text{C}$		-15	nA
I_{DSS}	Saturation Drain Current (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	0.7	7	mA
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DS} = 20V, V_{GS} = 0$	1000	4000	μS
g_{fs}	Common-Source Forward Transconductance (Note 2)	$V_{DG} = 20V, I_D = 200\mu\text{A}$			
g_{os}	Common-Source Output Conductance (Note 2)	$V_{DS} = 20V, V_{GS} = 0$		50	
g_{os}	Common-Source Output Conductance (Note 2)	$V_{DG} = 20V, I_D = 200\mu\text{A}$		4	
C_{iss}	Common-Source Input Capacitance (Note 4)	$V_{DS} = 20V, V_{GS} = 0$	f = 1MHz	6	
C_{rss}	Common-Source Reverse Transfer Capacitance (Note 4)				2
NF	Spot Noise Figure (Note 4)		f = 100Hz, $R_G = 10M\Omega$	0.5	dB
\bar{e}_n	Equivalent Input Noise Voltage (Note 4)		f = 1kHz	20	$\frac{\text{nV}}{\sqrt{\text{Hz}}}$

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NOTE: All typical values have been characterized but are not tested.

2N5196-2N5199

2N5196-2N5199

INTERMIL

T-29-27

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	2N5196		2N5197		2N5198		2N5199		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I _{G1} -I _{G2}	Differential Gate Current	V _{DG} = 20V, I _D = 200μA T _A = 125°C		5		5		5		5	nA
I _{DSS1} /I _{DSS2}	Saturation Drain Current Ratio (Note 2)	V _{DS} = 20V, V _{GS} = 0V	0.95	1	0.95	1	0.95	1	0.95	1	
g _{fs1} /g _{fs2}	Transconductance Ratio (Note 2)	f = 1kHz	0.97	1	0.97	1	0.95	1	0.95	1	
V _{GS1} -V _{GS2}	Differential Gate-Source Voltage			5		5		10		15	mV
Δ V _{GS1} =V _{GS2} ΔT	Gate-Source Differential Voltage Change with Temperature (Note 3)	V _{DG} = 20V, I _D = 200μA T _A = 25°C T _B = 125°C		5		10		20		40	μV/°C
		T _A = -55°C T _B = 25°C		5		10		20		40	
g _{os1} -g _{os2}	Differential Output Conductance	f = 1kHz		1		1		1		1	μS

- NOTES: 1. Per transistor.
 2. Pulse test required, pulsewidth = 300μs, duty cycle < 3%.
 3. Measured at endpoints T_A and T_B.
 4. For design reference only, not 100% tested.

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