

*SpeedPlus™* **14-Bit, 65MHz Sampling  
 ANALOG-TO-DIGITAL CONVERTER**

**FEATURES**

- **HIGH DYNAMIC RANGE:**  
 High SFDR: 100dB at 20MHz  $f_{IN}$   
 High SNR: 75dB at 20MHz  $f_{IN}$
- **PREMIUM TRACK/HOLD:**  
 High Bandwidth: 1GHz  
 Low Jitter: 0.25pS rms  
 Differential or Single-Ended Inputs  
 Selectable Full-Scale Input Range

- **FLEXIBLE CLOCKING:**  
 Differential or Single-Ended  
 Accepts Sine or Square Wave Clocking  
 Down to 0.5Vp-p  
 Variable Threshold Level

**APPLICATIONS**

- **BASESTATION WIDEBAND RADIOS:**  
 CDMA, GSM, TDMA, 3G, AMPS, NMT
- **TEST INSTRUMENTATION**
- **CCD IMAGING**

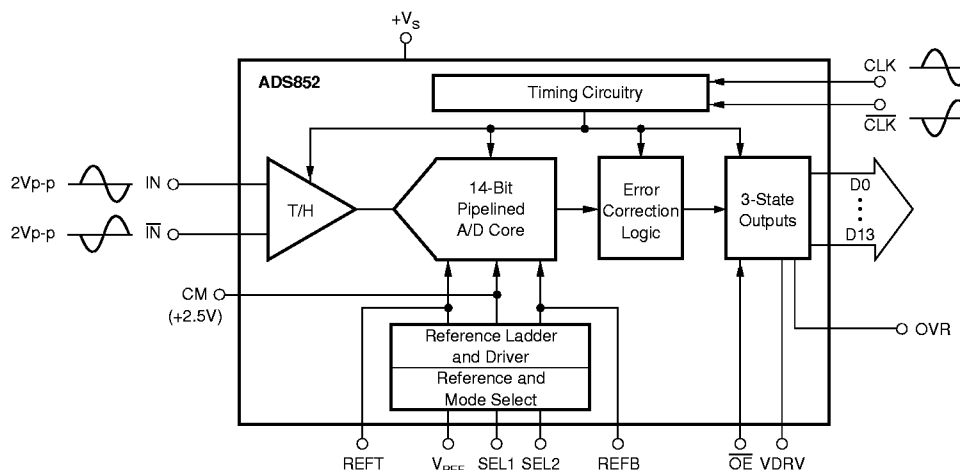
**DESCRIPTION**

The ADS852 is a high-dynamic range 14-bit, 65MHz pipelined analog-to-digital converter. It includes a high-bandwidth linear track/hold that gives excellent spurious performance up to and beyond the Nyquist rate. This high-bandwidth track/hold also has a low jitter of only 0.25pS rms, leading to excellent SNR performance. The clock input can accept a low level differential sine wave or square wave signal down to 0.5Vp-p, further improving the SNR performance. It also accepts a single-ended clock signal and has flexible threshold levels.

The ADS852 has a 4Vp-p differential input range (2Vp-p x 2 inputs, +16dBm) for optimum signal-to-noise ratio. The

differential operation gives the lowest even-order harmonic components. A lower input voltage of 3Vp-p or 2Vp-p can also be selected using the internal references, further optimizing SFDR. Alternatively, a single-ended input range can be used by tying the IN input to the common-mode voltage if desired.

The ADS852 also provides an over-range flag that indicates when the input signal has exceeded the converter's full-scale range. This flag can also be used to reduce the gain of the front end signal conditioning circuitry. It also employs digital error correction techniques to provide excellent differential linearity for demanding imaging applications. The ADS852 is available in a small 48-lead TQFP package.



# SPECIFICATIONS

At  $T_A$  = full specified temperature range, differential input range = 1.5V to 3.5V, sampling rate = 65MHz, and external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS852Y			UNITS
		MIN	TYP	MAX	
<b>RESOLUTION</b>			14 Guaranteed		Bits
<b>SPECIFIED TEMPERATURE RANGE</b>	Ambient Air	-40 to +85			°C
<b>ANALOG INPUT</b>					
Standard Differential Input Range	(2Vp-p x 2, +16dBm)	1.5		3.5	V
Optional Single-Ended Input Range	4Vp-p	0.5		4.5	V
Common-Mode Voltage			2.5		V
Optional Input Ranges	Selectable	2Vp-p (+10dBm) or 3Vp-p (+13dBm)			V
Analog Input Bias Current			1		μA
Track-Mode Input Bandwidth	-3dBFS		1		GHz
Input Impedance			1.25    9		MΩ    pF
<b>CONVERSION CHARACTERISTICS</b>					
Sample Rate		1M		65M	Samples/s
Data Latency			7		Clk Cyc
<b>DYNAMIC CHARACTERISTICS</b>					
Differential Linearity Error (largest code error)			±0.5	±1.0	LSB
f = 2.2MHz			±0.5		LSB
f = 20MHz			Guaranteed		
No Missing Codes			±0.5	±2.0	LSBs
Integral Nonlinearity Error, f = 1MHz					
Spurious Free Dynamic Range <sup>(1)</sup>					
f = 2.2MHz			105		dBFS <sup>(2)</sup>
f = 20MHz			100		dBFS
f = 31MHz			100		dBFS
Two-Tone Intermodulation Distortion <sup>(3)</sup>					
f = 4.5MHz and 5.5MHz (-7dB each tone)			-95		dBc
Signal-to-Noise Ratio (SNR)					
f = 2.2MHz			75		dBFS
f = 20MHz			75		dBFS
f = 31MHz			75		dBFS
Signal-to-(Noise + Distortion) (SINAD)					
f = 2.2MHz			75		dB
f = 20MHz			75		dB
f = 31MHz			74		dBFS
Output Noise	Input Grounded		TBD		LSBs rms
Aperture Delay Time			3		ns
Aperture Jitter			0.25		ps rms
Overvoltage Recovery Time			2		ns
Full-Scale Step Acquisition Time			5		ns
<b>DIGITAL INPUTS</b>					
Convert Command (Start Conversion)	Rising Edge of Convert Clock	+0.5		+V <sub>S</sub>	Vp-p
Logic Family (Other Clock Inputs)		+3V/+5V Logic Compatible CMOS			
High Level Input Current <sup>(4)</sup> (V <sub>IN</sub> = 5V)				100	μA
Low Level Input Current (V <sub>IN</sub> = 0V)				10	μA
High Level Input Voltage		+2.0			V
Low Level Input Voltage				+1.0	V
Input Capacitance			5		pF
<b>DIGITAL OUTPUTS</b>					
Logic Family		+3V/+5V Logic Compatible CMOS			
Logic Coding		Straight Offset Binary			
Low Output Voltage (I <sub>OL</sub> = 50μA to 1.6mA)	VDRV = 3V			+0.2	V
High Output Voltage, (I <sub>OH</sub> = 50μA to 0.5mA)		+2.5			V
Low Output Voltage, (I <sub>OL</sub> = 50μA to 1.6mA)	VDRV = 5V			+0.2	V
High Output Voltage, (I <sub>OH</sub> = 50μA to 1.6mA)		+2.5			V
3-State Enable Time	$\overline{OE} = L$		20	40	ns
3-State Disable Time	$\overline{OE} = H$		2	10	ns
Output Capacitance			5		pF
<b>ACCURACY (Internal Reference, = 2V, Unless Otherwise Noted)</b>					
Zero Error (Referred to -FS)	at 25°C		0.5	3.0	%FS
Zero Error Drift (Referred to -FS)			12		ppm/°C
Gain Error <sup>(5)</sup>	at 25°C		±1.5	±2.5	%FS
Gain Error Drift <sup>(5)</sup>			38		ppm/°C
Gain Error <sup>(6)</sup>	at 25°C		±0.75	±1.5	%FS
Gain Error Drift <sup>(6)</sup>			20		ppm/°C
Power Supply Rejection of Gain	ΔV <sub>S</sub> = ±5%		68		dB
Internal REF Tolerance	Deviation from Ideal		±10	±50	mV
External REF Voltage Range		0.9	2	2.025	V
Reference Input Resistance			1.0		kΩ

# SPECIFICATIONS (CONT)

At  $T_A$  = full specified temperature range, differential input range = 1.5V to 3.5V, sampling rate = 65MHz, and external reference, unless otherwise noted.

PARAMETER	CONDITIONS	ADS852Y			UNITS
		MIN	TYP	MAX	
<b>POWER SUPPLY REQUIREMENTS</b> Supply Voltage: $+V_S$ Supply Current: $+I_S$ Output Driver Supply Current (VDRV) Power Dissipation: VDRV = 5V VDRV = 3V Power Down Thermal Resistance, $\theta_{JA}$ 48-Lead TQFP	Operating	+4.75	+5.0	+5.25	V
	Operating		120		mA
			12		mA
			670	740	mW
			650	720	mW
		Operating		20	mW
					$^{\circ}\text{C}/\text{W}$

NOTES: (1) Spurious Free Dynamic Range refers to the magnitude of the largest harmonic. (2) dBFS means dB relative to Full Scale. (3) Two-tone intermodulation distortion is referred to the largest fundamental tone. This number will be 6dB higher if it is referred to the magnitude of the two-tone fundamental envelope. (4) A 50k $\Omega$  pull-down resistor is inserted internally. (5) Includes internal reference. (6) Excludes internal reference.

## ABSOLUTE MAXIMUM RATINGS

$+V_S$ .....	+6V
Analog Input .....	(-0.3V) to ( $+V_S + 0.3V$ )
Logic Input .....	(-0.3V) to ( $+V_S + 0.3V$ )
Case Temperature .....	+100 $^{\circ}\text{C}$
Junction Temperature .....	+150 $^{\circ}\text{C}$
Storage Temperature .....	+150 $^{\circ}\text{C}$

## PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE
ADS852Y	48-Lead TQFP	xxx	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

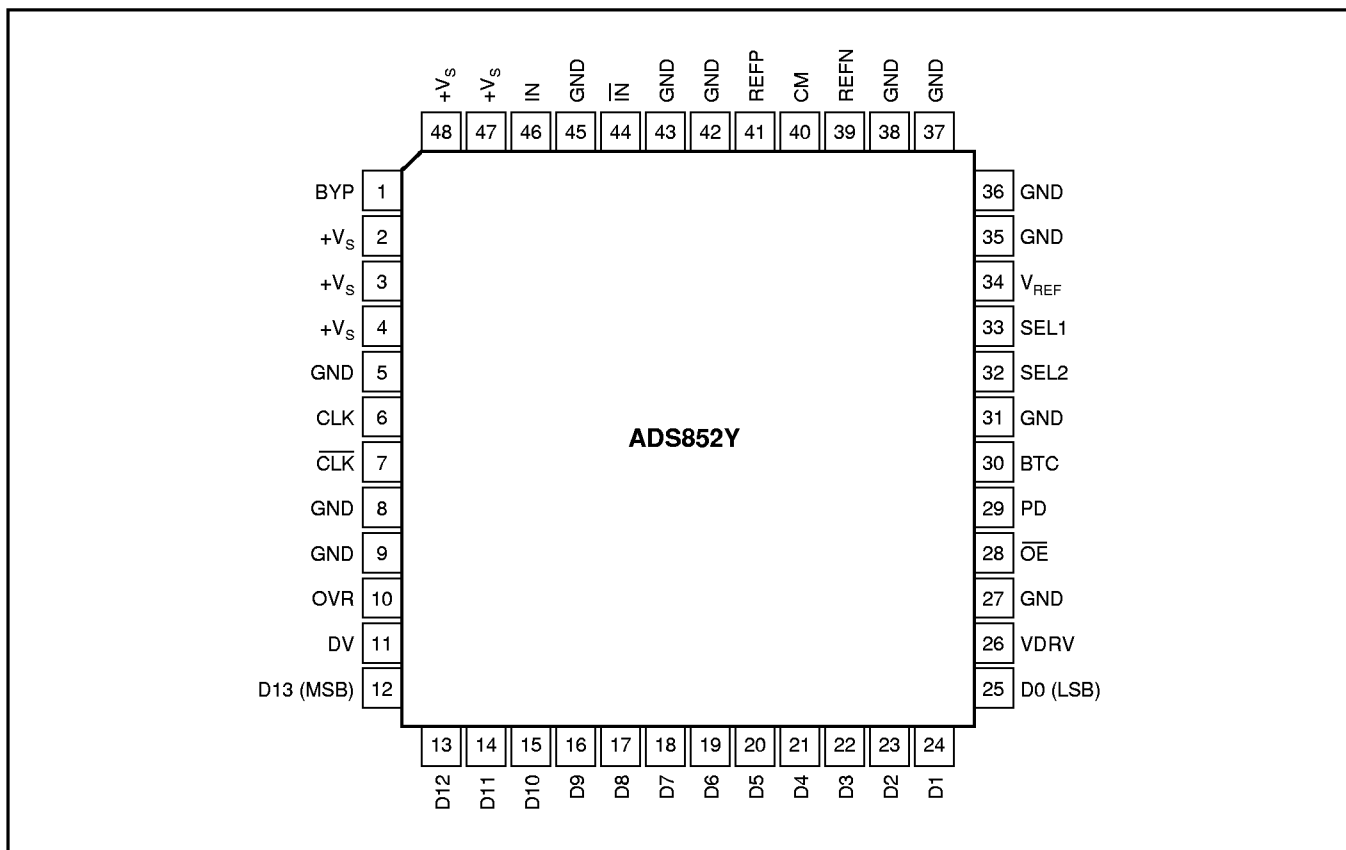
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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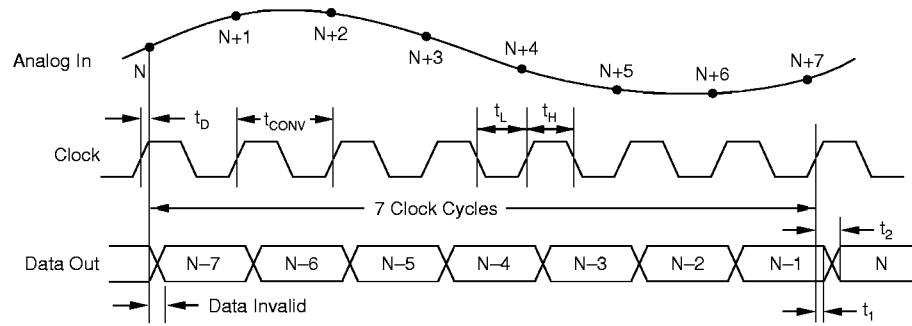
## PIN DESCRIPTIONS

PIN	I/O	DESIGNATOR	DESCRIPTION	PIN	I/O	DESIGNATOR	DESCRIPTION
1		BYP	Bypass Point	26		VDRV	Output Bit Driver Voltage Supply
2		+V <sub>S</sub>	Supply Voltage	27		GND	Ground
3		+V <sub>S</sub>	Supply Voltage	28		OE	Output Enable: HI = High Impedance; LO or Floating: Normal Operation
4		+V <sub>S</sub>	Supply Voltage				Power Down: HI = Power Down; LO = Normal
5		GND	Ground	29	I	PD	HI = Binary Two's Complement; LO = Straight Binary
6	I	CLK	Clock Input	30	I	BTC	Ground
7	I	CLK	Complementary Clock Input	31		GND	Reference Select 2: See Table
8		GND	Ground	32		SEL2	Reference Select 1: See Table
9		GND	Ground	33		SEL1	Internal Reference Voltage
10	O	OVR	Overrange Indicator	34		V <sub>REF</sub>	Ground
11	O	DV	Data Valid Pulse: HI = Data Valid	35		GND	Ground
12	O	D13	Most Significant Bit (MSB)	36		GND	Ground
13	O	D12	Data Bit 12	37		GND	Ground
14	O	D11	Data Bit 11	38		GND	Ground
15	O	D10	Data Bit 10	39		REFN	Bottom Reference Voltage Bypass
16	O	D9	Data Bit 9	40		CM	Common-Mode Voltage (mid-scale)
17	O	D8	Data Bit 8	41		REFP	Top Reference Voltage Bypass
18	O	D7	Data Bit 7	42		GND	Ground
19	O	D6	Data Bit 6	43		GND	Ground
20	O	D5	Data Bit 5	44	I	IN	Complementary Analog Input
21	O	D4	Data Bit 4	45		GND	Ground
22	O	D3	Data Bit 3	46	I	IN	Analog Input
23	O	D2	Data Bit 2	47		+V <sub>S</sub>	Supply Voltage
24	O	D1	Data Bit 1	48		+V <sub>S</sub>	Supply Voltage
25	O	D0	Least Significant Bit (LSB)				

## PIN DIAGRAM



## TIMING DIAGRAM



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{CONV}$	Convert Clock Period	15.4		1 $\mu$ s	ns
$t_L$	Clock Pulse Low	7.6	$t_{CONV}/2$		ns
$t_H$	Clock Pulse High	7.6	$t_{CONV}/2$		ns
$t_D$	Aperture Delay		3		ns
$t_1$	Data Hold Time, $C_L = 0pF$	3.9			ns
$t_2$	New Data Delay Time, $C_L = 15pF$ max			12	ns

## TABLE, REFERENCE/FULL SCALE RANGE SELECT

DESIRED FULL SCALE RANGE	SEL1	SEL2	INTERNAL $V_{REF}$
4Vp-p (2Vp-p x 2, +16dBm)	GND	GND	2V
3Vp-p (1.5Vp-p x 2, +13dBm)	GND	+ $V_S$	1.5V
2Vp-p (1Vp-p x 2, +10dBm)	$V_{REF}$	GND	1V

For External Reference Operation, tie  $V_{REF}$  to  $+V_S$ , the full scale range will be 2X the reference value. For instance, selecting a 2V External Reference will set the full scale values of 1.5V to 3.5V for both IN and  $\overline{IN}$  inputs.