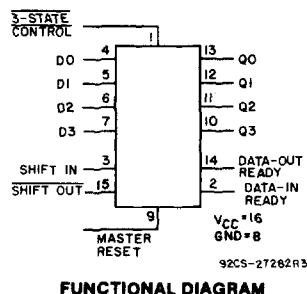


CD54/74HC40105

CD54/74HCT40105

High-Speed CMOS Logic



4-Bit x 16-Word FIFO Register

Type Features:

- Independent asynchronous inputs and outputs
- Expandable in either direction
- Reset capability
- Status indicators on inputs and outputs
- 3-state outputs
- Shift-out independent of 3-state control

Applications:

- Bit-rate smoothing
- CPU/terminal buffering
- Data communications
- Peripheral buffering
- Line printer input buffers
- Auto-dialers
- CRT buffer memories
- Radar data acquisition

The RCA-CD54/74HC40105 and CD54/74HCT40105 are high-speed silicon-gate CMOS devices that are compatible, except for "shift-out" circuitry, with the RCA-CD40105B. They are low-power first-in-first-out (FIFO) "elastic" storage registers that can store 16 four-bit words. The 40105 is capable of handling input and output data at different shifting rates. This feature makes it particularly useful as a buffer between asynchronous systems.

Each word position in the register is clocked by a control flip-flop, which stores a marker bit. A "1" signifies that the position's data is filled and a "0" denotes a vacancy in that position. The control flip-flop detects the state of the preceding flip-flop and communicates its own status to the succeeding flip-flop. When a control flip-flop is in the "0" state and sees a "1" in the preceding flip-flop, it generates a clock pulse that transfers data from the preceding four data latches into its own four data latches and resets the preceding flip-flop to "0". The first and last control flip-flops have buffered outputs. Since all empty locations "bubble" automatically to the input end, and all valid data ripple through to the output end, the status of the first control flip-flop (DATA-IN READY) indicates if the FIFO is full, and the status of the last flip-flop (DATA-OUT READY) indicates if the FIFO contains data. As the earliest data are removed from the bottom of the data stack (the output end), all data entered later will automatically propagate (ripple) toward the output.

Loading Data

Data can be entered whenever the DATA-IN READY (DIR) flag is high, by a low to high transition on the SHIFT-IN (SI) input. This input must go low momentarily before the next word is accepted by the FIFO. The DIR flag will go low momentarily, until the data have been transferred to the second location. The flag will remain low when all 16-word locations are filled with valid data, and further pulses on the SI input will be ignored until DIR goes high.

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ,
@ $V_{CC} = 5$ V
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL} = 0.8$ V Max., $V_{IH} = 2$ V Min.
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}

Unloading Data

As soon as the first word has rippled to the output, the data-out ready output (DOR) goes HIGH and data of the first word is available on the outputs. Data of other words can be removed by a negative-going transition on the shift-out input (SO). This negative-going transition causes the DOR signal to go LOW while the next word moves to the output. As long as valid data is available in the FIFO, the DOR signal will go high again, signifying that the next word is ready at the output. When the FIFO is empty, DOR will remain LOW, and any further commands will be ignored until a "1" marker ripples down to the last control register and DOR goes HIGH.

CD54/74HC40105

CD54/74HCT40105

If during unloading SI is HIGH, (FIFO is full) data on the data input of the FIFO is entered in the first location.

Master Reset

A high on the MASTER RESET (MR) sets all the control logic marker bits to "0". DOR goes low and DIR goes high. The contents of the data register are not changed, only declared invalid, and will be superseded when the first word is loaded. Thus, MR does not clear data within the register but only the control logic. If the shift-in flag (SI) is HIGH during the master reset pulse, data present at the input (D0 to D3) are immediately moved into the first location upon completion of the reset process.

3-State Outputs

In order to facilitate data busing, 3-state outputs (Q0 to Q3) are provided on the data output lines, while the load condition of the register can be detected by the state of the DOR output. A HIGH on the 3-state control flag (output enable input OE) forces the outputs into the high-impedance OFF-state mode. Note that the shift-out signal, unlike that in

the RCA-CD40105B, is independent of the 3-state output control. In the CD40105B, the 3-state control must not be shifted from High to Low when the shift-out signal is Low (data loss would occur). In the high-speed CMOS version this restriction has been eliminated.

Cascading

The 40105 can be cascaded to form longer registers simply by connecting the DIR to SO and DOR to SI. In the cascaded mode, a MASTER RESET pulse must be applied after the supply voltage is turned on. For words wider than four bits, the DIR and the DOR outputs must be gated together with AND gates. Their outputs drive the SI and SO inputs in parallel, if expanding is done in both directions (see Figs. 3 and 4).

The CD54HC40105 and CD54HCT40105 are supplied in 16-lead hermetic dual-in-line frit-seal ceramic packages (F suffix). The CD74HC40105 and CD74HCT40105 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):

(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) ± 20 mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ± 20 mA

DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V) ± 25 mA

DC V_{CC} OR GROUND CURRENT (I_{CC}) ± 50 mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW

For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H) 500 mW

For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW

For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M) 400 mW

For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to $+125^\circ\text{C}$

PACKAGE TYPE E, M -40 to $+85^\circ\text{C}$

STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ\text{C}$

Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only $+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package Temperature Range) V_{CC}^*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage, V_i , V_o	0	V_{CC}	V
Operating Temperature, T_A :			
CD74 Types	-40	+85	$^\circ\text{C}$
CD54 Types	-55	+125	
Input Rise and Fall Times, t_r , t_f :			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC40105

CD54/74HCT40105

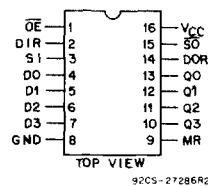
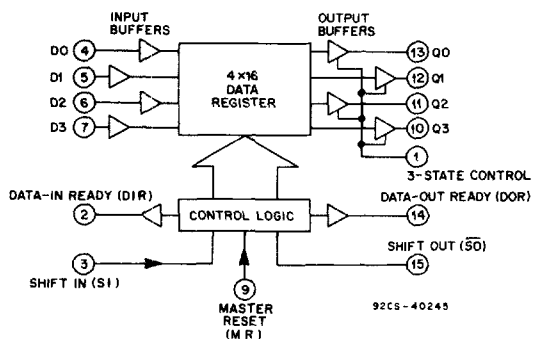


Fig. 1 - Functional block diagram.

TERMINAL ASSIGNMENT

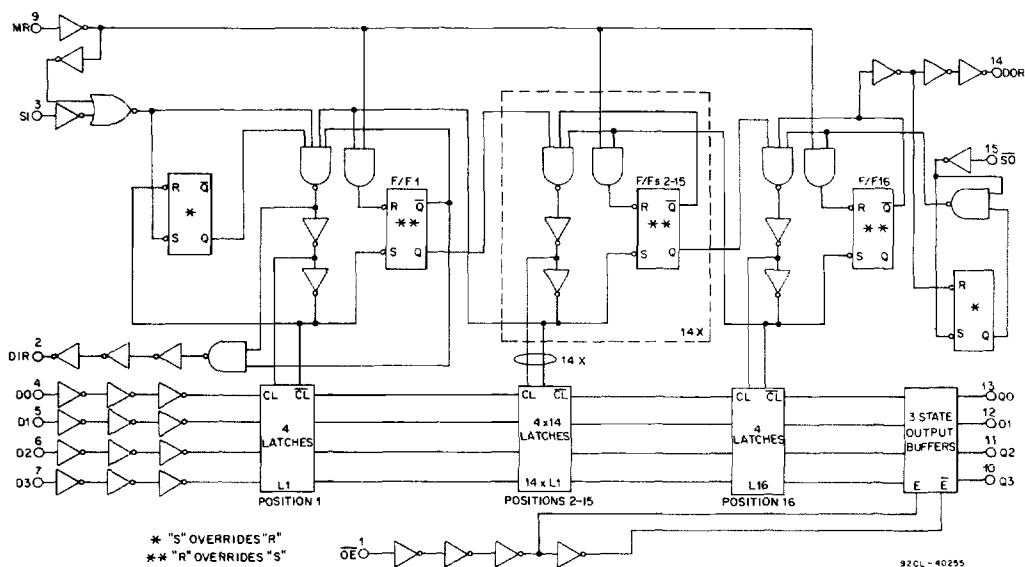


Fig. 2 - Logic diagram.

CD54/74HC40105

CD54/74HCT40105

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC40105/CD54HC40105											CD74HCT40105/CD54HCT40105											UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES					
	V _I V	I _O mA	V _{OC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{OC} V	+25°C			-40/ +85°C		-55/ +125°C					
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max				
High-Level Input Voltage	V _{IH}		2	1.5	—	—	1.5	—	1.5	—	—	4.5	to	2	—	—	2	—	2	—	V		
			4.5	3.15	—	—	3.15	—	3.15	—	—	5.5											
			6	4.2	—	—	4.2	—	4.2	—	—												
Low-Level Input Voltage	V _{IL}		2	—	—	0.5	—	0.5	—	0.5	—	4.5	to	—	—	0.8	—	0.8	—	0.8	V		
			4.5	—	—	1.35	—	1.35	—	1.35	—	5.5											
			6	—	—	1.8	—	1.8	—	1.8	—												
High-Level Output Voltage	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V		
CMOS Loads				4.5	4.4	—	—	4.4	—	4.4	—												
				6	5.9	—	—	5.9	—	5.9	—												
TTL Loads	V _{IL} or V _{IH}	V _{IL} or V _{IH}		—	—	—	—	—	—	—	—	V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V		
			-4	4.5	3.98	—	—	3.84	—	3.7	—												
			-5.2	6	5.48	—	—	5.34	—	5.2	—												
Low-Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V		
CMOS Loads				4.5	—	—	0.1	—	0.1	—	0.1												
				6	—	—	0.1	—	0.1	—	0.1												
TTL Loads	V _{IL} or V _{IH}	V _{IL} or V _{IH}		—	—	—	—	—	—	—	—	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V		
			4	4.5	—	—	0.26	—	0.33	—	0.4												
			5.2	6	—	—	0.26	—	0.33	—	0.4												
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA		
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA		
Additional Quiescent Device Current per input pin: 1 unit load	ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA		
3-State Leakage Current	I _{OZ}	V _{IL} or V _{IH}	V _O =V _{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V _{IL} or V _{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA		

*For dual-supply systems theoretical worst case ($V_i = 2.4$ V, $V_{cc} = 5.5$ V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
$\overline{OE}$	0.75
SI, SO	0.4
Dn	0.3
MR	1.5

*Unit Load is ΔI_{cc} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC40105

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SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 6\text{ ns}$)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL		UNITS
			HC	HCT	
Propagation Delay	t_{PLH} t_{PHL}	15	15	15	ns
MR to DIR, DOR			35	35	
$\overline{S}O$ to Qn			18	18	
SI to DIR	t_{PHL}		18	18	
$\overline{S}O$ to DOR					
Maximum SI, $\overline{S}O$ Frequency	$f_{max.}$	15	32	32	MHz
Power Dissipation Capacitance*	C_{PD}	—	83	83	pF

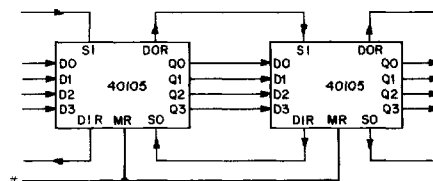
* C_{PD} is used to determine the dynamic power consumption, per package.

PD = $C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V _{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
SI Pulse Width: HIGH or LOW	t _w Fig. 6	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
S $\overline{O}$ Pulse Width HIGH or LOW	t _w Fig. 7	2	120	—	—	—	150	—	—	—	180	—	—	—	
		4.5	24	—	16	—	30	—	20	—	36	—	24	—	
		6	20	—	—	—	26	—	—	—	31	—	—	—	
DIR Pulse Width HIGH or LOW	t _w Fig. 6	2	200	—	—	—	250	—	—	—	300	—	—	—	
		4.5	40	—	40	—	50	—	50	—	60	—	60	—	
		6	34	—	—	—	43	—	—	—	51	—	—	—	
DOR Pulse Width HIGH or LOW	t _w Fig. 7	2	200	—	—	—	250	—	—	—	300	—	—	—	
		4.5	40	—	40	—	50	—	50	—	60	—	60	—	
		6	34	—	—	—	43	—	—	—	51	—	—	—	
MR Pulse Width HIGH	t _w Fig. 5	2	120	—	—	—	150	—	—	—	180	—	—	—	
		4.5	24	—	24	—	30	—	30	—	36	—	36	—	
		6	20	—	—	—	26	—	—	—	31	—	—	—	
Removal Time MR to SI	t _{REM} Fig. 12	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	15	—	13	—	19	—	15	—	22	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Setup Time Dn to SI	t _{SU} Fig. 13	2	5	—	—	—	5	—	—	—	5	—	—	—	
		4.5	5	—	0	—	5	—	0	—	5	—	0	—	
		6	5	—	—	—	5	—	—	—	5	—	—	—	
Hold Time Dn to SI	t _H Fig. 13	2	125	—	—	—	155	—	—	—	190	—	—	—	
		4.5	25	—	25	—	31	—	31	—	38	—	38	—	
		6	21	—	—	—	26	—	—	—	32	—	—	—	
Maximum Pulse Frequency SI, S $\overline{O}$	f _{MAX} Figs. 6, 7	2	3	—	—	—	2	—	—	—	2	—	—	—	MHz
		4.5	15	—	15	—	12	—	12	—	10	—	10	—	
		6	18	—	—	—	14	—	—	—	12	—	—	—	

CHARACTERISTIC		V _{CC} (V)	LIMITS												UNITS
			25° C				-40° C to +85° C				-55° C to +125° C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay,	t _{PHL}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
	t _{PLH}	4.5	—	35	—	36	—	44	—	45	—	53	—	54	
MR to DIR, DOR	Fig. 5	6	—	30	—	—	—	37	—	—	—	45	—	—	
Propagation Delay,	t _{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	42	—	53	—	53	—	63	—	63	
SI to DIR	Fig. 6	6	—	36	—	—	—	45	—	—	—	54	—	—	
Propagation Delay,	t _{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	42	—	53	—	53	—	63	—	63	
$\overline{SO}$ to DOR	Fig. 7	6	—	36	—	—	—	45	—	—	—	54	—	—	
Propagation Delay,	t _{PHL}	2	—	400	—	—	—	500	—	—	—	600	—	—	
	t _{PLH}	4.5	—	80	—	80	—	100	—	100	—	120	—	120	
$\overline{SO}$ to Qn	Fig. 8	6	—	68	—	—	—	85	—	—	—	102	—	—	
Propagation Delay/ Ripple thru Delay	t _{PLH}	2	—	2000	—	—	—	2500	—	—	—	3000	—	—	
		4.5	—	400	—	400	—	500	—	500	—	600	—	600	
SI to DOR	Fig. 9	6	—	340	—	—	—	425	—	—	—	510	—	—	
Propagation Delay/ Ripple thru Delay	t _{PLH}	2	—	2500	—	—	—	3125	—	—	—	3750	—	—	
		4.5	—	500	—	500	—	625	—	625	—	750	—	750	
$\overline{SO}$ to DIR	Fig. 10	6	—	425	—	—	—	532	—	—	—	638	—	—	
Propagation Delay/ Ripple thru Delay	t _{PHL}	2	—	1500	—	—	—	1900	—	—	—	2250	—	—	
	t _{PLH}	4.5	—	300	—	300	—	380	—	380	—	450	—	450	
SI to Qn		6	—	260	—	—	—	330	—	—	—	380	—	—	
3-State Output Enable	t _{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
	t _{PZL}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	
OE to Qn	Fig. 11	6	—	26	—	—	—	33	—	—	—	38	—	—	
3-State Output Disable	t _{PHZ}	2	—	140	—	—	—	175	—	—	—	210	—	—	
	t _{PLZ}	4.5	—	28	—	30	—	35	—	38	—	42	—	45	
OE to Qn	Fig. 11	6	—	24	—	—	—	30	—	—	—	36	—	—	
Output Transition Time	t _{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t _{TLH}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
	Fig. 8	6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C														



92CS-40243

Fig. 3 - Expansion, 4-bits wide by 16 N-bits long.

CD54/74HC40105 CD54/74HCT40105

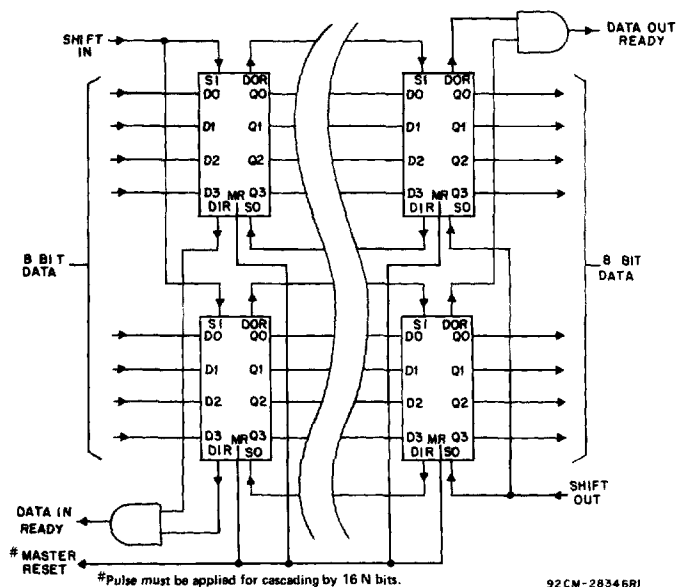


Fig. 4 - Expansion, 8-bits wide by 16 N-bits long using HC/HCT40105.

AC WAVEFORMS

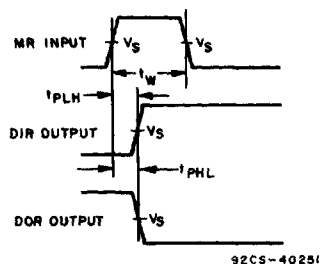


Fig. 5 - Waveforms showing the MR input to DIR, DOR output propagation delays and the MR pulse width.

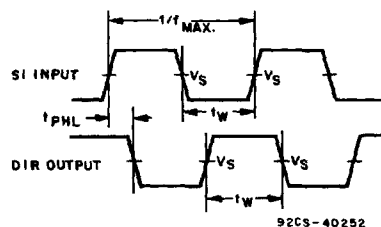


Fig. 6 - Waveforms showing the SI input to DIR output propagation delay. The SI, DIR pulse widths and SI maximum pulse frequency.

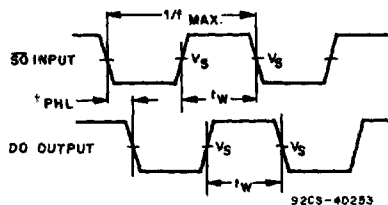


Fig. 7 - Waveforms showing the $\overline{SO}$ input to DOR output propagation delay. The $\overline{SO}$, DOR pulse widths and $\overline{SO}$ maximum pulse frequency.

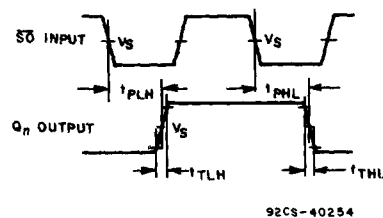


Fig. 8 - Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.

CD54/74HC40105

CD54/74HCT40105

• DATA VALID GOES TO HIGH LEVEL IN ADVANCE OF THE DATA OUT BY A MAXIMUM OF 38 ns AT $V_{CC} = 4.5$ V, FOR $C_L = 50$ pF AND $T_A = 25^\circ\text{C}$

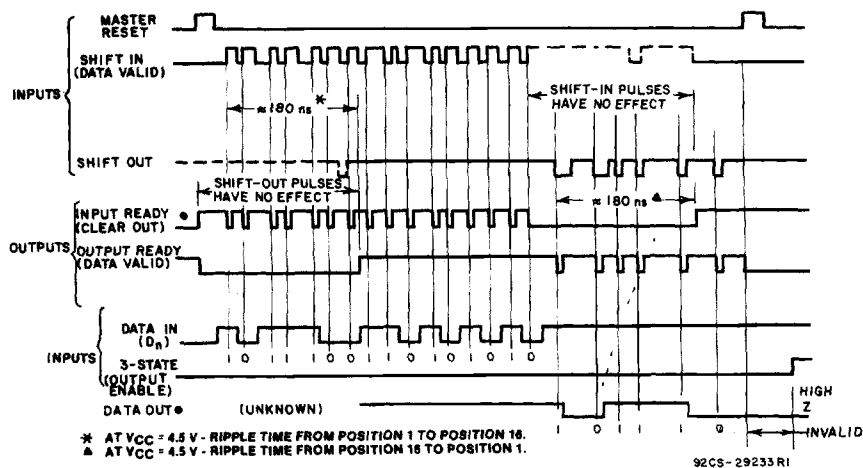


Fig. 14 - Timing diagram for the CD54/74HC/HCT40105.